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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	79
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-1200ze-2tg100ir1

This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the t_{LOCK} parameter has been satisfied.

The MachXO2 also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the [sysCLOCK PLL Timing](#) table.

The MachXO2 PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the t_{LOCK} parameter has been satisfied. The timing parameters for the PLL are shown in the [sysCLOCK PLL Timing](#) table.

For more details on the PLL and the WISHBONE interface, see TN1199, [MachXO2 sysCLOCK PLL Design and Usage Guide](#).

Figure 2-7. PLL Diagram

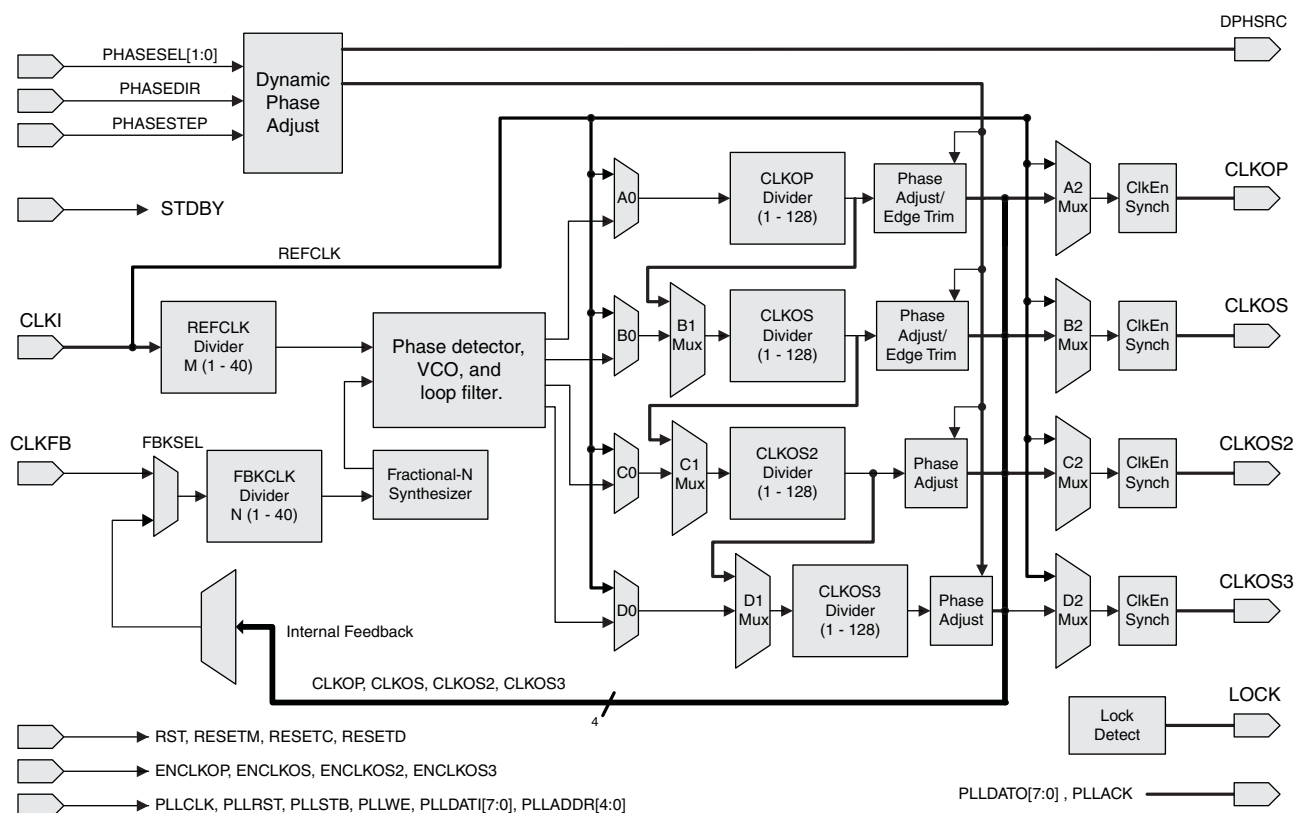
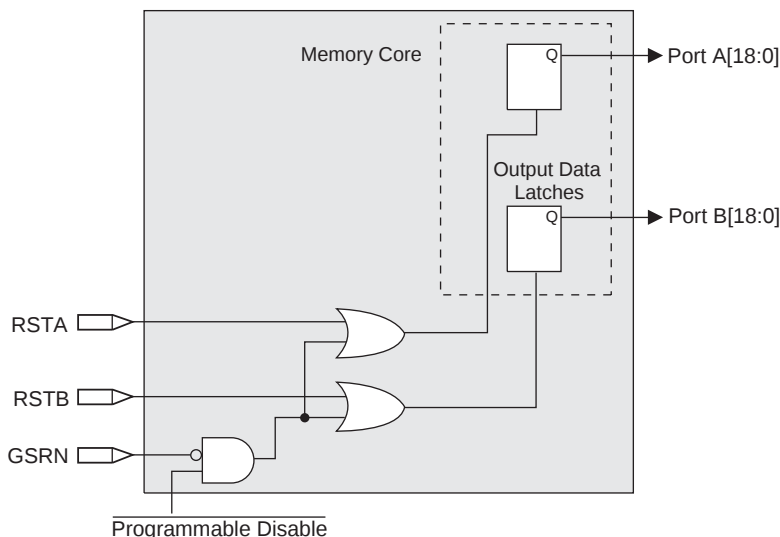


Table 2-4 provides signal descriptions of the PLL block.

Table 2-4. PLL Signal Descriptions

Port Name	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	I	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	I	Dynamic Phase step – toggle shifts VCO phase adjust by one step.

Figure 2-9. Memory Core Reset

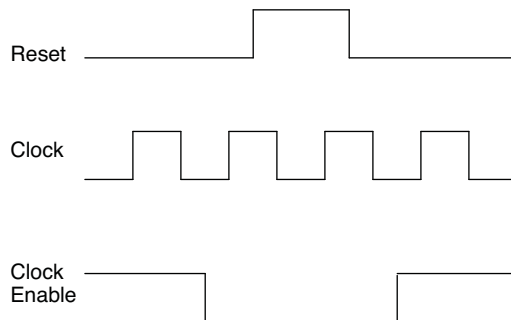


For further information on the sysMEM EBR block, please refer to TN1201, [Memory Usage Guide for MachXO2 Devices](#).

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-10. The reset timing rules apply to the RPRreset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPRreset are always asynchronous EBR inputs. For more details refer to TN1201, [Memory Usage Guide for MachXO2 Devices](#).

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

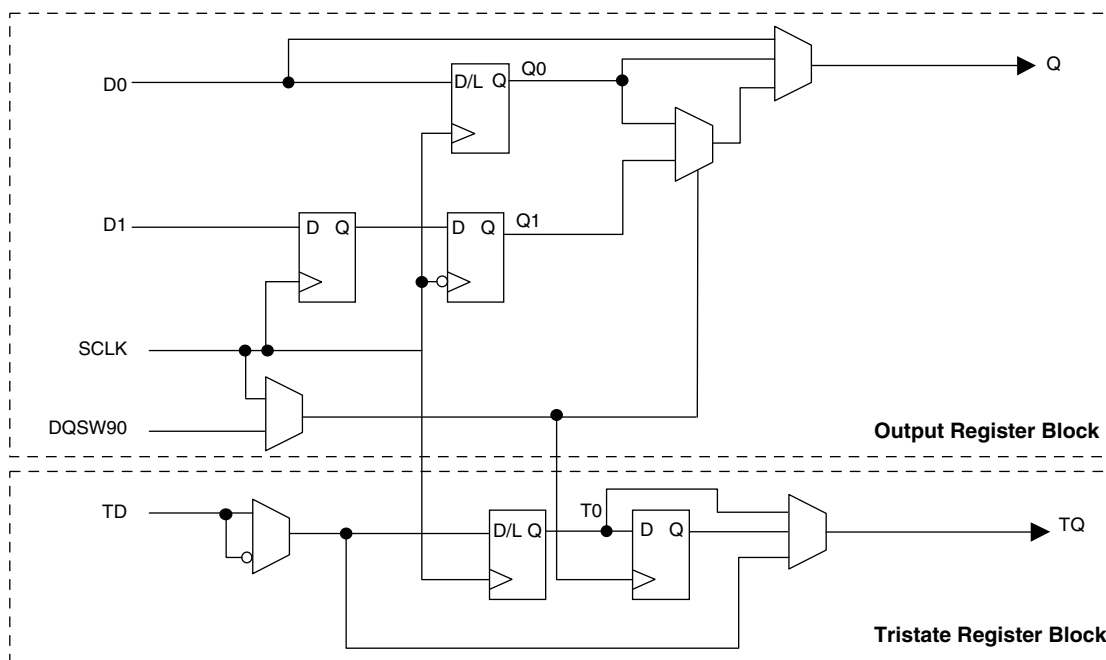
Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO2 devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO2 devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

The MachXO2-640U, MachXO2-1200/U and higher density devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these higher density devices have on-chip differential termination and also provide PCI support.

Figure 2-15. MachXO2 Output Register Block Diagram (PIO on the Right Edges)



Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

The tri-state register blocks on the right edge contain an additional register for DDR memory operation. In DDR memory mode, the register TS input is fed into another register that is clocked using the DQSW90 signal. The output of this register is used as a tri-state control.

Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

Table 2-9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDR4(1:8): Q[7:0] GDDR2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDR2(1:4)(IOL-C): Q0, Q1, Q2, Q3

More information on the input gearbox is available in TN1203, [Implementing High-Speed Interfaces with MachXO2 Devices](#).

Output Gearbox

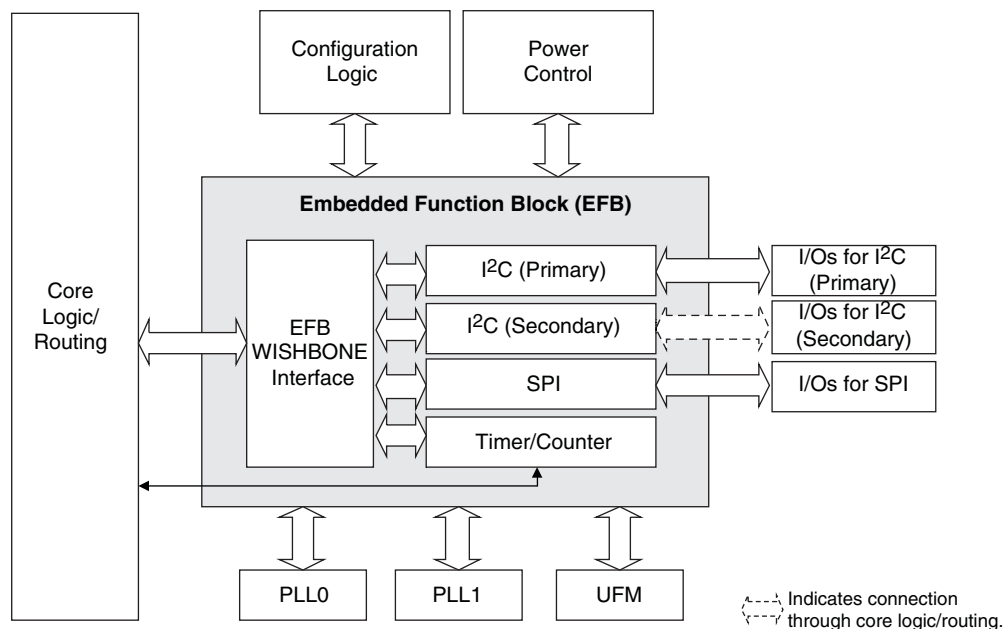
Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDR4 (8:1) gearbox or as two ODDR2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

Table 2-10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDR4(8:1): D[7:0]		
GDDR2(4:1)(IOL-A): D[3:0]		
GDDR2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-17 shows the output gearbox block diagram.

Figure 2-20. Embedded Function Block Interface



Hardened I²C IP Core

Every MachXO2 device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I²C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface

There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#) (Appendix B)
- TN1205, [Using User Flash Memory and Hardened Control Functions in MachXO2 Devices](#)

Figure 2-22. SPI Core Block Diagram

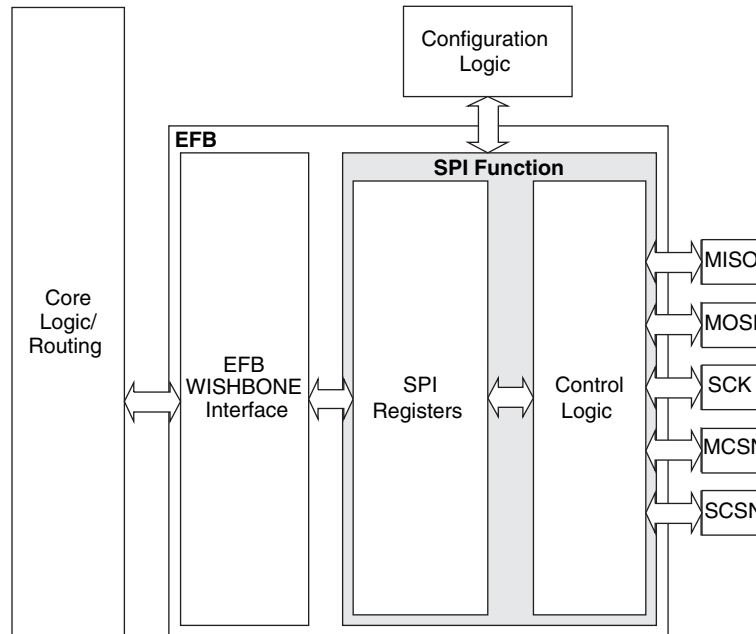


Table 2-16 describes the signals interfacing with the SPI cores.

Table 2-16. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	O	Master	SPI master chip-select output
spi_csn[1..7]	O	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	O	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
ufm_sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the User Flash Memory (UFM).
cfg_stdbby	O	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.
cfg_wake	O	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.

Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, [Boundary Scan Testability with Lattice sysIO Capability](#) and TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#).

Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I²C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

1. Internal Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I²C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, [MachXO2 Programming and Configuration Usage Guide](#) for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#) for details.

Power-On-Reset Voltage Levels^{1, 2, 3, 4, 5}

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and V_{CCIO0})	0.9	—	1.06	V
$V_{PORUPEXT}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	—	2.1	V
$V_{PORDNBG}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CCINT})	0.75	—	0.93	V
$V_{PORDNBGEXT}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	—	1.33	V
$V_{PORDNSRAM}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CCINT})	—	0.6	—	V
$V_{PORDNSRAMEXT}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	—	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.
3. Note that V_{PORUP} (min.) and $V_{PORDNBG}$ (max.) are in different process corners. For any given process corner $V_{PORDNBG}$ (max.) is always 12.0 mV below V_{PORUP} (min.).
4. $V_{PORUPEXT}$ is for HC devices only. In these devices a separate POR circuit monitors the external V_{CC} power supply.
5. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

Programming/Erase Specifications

Symbol	Parameter	Min.	Max. ¹	Units
N_{PROG}	Flash Programming cycles per $t_{RETENTION}$	—	10,000	Cycles
	Flash functional programming cycles	—	100,000	
$t_{RETENTION}$	Data retention at 100 °C junction temperature	10	—	Years
	Data retention at 85 °C junction temperature	20	—	

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

Hot Socketing Specifications^{1, 2, 3}

Symbol	Parameter	Condition	Max.	Units
I_{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/-1000	μA

1. Insensitive to sequence of V_{CC} and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO} .
2. $0 < V_{CC} < V_{CC} (MAX)$, $0 < V_{CCIO} < V_{CCIO} (MAX)$.
3. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} .

ESD Performance

Please refer to the [MachXO2 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
LVDS25	400	MHz
LVDS25E	150	MHz
RSDS25	150	MHz
RSDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
SSTL25_I	150	MHz
SSTL25_II	150	MHz
SSTL25D_I	150	MHz
SSTL25D_II	150	MHz
SSTL18_I	150	MHz
SSTL18_II	150	MHz
SSTL18D_I	150	MHz
SSTL18D_II	150	MHz
HSTL18_I	150	MHz
HSTL18_II	150	MHz
HSTL18D_I	150	MHz
HSTL18D_II	150	MHz
PCI33	134	MHz
LVTTTL33	150	MHz
LVTTTL33D	150	MHz
LVC MOS33	150	MHz
LVC MOS33D	150	MHz
LVC MOS25	150	MHz
LVC MOS25D	150	MHz
LVC MOS25R33	150	MHz
LVC MOS18	150	MHz
LVC MOS18D	150	MHz
LVC MOS18R33	150	MHz
LVC MOS18R25	150	MHz
LVC MOS15	150	MHz
LVC MOS15D	150	MHz
LVC MOS15R33	150	MHz
LVC MOS15R25	150	MHz
LVC MOS12	91	MHz
LVC MOS12D	91	MHz

MachXO2 External Switching Characteristics – ZE Devices^{1, 2, 3, 4, 5, 6, 7}

Over Recommended Operating Conditions

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f _{MAX_PRI} ⁸	Frequency for Primary Clock Tree	All MachXO2 devices	—	150	—	125	—	104	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	1.00	—	1.20	—	1.40	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO2-256ZE	—	1250	—	1272	—	1296	ps
		MachXO2-640ZE	—	1161	—	1183	—	1206	ps
		MachXO2-1200ZE	—	1213	—	1267	—	1322	ps
		MachXO2-2000ZE	—	1204	—	1250	—	1296	ps
		MachXO2-4000ZE	—	1195	—	1233	—	1269	ps
		MachXO2-7000ZE	—	1243	—	1268	—	1296	ps
Edge Clock									
f _{MAX_EDGE} ⁸	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	210	—	175	—	146	MHz
Pin-LUT-Pin Propagation Delay									
t _{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	—	9.35	—	9.78	—	10.21	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t _{CO}	Clock to Output – PIO Output Register	MachXO2-256ZE	—	10.46	—	10.86	—	11.25	ns
		MachXO2-640ZE	—	10.52	—	10.92	—	11.32	ns
		MachXO2-1200ZE	—	11.24	—	11.68	—	12.12	ns
		MachXO2-2000ZE	—	11.27	—	11.71	—	12.16	ns
		MachXO2-4000ZE	—	11.28	—	11.78	—	12.28	ns
		MachXO2-7000ZE	—	11.22	—	11.76	—	12.30	ns
t _{SU}	Clock to Data Setup – PIO Input Register	MachXO2-256ZE	–0.21	—	–0.21	—	–0.21	—	ns
		MachXO2-640ZE	–0.22	—	–0.22	—	–0.22	—	ns
		MachXO2-1200ZE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-2000ZE	–0.27	—	–0.27	—	–0.27	—	ns
		MachXO2-4000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-7000ZE	–0.33	—	–0.33	—	–0.33	—	ns
t _H	Clock to Data Hold – PIO Input Register	MachXO2-256ZE	3.96	—	4.25	—	4.65	—	ns
		MachXO2-640ZE	4.01	—	4.31	—	4.71	—	ns
		MachXO2-1200ZE	3.95	—	4.29	—	4.73	—	ns
		MachXO2-2000ZE	3.94	—	4.29	—	4.74	—	ns
		MachXO2-4000ZE	3.96	—	4.36	—	4.87	—	ns
		MachXO2-7000ZE	3.93	—	4.37	—	4.91	—	ns

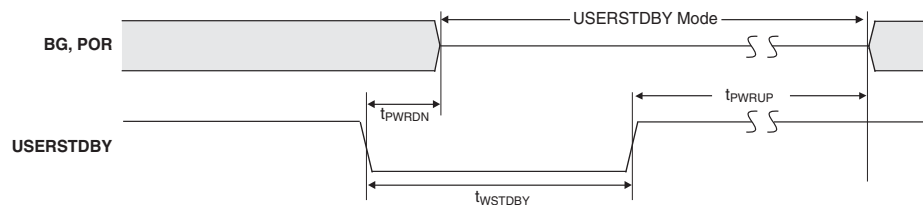
MachXO2 Oscillator Output Frequency

Symbol	Parameter	Min.	Typ.	Max	Units
f_{MAX}	Oscillator Output Frequency (Commercial Grade Devices, 0 to 85°C)	125.685	133	140.315	MHz
	Oscillator Output Frequency (Industrial Grade Devices, -40 °C to 100 °C)	124.355	133	141.645	MHz
t_{DT}	Output Clock Duty Cycle	43	50	57	%
t_{OPJIT}^1	Output Clock Period Jitter	0.01	0.012	0.02	UIPP
$t_{STABLEOSC}$	STDBY Low to Oscillator Stable	0.01	0.05	0.1	μs

1. Output Clock Period Jitter specified at 133 MHz. The values for lower frequencies will be smaller UIPP. The typical value for 133 MHz is 95 ps and for 2.08 MHz the typical value is 1.54 ns.

MachXO2 Standby Mode Timing – HC/HE Devices

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	USERSTDBY High to Stop	All	—	—	9	ns
t_{PWRUP}	USERSTDBY Low to Power Up	LCMXO2-256		—		μs
		LCMXO2-640		—		μs
		LCMXO2-640U		—		μs
		LCMXO2-1200	20	—	50	μs
		LCMXO2-1200U		—		μs
		LCMXO2-2000		—		μs
		LCMXO2-2000U		—		μs
		LCMXO2-4000		—		μs
		LCMXO2-7000		—		μs
t_{WSTDBY}	USERSTDBY Pulse Width	All	18	—	—	ns



MachXO2 Standby Mode Timing – ZE Devices

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	USERSTDBY High to Stop	All	—	—	13	ns
t_{PWRUP}	USERSTDBY Low to Power Up	LCMXO2-256		—		μs
		LCMXO2-640		—		μs
		LCMXO2-1200	20	—	50	μs
		LCMXO2-2000		—		μs
		LCMXO2-4000		—		μs
		LCMXO2-7000		—		μs
t_{WSTDBY}	USERSTDBY Pulse Width	All	19	—	—	ns
$t_{BNDGAPSTBL}$	USERSTDBY High to Bandgap Stable	All	—	—	15	ns

	MachXO2-2000						MachXO2-2000U
	49 WLCSP	100 TQFP	132 csBGA	144 TQFP	256 caBGA	256 ftBGA	484 ftBGA
General Purpose I/O per Bank							
Bank 0	19	18	25	27	50	50	70
Bank 1	0	21	26	28	52	52	68
Bank 2	13	20	28	28	52	52	72
Bank 3	0	6	7	8	16	16	24
Bank 4	0	6	8	10	16	16	16
Bank 5	6	8	10	10	20	20	28
Total General Purpose Single-Ended I/O	38	79	104	111	206	206	278
Differential I/O per Bank							
Bank 0	7	9	13	14	25	25	35
Bank 1	0	10	13	14	26	26	34
Bank 2	6	10	14	14	26	26	36
Bank 3	0	3	3	4	8	8	12
Bank 4	0	3	4	5	8	8	8
Bank 5	3	4	5	5	10	10	14
Total General Purpose Differential I/O	16	39	52	56	103	103	139
Dual Function I/O							
	24	31	33	33	33	33	37
High-speed Differential I/O							
Bank 0	5	4	8	9	14	14	18
Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	4	8	9	14	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	10	14	14	14	14	18
DQS Groups							
Bank 1	0	1	2	2	2	2	2
VCCIO Pins							
Bank 0	2	2	3	3	4	4	10
Bank 1	0	2	3	3	4	4	10
Bank 2	1	2	3	3	4	4	10
Bank 3	0	1	1	1	1	1	3
Bank 4	0	1	1	1	2	2	4
Bank 5	1	1	1	1	1	1	3
VCC	2	2	4	4	8	8	12
GND	4	8	10	12	24	24	48
NC	0	1	1	4	1	1	105
Reserved for Configuration	1	1	1	1	v	1	1
Total Count of Bonded Pins	39	100	132	144	256	256	484

	MachXO2-4000							
	84 QFN	132 csBGA	144 TQFP	184 csBGA	256 caBGA	256 ftBGA	332 caBGA	484 fpBGA
General Purpose I/O per Bank								
Bank 0	27	25	27	37	50	50	68	70
Bank 1	10	26	29	37	52	52	68	68
Bank 2	22	28	29	39	52	52	70	72
Bank 3	0	7	9	10	16	16	24	24
Bank 4	9	8	10	12	16	16	16	16
Bank 5	0	10	10	15	20	20	28	28
Total General Purpose Single Ended I/O	68	104	114	150	206	206	274	278
Differential I/O per Bank								
Bank 0	13	13	14	18	25	25	34	35
Bank 1	4	13	14	18	26	26	34	34
Bank 2	11	14	14	19	26	26	35	36
Bank 3	0	3	4	4	8	8	12	12
Bank 4	4	4	5	6	8	8	8	8
Bank 5	0	5	5	7	10	10	14	14
Total General Purpose Differential I/O	32	52	56	72	103	103	137	139
Dual Function I/O								
	28	37	37	37	37	37	37	37
High-speed Differential I/O								
Bank 0	8	8	9	8	18	18	18	18
Gearboxes								
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	8	8	9	9	18	18	18	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	11	14	14	12	18	18	18	18
DQS Groups								
Bank 1	1	2	2	2	2	2	2	2
VCCIO Pins								
Bank 0	3	3	3	3	4	4	4	10
Bank 1	1	3	3	3	4	4	4	10
Bank 2	2	3	3	3	4	4	4	10
Bank 3	1	1	1	1	1	1	2	3
Bank 4	1	1	1	1	2	2	1	4
Bank 5	1	1	1	1	1	1	2	3
VCC								
	4	4	4	4	8	8	8	12
GND								
	4	10	12	16	24	24	27	48
NC								
	1	1	1	1	1	1	5	105
Reserved for configuration								
	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	84	132	144	184	256	256	332	484

Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32C	256	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-256ZE-2SG32C	256	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-256ZE-3SG32C	256	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-256ZE-1UMG64C	256	1.2 V	–1	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-2UMG64C	256	1.2 V	–2	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-3UMG64C	256	1.2 V	–3	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-1TG100C	256	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-2TG100C	256	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-3TG100C	256	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-1MG132C	256	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-2MG132C	256	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-3MG132C	256	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100C	640	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-2TG100C	640	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-3TG100C	640	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-1MG132C	640	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-2MG132C	640	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-3MG132C	640	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1SG32C	1280	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-2SG32C	1280	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-3SG32C	1280	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-1TG100C	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100C	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100C	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132C	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132C	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132C	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144C	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144C	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144C	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1TG100C	2112	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-2TG100C	2112	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-3TG100C	2112	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-1MG132C	2112	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-2MG132C	2112	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-3MG132C	2112	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-1TG144C	2112	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-2TG144C	2112	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-3TG144C	2112	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-1BG256C	2112	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-2BG256C	2112	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-3BG256C	2112	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-1FTG256C	2112	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-2000ZE-2FTG256C	2112	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-2000ZE-3FTG256C	2112	1.2 V	–3	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000ZE-1QN84C	4320	1.2 V	–1	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-2QN84C	4320	1.2 V	–2	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-3QN84C	4320	1.2 V	–3	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-1MG132C	4320	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-2MG132C	4320	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-3MG132C	4320	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-1TG144C	4320	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-2TG144C	4320	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-3TG144C	4320	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-1BG256C	4320	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-2BG256C	4320	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-3BG256C	4320	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-1FTG256C	4320	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-2FTG256C	4320	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-3FTG256C	4320	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-1BG332C	4320	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-2BG332C	4320	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-3BG332C	4320	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-1FG484C	4320	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-4000ZE-2FG484C	4320	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-4000ZE-3FG484C	4320	1.2 V	–3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144C	6864	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-2TG144C	6864	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-3TG144C	6864	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-1BG256C	6864	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-2BG256C	6864	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-3BG256C	6864	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-1FTG256C	6864	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-2FTG256C	6864	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-3FTG256C	6864	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-1BG332C	6864	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-2BG332C	6864	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-3BG332C	6864	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-1FG484C	6864	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-2FG484C	6864	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-3FG484C	6864	1.2 V	–3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100CR1 ¹	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100CR1 ¹	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100CR1 ¹	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132CR1 ¹	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132CR1 ¹	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132CR1 ¹	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144CR1 ¹	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144CR1 ¹	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144CR1 ¹	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200ZE-speed package CR1” are the same as the “LCMXO2-1200ZE-speed package C” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32C	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	COM
LCMXO2-256HC-5SG32C	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	COM
LCMXO2-256HC-6SG32C	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	COM
LCMXO2-256HC-4SG48C	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	COM
LCMXO2-256HC-5SG48C	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	COM
LCMXO2-256HC-6SG48C	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	COM
LCMXO2-256HC-4UMG64C	256	2.5 V / 3.3 V	–4	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-5UMG64C	256	2.5 V / 3.3 V	–5	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-6UMG64C	256	2.5 V / 3.3 V	–6	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-4TG100C	256	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-256HC-5TG100C	256	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-256HC-6TG100C	256	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-256HC-4MG132C	256	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-256HC-5MG132C	256	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-256HC-6MG132C	256	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48C	640	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	COM
LCMXO2-640HC-5SG48C	640	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	COM
LCMXO2-640HC-6SG48C	640	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	COM
LCMXO2-640HC-4TG100C	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-640HC-5TG100C	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-640HC-6TG100C	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-640HC-4MG132C	640	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-640HC-5MG132C	640	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-640HC-6MG132C	640	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144C	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-5TG144C	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-6TG144C	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144C	6864	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-5TG144C	6864	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-6TG144C	6864	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-4BG256C	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-5BG256C	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-6BG256C	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-4FTG256C	6864	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-5FTG256C	6864	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-6FTG256C	6864	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-4BG332C	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-5BG332C	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-6BG332C	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-4FG400C	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-5FG400C	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-6FG400C	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-4FG484C	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-5FG484C	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-6FG484C	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100CR1 ¹	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100CR1 ¹	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100CR1 ¹	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132CR1 ¹	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132CR1 ¹	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132CR1 ¹	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144CR1 ¹	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144CR1 ¹	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144CR1 ¹	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200HC-speed package CR1” are the same as the “LCMXO2-1200HC-speed package C” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1UWG49ITR ¹	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR50 ³	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR1K ²	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1TG100I	2112	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-2TG100I	2112	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-3TG100I	2112	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-1MG132I	2112	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-2MG132I	2112	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-3MG132I	2112	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-1TG144I	2112	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-2TG144I	2112	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-3TG144I	2112	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-1BG256I	2112	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-2BG256I	2112	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-3BG256I	2112	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-1FTG256I	2112	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-2FTG256I	2112	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-3FTG256I	2112	1.2 V	–3	Halogen-Free ftBGA	256	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.