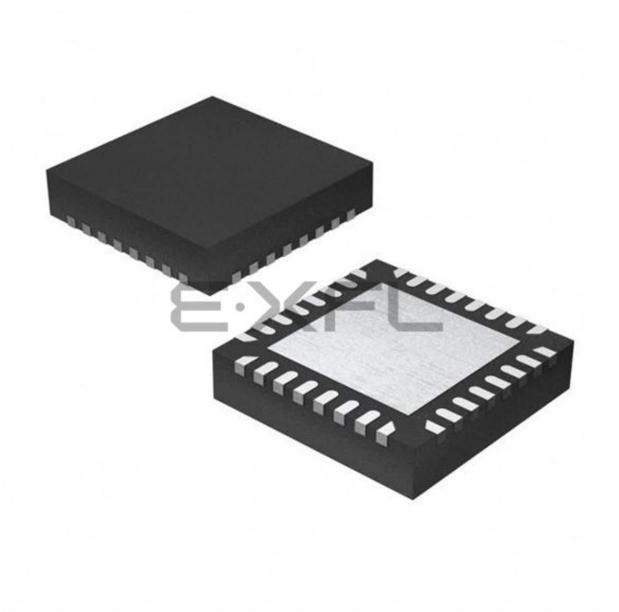
# Lattice Semiconductor Corporation - LCMXO2-1200ZE-3SG32C Datasheet



**Welcome to** E-XFL.COM

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

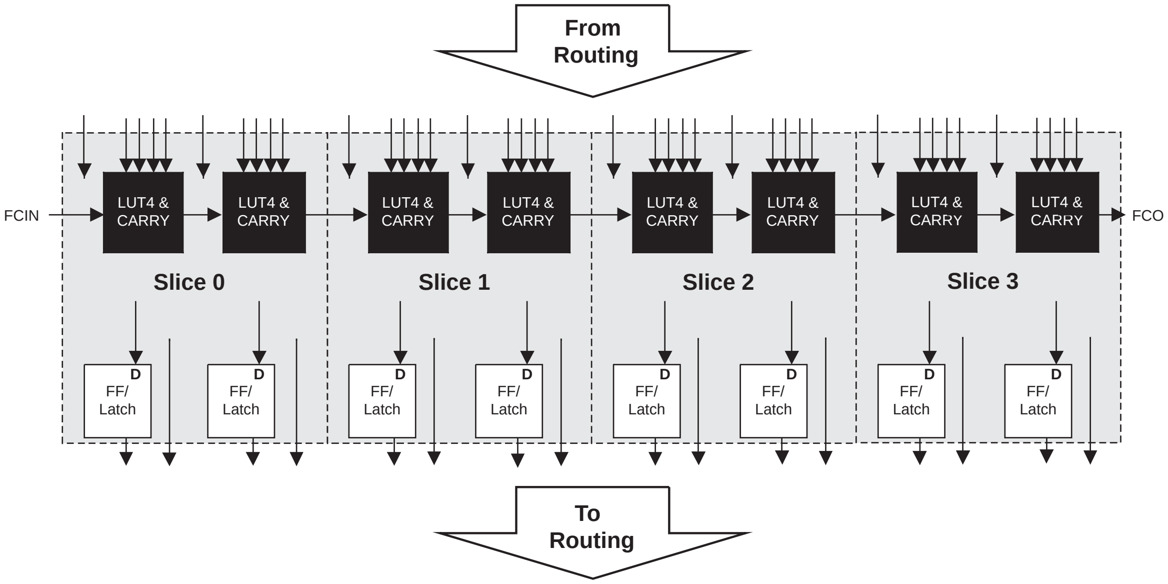
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 160 |
| Number of Logic Elements/Cells | 1280 |
| Total RAM Bits | 65536 |
| Number of I/O | 21 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 32-UFQFN Exposed Pad |
| Supplier Device Package | 32-QFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-1200ze-3sg32c |

*Figure 2-3. PFU Block Diagram*



## Slices

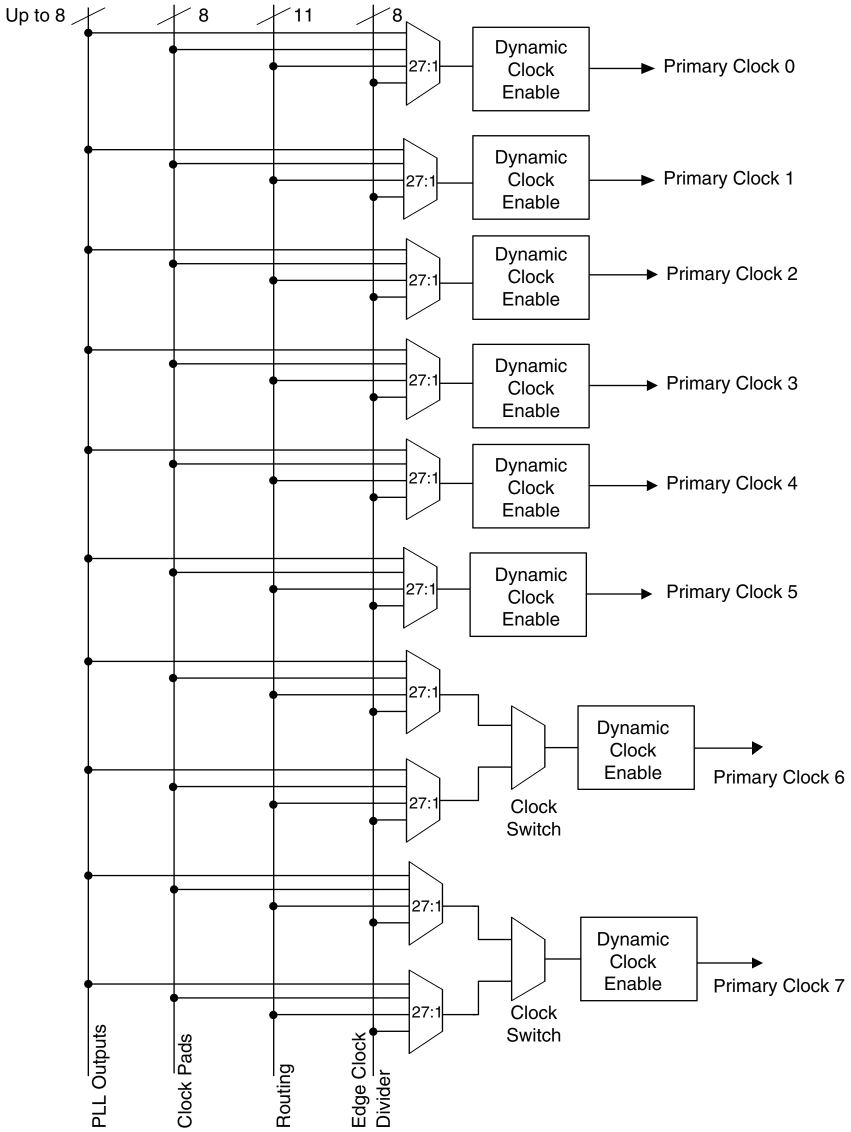
Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

*Table 2-1. Resources and Modes Available per Slice*

| | PFU Block | |
|---|---|---|
| **Slice** | **Resources** | **Modes** |
| Slice 0 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 1 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 2 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 3 | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.

*Figure 2-5. Primary Clocks for MachXO2 Devices*



Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO2 External Switching Characteristics table.

*Table 2-5. sysMEM Block Configurations*

| Memory Mode | Configurations |
|---|---|
| Single Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9 |
| True Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9 |
| Pseudo Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |
| FIFO | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |

### Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

### RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO2 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

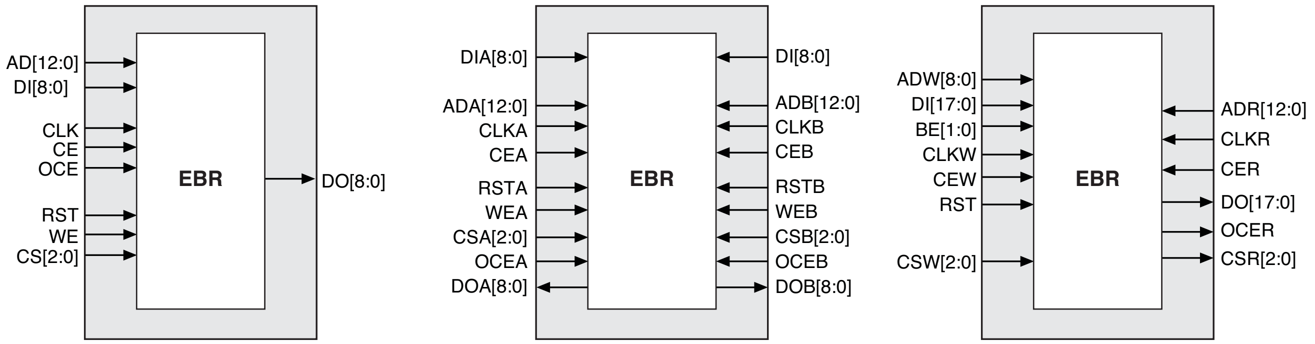
### Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

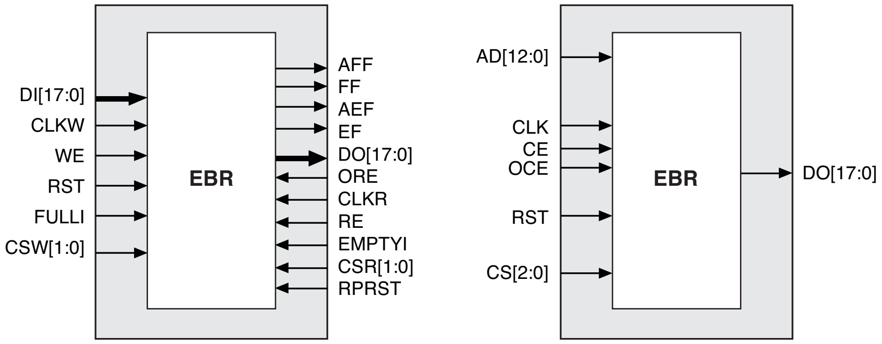
### Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

## Figure 2-8. sysMEM Memory Primitives



**Single-Port RAM** **True Dual Port RAM** **Pseudo Dual Port RAM**



**FIFO RAM** **ROM**

## Table 2-6. EBR Signal Descriptions

| Port Name | Description | Active State |
|---|---|---|
| CLK | Clock | Rising Clock Edge |
| CE | Clock Enable | Active High |
| OCE[1] | Output Clock Enable | Active High |
| RST | Reset | Active High |
| BE[1] | Byte Enable | Active High |
| WE | Write Enable | Active High |
| AD | Address Bus | — |
| DI | Data In | — |
| DO | Data Out | — |
| CS | Chip Select | Active High |
| AFF | FIFO RAM Almost Full Flag | — |
| FF | FIFO RAM Full Flag | — |
| AEF | FIFO RAM Almost Empty Flag | — |
| EF | FIFO RAM Empty Flag | — |
| RPRST | FIFO RAM Read Pointer Reset | — |

1. Optional signals.
2. For dual port EBR primitives a trailing ‘A’ or ‘B’ in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing ‘R’ or ‘W’ in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

*Figure 2-21. I²C Core Block Diagram*

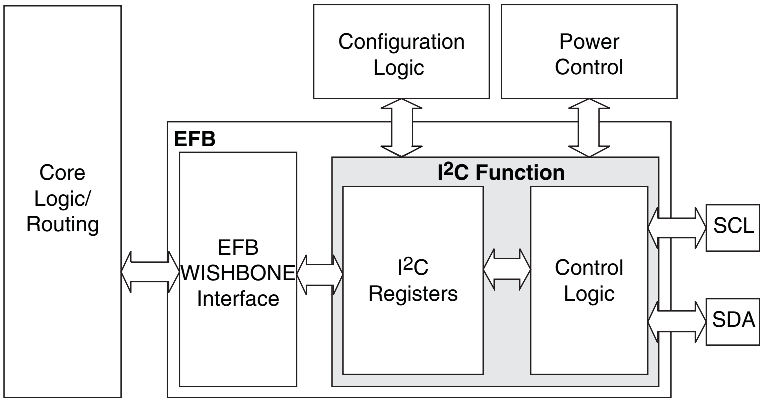


Table 2-15 describes the signals interfacing with the I²C cores.

*Table 2-15. I²C Core Signal Description*

| Signal Name | I/O | Description |
|---|---|---|
| i2c_scl | Bi-directional | Bi-directional clock line of the I²C core. The signal is an output if the I²C core is in master mode. The signal is an input if the I²C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device. |
| i2c_sda | Bi-directional | Bi-directional data line of the I²C core. The signal is an output when data is transmitted from the I²C core. The signal is an input when data is received into the I²C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device. |
| i2c_irqo | Output | Interrupt request output signal of the I²C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I²C register definitions. |
| cfg_wake | Output | Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab. |
| cfg_stdby | Output | Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab. |

## Hardened SPI IP Core

Every MachXO2 device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO2 devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface

There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology (Appendix B)
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices

*Figure 2-22. SPI Core Block Diagram*

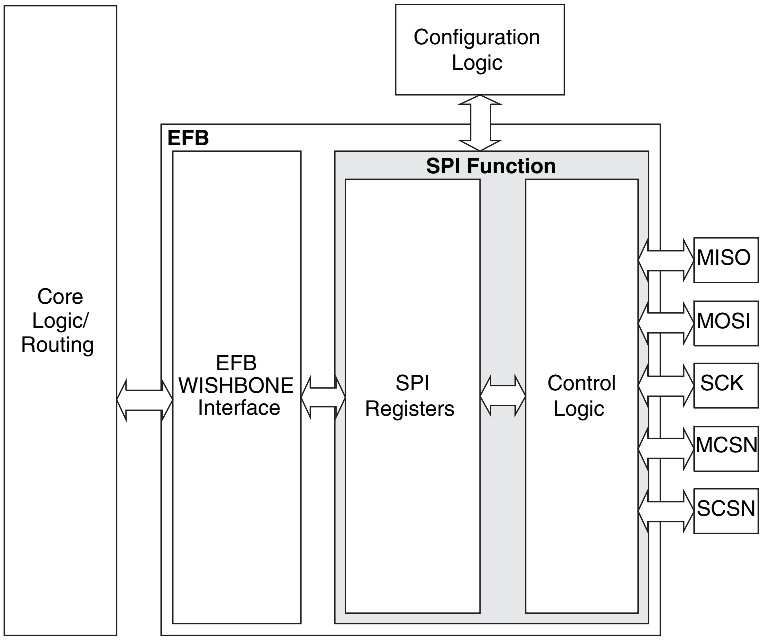


Table 2-16 describes the signals interfacing with the SPI cores.

*Table 2-16. SPI Core Signal Description*

| Signal Name | I/O | Master/Slave | Description |
|---|---|---|---|
| spi_csn[0] | O | Master | SPI master chip-select output |
| spi_csn[1..7] | O | Master | Additional SPI chip-select outputs (total up to eight slaves) |
| spi_scsn | I | Slave | SPI slave chip-select input |
| spi_irq | O | Master/Slave | Interrupt request |
| spi_clk | I/O | Master/Slave | SPI clock. Output in master mode. Input in slave mode. |
| spi_miso | I/O | Master/Slave | SPI data. Input in master mode. Output in slave mode. |
| spi_mosi | I/O | Master/Slave | SPI data. Output in master mode. Input in slave mode. |
| ufm_sn | I | Slave | Configuration Slave Chip Select (active low), dedicated for selecting the User Flash Memory (UFM). |
| cfg_stdby | O | Master/Slave | Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab. |
| cfg_wake | O | Master/Slave | Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab. |

## BLVDS

The MachXO2 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

*Figure 3-2. BLVDS Multi-point Output Example*

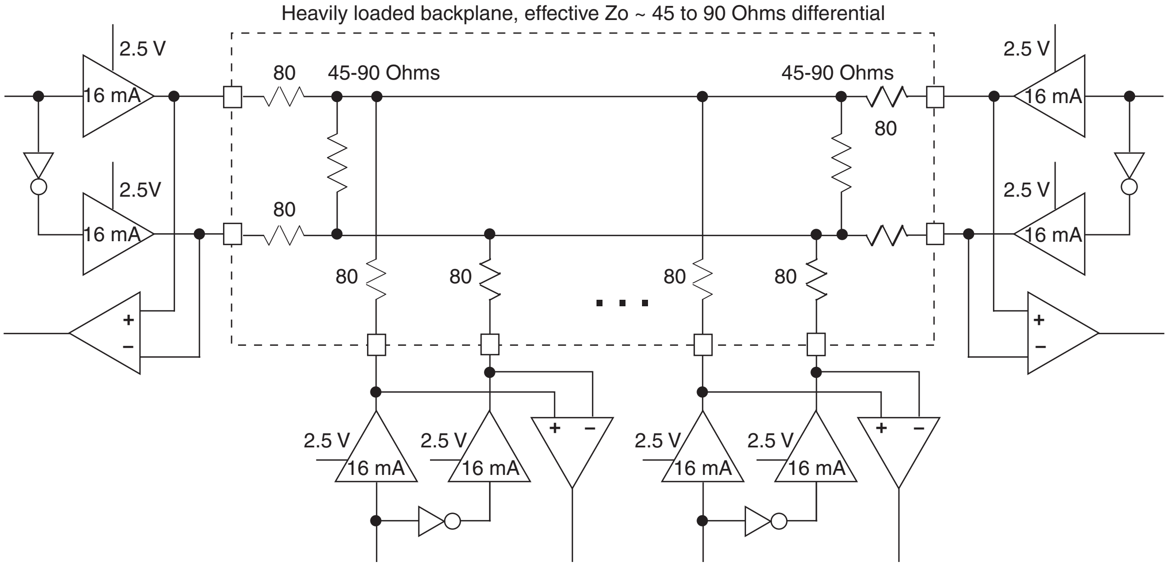


*Table 3-2. BLVDS DC Conditions*[1]

**Over Recommended Operating Conditions**

| Symbol | Description | Nominal | | Units |
|---|---|---|---|---|
| | | Zo = 45 | Zo = 90 | |
| $Z_{OUT}$ | Output impedance | 20 | 20 | Ohms |
| $R_S$ | Driver series resistance | 80 | 80 | Ohms |
| $R_{TLEFT}$ | Left end termination | 45 | 90 | Ohms |
| $R_{TRIGHT}$ | Right end termination | 45 | 90 | Ohms |
| $V_{OH}$ | Output high voltage | 1.376 | 1.480 | V |
| $V_{OL}$ | Output low voltage | 1.124 | 1.020 | V |
| $V_{OD}$ | Output differential voltage | 0.253 | 0.459 | V |
| $V_{CM}$ | Output common mode voltage | 1.250 | 1.250 | V |
| $I_{DC}$ | DC output current | 11.236 | 10.204 | mA |

1. For input buffer, see LVDS table.

| Parameter | Description | Device | –6 | | –5 | | –4 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{HPLL}$ | Clock to Data Hold – PIO Input Register | MachXO2-1200HC-HE | 0.41 | — | 0.48 | — | 0.55 | — | ns |
| | | MachXO2-2000HC-HE | 0.42 | — | 0.49 | — | 0.56 | — | ns |
| | | MachXO2-4000HC-HE | 0.43 | — | 0.50 | — | 0.58 | — | ns |
| | | MachXO2-7000HC-HE | 0.46 | — | 0.54 | — | 0.62 | — | ns |
| $t_{SU\_DELPLL}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-1200HC-HE | 2.88 | — | 3.19 | — | 3.72 | — | ns |
| | | MachXO2-2000HC-HE | 2.87 | — | 3.18 | — | 3.70 | — | ns |
| | | MachXO2-4000HC-HE | 2.96 | — | 3.28 | — | 3.81 | — | ns |
| | | MachXO2-7000HC-HE | 3.05 | — | 3.35 | — | 3.87 | — | ns |
| $t_{H\_DELPLL}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-1200HC-HE | –0.83 | — | –0.83 | — | –0.83 | — | ns |
| | | MachXO2-2000HC-HE | –0.83 | — | –0.83 | — | –0.83 | — | ns |
| | | MachXO2-4000HC-HE | –0.87 | — | –0.87 | — | –0.87 | — | ns |
| | | MachXO2-7000HC-HE | –0.91 | — | –0.91 | — | –0.91 | — | ns |
| **Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 12]** | | | | | | | | | |
| $t_{DVA}$ | Input Data Valid After CLK | All MachXO2 devices, all sides | — | 0.317 | — | 0.344 | — | 0.368 | UI |
| $t_{DVE}$ | Input Data Hold After CLK | | 0.742 | — | 0.702 | — | 0.668 | — | UI |
| $f_{DATA}$ | DDRX1 Input Data Speed | | — | 300 | — | 250 | — | 208 | Mbps |
| $f_{DDRX1}$ | DDRX1 SCLK Frequency | | — | 150 | — | 125 | — | 104 | MHz |
| **Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 12]** | | | | | | | | | |
| $t_{SU}$ | Input Data Setup Before CLK | All MachXO2 devices, all sides | 0.566 | — | 0.560 | — | 0.538 | — | ns |
| $t_{HO}$ | Input Data Hold After CLK | | 0.778 | — | 0.879 | — | 1.090 | — | ns |
| $f_{DATA}$ | DDRX1 Input Data Speed | | — | 300 | — | 250 | — | 208 | Mbps |
| $f_{DDRX1}$ | DDRX1 SCLK Frequency | | — | 150 | — | 125 | — | 104 | MHz |
| **Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 12]** | | | | | | | | | |
| $t_{DVA}$ | Input Data Valid After CLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11] | — | 0.316 | — | 0.342 | — | 0.364 | UI |
| $t_{DVE}$ | Input Data Hold After CLK | | 0.710 | — | 0.675 | — | 0.679 | — | UI |
| $f_{DATA}$ | DDRX2 Serial Input Data Speed | | — | 664 | — | 554 | — | 462 | Mbps |
| $f_{DDRX2}$ | DDRX2 ECLK Frequency | | — | 332 | — | 277 | — | 231 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 166 | — | 139 | — | 116 | MHz |
| **Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 12]** | | | | | | | | | |
| $t_{SU}$ | Input Data Setup Before CLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11] | 0.233 | — | 0.219 | — | 0.198 | — | ns |
| $t_{HO}$ | Input Data Hold After CLK | | 0.287 | — | 0.287 | — | 0.344 | — | ns |
| $f_{DATA}$ | DDRX2 Serial Input Data Speed | | — | 664 | — | 554 | — | 462 | Mbps |
| $f_{DDRX2}$ | DDRX2 ECLK Frequency | | — | 332 | — | 277 | — | 231 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 166 | — | 139 | — | 116 | MHz |

| Parameter | Description | Device | –6 | | –5 | | –4 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered**[9, 12] | | | | | | | | | |
| $t_{DVB}$ | Output Data Valid Before CLK Output | MachXO2-640U, MachXO2-1200/U and larger devices, top side only. | 0.535 | — | 0.670 | — | 0.830 | — | ns |
| $t_{DVA}$ | Output Data Valid After CLK Output | | 0.535 | — | 0.670 | — | 0.830 | — | ns |
| $f_{DATA}$ | DDRX2 Serial Output Data Speed | | — | 664 | — | 554 | — | 462 | Mbps |
| $f_{DDRX2}$ | DDRX2 ECLK Frequency (minimum limited by PLL) | | — | 332 | — | 277 | — | 231 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 166 | — | 139 | — | 116 | MHz |
| **Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned**[9, 12] | | | | | | | | | |
| $t_{DIA}$ | Output Data Invalid After CLK Output | MachXO2-640U, MachXO2-1200/U and larger devices, top side only. | — | 0.200 | — | 0.215 | — | 0.230 | ns |
| $t_{DIB}$ | Output Data Invalid Before CLK Output | | — | 0.200 | — | 0.215 | — | 0.230 | ns |
| $f_{DATA}$ | DDRX4 Serial Output Data Speed | | — | 756 | — | 630 | — | 524 | Mbps |
| $f_{DDRX4}$ | DDRX4 ECLK Frequency | | — | 378 | — | 315 | — | 262 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 95 | — | 79 | — | 66 | MHz |
| **Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered**[9, 12] | | | | | | | | | |
| $t_{DVB}$ | Output Data Valid Before CLK Output | MachXO2-640U, MachXO2-1200/U and larger devices, top side only. | 0.455 | — | 0.570 | — | 0.710 | — | ns |
| $t_{DVA}$ | Output Data Valid After CLK Output | | 0.455 | — | 0.570 | — | 0.710 | — | ns |
| $f_{DATA}$ | DDRX4 Serial Output Data Speed | | — | 756 | — | 630 | — | 524 | Mbps |
| $f_{DDRX4}$ | DDRX4 ECLK Frequency (minimum limited by PLL) | | — | 378 | — | 315 | — | 262 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 95 | — | 79 | — | 66 | MHz |
| **7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1**[9, 12] | | | | | | | | | |
| $t_{DIB}$ | Output Data Invalid Before CLK Output | MachXO2-640U, MachXO2-1200/U and larger devices, top side only. | — | 0.160 | — | 0.180 | — | 0.200 | ns |
| $t_{DIA}$ | Output Data Invalid After CLK Output | | — | 0.160 | — | 0.180 | — | 0.200 | ns |
| $f_{DATA}$ | DDR71 Serial Output Data Speed | | — | 756 | — | 630 | — | 524 | Mbps |
| $f_{DDR71}$ | DDR71 ECLK Frequency | | — | 378 | — | 315 | — | 262 | MHz |
| $f_{CLKOUT}$ | 7:1 Output Clock Frequency (SCLK) (minimum limited by PLL) | | — | 108 | — | 90 | — | 75 | MHz |

| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **LPDDR**[9, 12] | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only.[13] | — | 0.349 | — | 0.381 | — | 0.396 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.665 | — | 0.630 | — | 0.613 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM LPDDR Serial Data Speed | | — | 120 | — | 110 | — | 96 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 60 | — | 55 | — | 48 | MHz |
| $f_{LPDDR}$ | LPDDR Data Transfer Rate | | 0 | 120 | 0 | 110 | 0 | 96 | Mbps |
| **DDR**[9, 12] | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only.[13] | — | 0.347 | — | 0.374 | — | 0.393 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.665 | — | 0.637 | — | 0.616 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM DDR Serial Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 58 | — | 49 | MHz |
| $f_{MEM\_DDR}$ | MEM DDR Data Transfer Rate | | N/A | 140 | N/A | 116 | N/A | 98 | Mbps |
| **DDR2**[9, 12] | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only.[13] | — | 0.372 | — | 0.394 | — | 0.410 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.690 | — | 0.658 | — | 0.618 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM DDR Serial Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 58 | — | 49 | MHz |
| $f_{MEM\_DDR2}$ | MEM DDR2 Data Transfer Rate | | N/A | 140 | N/A | 116 | N/A | 98 | Mbps |

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\text{ ns})/2$.
7. The $t_{SU\_DEL}$ and $t_{H\_DEL}$ values use the SCLK_ZERHOLD default step size. Each step is 167 ps (–3), 182 ps (–2), 195 ps (–1).
8. This number for general purpose usage. Duty cycle tolerance is +/–10%.
9. Duty cycle is +/– 5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

*Figure 3-5. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms*

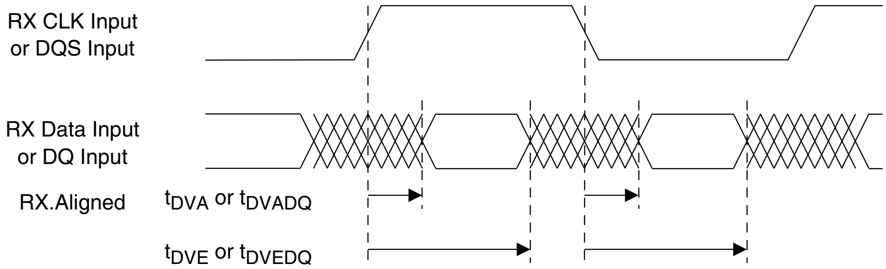


*Figure 3-6. Receiver RX.CLK.Centered Waveforms*

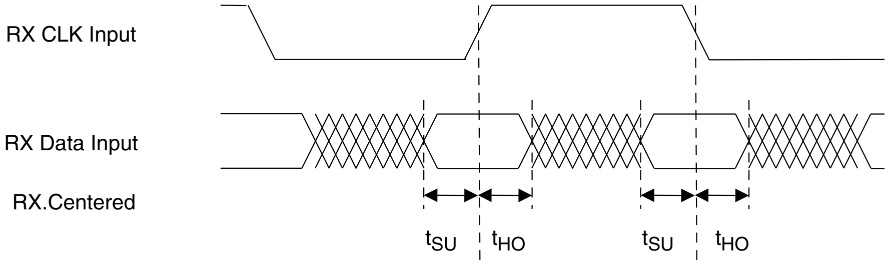


*Figure 3-7. Transmitter TX.CLK.Aligned Waveforms*

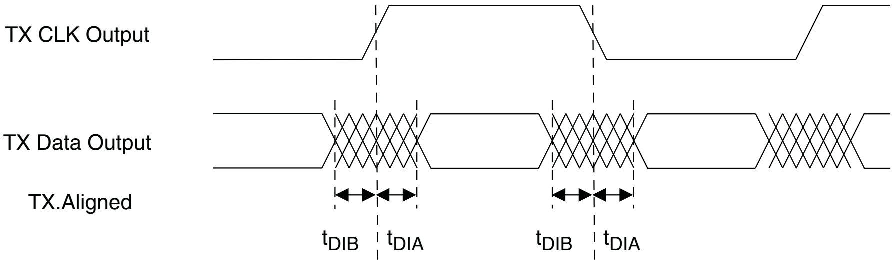
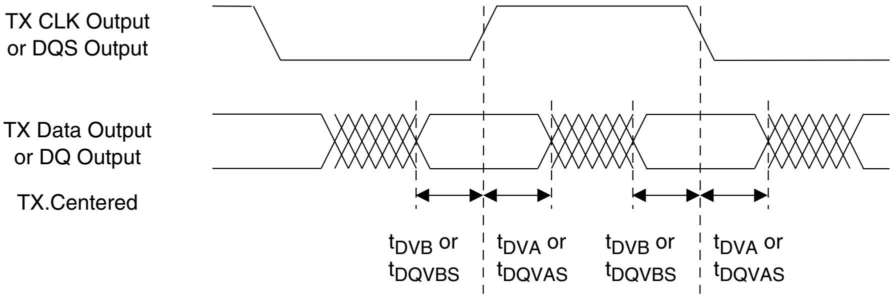


*Figure 3-8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms*



## sysCLOCK PLL Timing

**Over Recommended Operating Conditions**

| Parameter | Descriptions | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $f_{IN}$ | Input Clock Frequency (CLKI, CLKFB) | | 7 | 400 | MHz |
| $f_{OUT}$ | Output Clock Frequency (CLKOP, CLKOS, CLKOS2) | | 1.5625 | 400 | MHz |
| $f_{OUT2}$ | Output Frequency (CLKOS3 cascaded from CLKOS2) | | 0.0122 | 400 | MHz |
| $f_{VCO}$ | PLL VCO Frequency | | 200 | 800 | MHz |
| $f_{PFD}$ | Phase Detector Input Frequency | | 7 | 400 | MHz |
| **AC Characteristics** | | | | | |
| $t_{DT}$ | Output Clock Duty Cycle | Without duty trim selected[3] | 45 | 55 | % |
| $t_{DT\_TRIM}$[7] | Edge Duty Trim Accuracy | | –75 | 75 | % |
| $t_{PH}$[4] | Output Phase Accuracy | | –6 | 6 | % |
| $t_{OPJIT}$[1, 8] | Output Clock Period Jitter | $f_{OUT}$ > 100 MHz | — | 150 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.007 | UIPP |
| | Output Clock Cycle-to-cycle Jitter | $f_{OUT}$ > 100 MHz | — | 180 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.009 | UIPP |
| | Output Clock Phase Jitter | $f_{PFD}$ > 100 MHz | — | 160 | ps p-p |
| | | $f_{PFD}$ < 100 MHz | — | 0.011 | UIPP |
| | Output Clock Period Jitter (Fractional-N) | $f_{OUT}$ > 100 MHz | — | 230 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.12 | UIPP |
| | Output Clock Cycle-to-cycle Jitter (Fractional-N) | $f_{OUT}$ > 100 MHz | — | 230 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.12 | UIPP |
| $t_{SPO}$ | Static Phase Offset | Divider ratio = integer | –120 | 120 | ps |
| $t_W$ | Output Clock Pulse Width | At 90% or 10%[3] | 0.9 | — | ns |
| $t_{LOCK}$[2, 5] | PLL Lock-in Time | | — | 15 | ms |
| $t_{UNLOCK}$ | PLL Unlock Time | | — | 50 | ns |
| $t_{IPJIT}$[6] | Input Clock Period Jitter | $f_{PFD} \geq 20$ MHz | — | 1,000 | ps p-p |
| | | $f_{PFD}$ < 20 MHz | — | 0.02 | UIPP |
| $t_{HI}$ | Input Clock High Time | 90% to 90% | 0.5 | — | ns |
| $t_{LO}$ | Input Clock Low Time | 10% to 10% | 0.5 | — | ns |
| $t_{STABLE}$[5] | STANDBY High to PLL Stable | | — | 15 | ms |
| $t_{RST}$ | RST/RESETM Pulse Width | | 1 | — | ns |
| $t_{RSTREC}$ | RST Recovery Time | | 1 | — | ns |
| $t_{RST\_DIV}$ | RESETC/D Pulse Width | | 10 | — | ns |
| $t_{RSTREC\_DIV}$ | RESETC/D Recovery Time | | 1 | — | ns |
| $t_{ROTATE\text{-}SETUP}$ | PHASESTEP Setup Time | | 10 | — | ns |

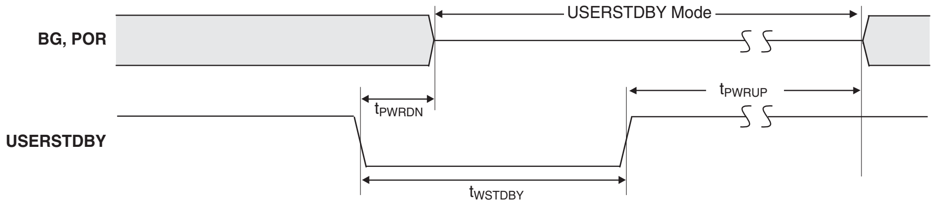
## MachXO2 Oscillator Output Frequency

| Symbol | Parameter | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|
| $f_{MAX}$ | Oscillator Output Frequency (Commercial Grade Devices, 0 to 85°C) | 125.685 | 133 | 140.315 | MHz |
| | Oscillator Output Frequency (Industrial Grade Devices, –40 °C to 100 °C) | 124.355 | 133 | 141.645 | MHz |
| $t_{DT}$ | Output Clock Duty Cycle | 43 | 50 | 57 | % |
| $t_{OPJIT}$[1] | Output Clock Period Jitter | 0.01 | 0.012 | 0.02 | UIPP |
| $t_{STABLEOSC}$ | STDBY Low to Oscillator Stable | 0.01 | 0.05 | 0.1 | µs |

1. Output Clock Period Jitter specified at 133 MHz. The values for lower frequencies will be smaller UIPP. The typical value for 133 MHz is 95 ps and for 2.08 MHz the typical value is 1.54 ns.

## MachXO2 Standby Mode Timing – HC/HE Devices

| Symbol | Parameter | Device | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PWRDN}$ | USERSTDBY High to Stop | All | — | — | 9 | ns |
| $t_{PWRUP}$ | USERSTDBY Low to Power Up | LCMXO2-256 | | — | | µs |
| | | LCMXO2-640 | | — | | µs |
| | | LCMXO2-640U | | — | | µs |
| | | LCMXO2-1200 | 20 | — | 50 | µs |
| | | LCMXO2-1200U | | — | | µs |
| | | LCMXO2-2000 | | — | | µs |
| | | LCMXO2-2000U | | — | | µs |
| | | LCMXO2-4000 | | — | | µs |
| | | LCMXO2-7000 | | — | | µs |
| $t_{WSTDBY}$ | USERSTDBY Pulse Width | All | 18 | — | — | ns |



## MachXO2 Standby Mode Timing – ZE Devices

| Symbol | Parameter | Device | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PWRDN}$ | USERSTDBY High to Stop | All | — | — | 13 | ns |
| $t_{PWRUP}$ | USERSTDBY Low to Power Up | LCMXO2-256 | | — | | µs |
| | | LCMXO2-640 | | — | | µs |
| | | LCMXO2-1200 | 20 | — | 50 | µs |
| | | LCMXO2-2000 | | — | | µs |
| | | LCMXO2-4000 | | — | | µs |
| | | LCMXO2-7000 | | — | | µs |
| $t_{WSTDBY}$ | USERSTDBY Pulse Width | All | 19 | — | — | ns |
| $t_{BNDGAPSTBL}$ | USERSTDBY High to Bandgap Stable | All | — | — | 15 | ns |

## For Further Information

For further information regarding logic signal connections for various packages please refer to the MachXO2 Device Pinout Files.

## Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Users must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

### For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1198, Power Estimation and Management for MachXO2 Devices
- The Power Calculator tool is included with the Lattice design tools, or as a standalone download from www.latticesemi.com/software

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-1200HC-4SG32C | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200HC-5SG32C | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200HC-6SG32C | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200HC-4TG100C | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200HC-5TG100C | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200HC-6TG100C | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200HC-4MG132C | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200HC-5MG132C | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200HC-6MG132C | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200HC-4TG144C | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200HC-5TG144C | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200HC-6TG144C | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-1200UHC-4FTG256C | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-1200UHC-5FTG256C | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-1200UHC-6FTG256C | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000HC-4TG100C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000HC-5TG100C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000HC-6TG100C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000HC-4MG132C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000HC-5MG132C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000HC-6MG132C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000HC-4TG144C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000HC-5TG144C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000HC-6TG144C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000HC-4BG256C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000HC-5BG256C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000HC-6BG256C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000HC-4FTG256C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000HC-5FTG256C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000HC-6FTG256C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | COM |

## Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-256ZE-1SG32I | 256 | 1.2 V | –1 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256ZE-2SG32I | 256 | 1.2 V | –2 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256ZE-3SG32I | 256 | 1.2 V | –3 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256ZE-1UMG64I | 256 | 1.2 V | –1 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256ZE-2UMG64I | 256 | 1.2 V | –2 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256ZE-3UMG64I | 256 | 1.2 V | –3 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256ZE-1TG100I | 256 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256ZE-2TG100I | 256 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256ZE-3TG100I | 256 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256ZE-1MG132I | 256 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256ZE-2MG132I | 256 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256ZE-3MG132I | 256 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640ZE-1TG100I | 640 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640ZE-2TG100I | 640 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640ZE-3TG100I | 640 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640ZE-1MG132I | 640 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640ZE-2MG132I | 640 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640ZE-3MG132I | 640 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-1200ZE-1UWG25ITR[1] | 1280 | 1.2 V | –1 | Halogen-Free WLCSP | 25 | IND |
| LCMXO2-1200ZE-1UWG25ITR50[3] | 1280 | 1.2 V | –1 | Halogen-Free WLCSP | 25 | IND |
| LCMXO2-1200ZE-1UWG25ITR1K[2] | 1280 | 1.2 V | –1 | Halogen-Free WLCSP | 25 | IND |
| LCMXO2-1200ZE-1SG32I | 1280 | 1.2 V | –1 | Halogen-Free QFN | 32 | IND |
| LCMXO2-1200ZE-2SG32I | 1280 | 1.2 V | –2 | Halogen-Free QFN | 32 | IND |
| LCMXO2-1200ZE-3SG32I | 1280 | 1.2 V | –3 | Halogen-Free QFN | 32 | IND |
| LCMXO2-1200ZE-1TG100I | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-2TG100I | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-3TG100I | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-1MG132I | 1280 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-2MG132I | 1280 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-3MG132I | 1280 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-1TG144I | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200ZE-2TG144I | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200ZE-3TG144I | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 144 | IND |

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

## High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-256HC-4SG32I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256HC-5SG32I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256HC-6SG32I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256HC-4SG48I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 48 | IND |
| LCMXO2-256HC-5SG48I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 48 | IND |
| LCMXO2-256HC-6SG48I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 48 | IND |
| LCMXO2-256HC-4UMG64I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256HC-5UMG64I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256HC-6UMG64I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256HC-4TG100I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256HC-5TG100I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256HC-6TG100I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256HC-4MG132I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256HC-5MG132I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256HC-6MG132I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640HC-4SG48I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 48 | IND |
| LCMXO2-640HC-5SG48I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 48 | IND |
| LCMXO2-640HC-6SG48I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 48 | IND |
| LCMXO2-640HC-4TG100I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640HC-5TG100I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640HC-6TG100I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640HC-4MG132I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640HC-5MG132I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640HC-6MG132I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640UHC-4TG144I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-640UHC-5TG144I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-640UHC-6TG144I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000HC-4QN84I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000HC-5QN84I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000HC-6QN84I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000HC-4TG144I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HC-5TG144I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HC-6TG144I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HC-4MG132I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HC-5MG132I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HC-6MG132I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HC-4BG256I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HC-5BG256I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HC-6BG256I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HC-4FTG256I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HC-5FTG256I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HC-6FTG256I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HC-4BG332I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HC-5BG332I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HC-6BG332I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HC-4FG484I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HC-5FG484I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HC-6FG484I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000HC-4TG144I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HC-5TG144I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HC-6TG144I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HC-4BG256I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HC-5BG256I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HC-6BG256I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HC-4FTG256I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HC-5FTG256I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HC-6FTG256I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HC-4BG332I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HC-5BG332I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HC-6BG332I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HC-4FG400I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 400 | IND |
| LCMXO2-7000HC-5FG400I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 400 | IND |
| LCMXO2-7000HC-6FG400I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 400 | IND |
| LCMXO2-7000HC-4FG484I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HC-5FG484I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HC-6FG484I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | IND |

# MachXO2 Family Data Sheet Supplemental Information

**April 2012** **Data Sheet DS1035**

## For Further Information

A variety of technical notes for the MachXO2 family are available on the Lattice web site.

- TN1198, Power Estimation and Management for MachXO2 Devices
- TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide
- TN1201, Memory Usage Guide for MachXO2 Devices
- TN1202, MachXO2 sysIO Usage Guide
- TN1203, Implementing High-Speed Interfaces with MachXO2 Devices
- TN1204, MachXO2 Programming and Configuration Usage Guide
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices
- TN1206, MachXO2 SRAM CRC Error Detection Usage Guide
- TN1207, Using TraceID in MachXO2 Devices
- TN1074, PCB Layout Recommendations for BGA Packages
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices
- AN8066, Boundary Scan Testability with Lattice sysIO Capability

- MachXO2 Device Pinout Files
- Thermal Management document
- Lattice design tools

For further information on interface standards, refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, LVDS, DDR, DDR2, LPDDR): www.jedec.org
- PCI: www.pcisig.com

| Date | Version | Section | Change Summary |
|---|---|---|---|
| January 2013 | 02.0 | Introduction | Updated the total number IOs to include JTAGENB. |
| | | Architecture | Supported Output Standards table – Added 3.3 $V_{CCIO}$ (Typ.) to LVDS row. |
| | | | Changed SRAM CRC Error Detection to Soft Error Detection. |
| | | DC and Switching Characteristics | Power Supply Ramp Rates table – Updated Units column for $t_{RAMP}$ symbol. |
| | | | Added new Maximum sysIO Buffer Performance table. |
| | | | sysCLOCK PLL Timing table – Updated Min. column values for $f_{IN}$, $f_{OUT}$, $f_{OUT2}$ and $f_{PFD}$ parameters. Added $t_{SPO}$ parameter. Updated footnote 6. |
| | | | MachXO2 Oscillator Output Frequency table – Updated symbol name for $t_{STABLEOSC}$. |
| | | | DC Electrical Characteristics table – Updated conditions for $I_{IL}$, $I_{IH}$ symbols. |
| | | | Corrected parameters tDQVBS and tDQVAS |
| | | | Corrected MachXO2 ZE parameters tDVADQ and tDVEDQ |
| | | Pinout Information | Included the MachXO2-4000HE 184 csBGA package. |
| | | Ordering Information | Updated part number. |
| April 2012 | 01.9 | Architecture | Removed references to TN1200. |
| | | Ordering Information | Updated the Device Status portion of the MachXO2 Part Number Description to include the 50 parts per reel for the WLCSP package. |
| | | | Added new part number and footnote 2 for LCMXO2-1200ZE-1UWG25ITR50. |
| | | | Updated footnote 1 for LCMXO2-1200ZE-1UWG25ITR. |
| | | Supplemental Information | Removed references to TN1200. |
| March 2012 | 01.8 | Introduction | Added 32 QFN packaging information to Features bullets and MachXO2 Family Selection Guide table. |
| | | DC and Switching Characteristics | Changed ‘STANDBY’ to ‘USERSTDBY’ in Standby Mode timing diagram. |
| | | Pinout Information | Removed footnote from Pin Information Summary tables. |
| | | | Added 32 QFN package to Pin Information Summary table. |
| | | Ordering Information | Updated Part Number Description and Ordering Information tables for 32 QFN package. |
| | | | Updated topside mark diagram in the Ordering Information section. |