E. K Hattice Semiconductor Corporation - LCMX02-2000HE-5TG100I Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	264
Number of Logic Elements/Cells	2112
Total RAM Bits	75776
Number of I/O	79
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-2000he-5tg100i

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The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag "hard" control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysl/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2-640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO2 devices provide commonly used hardened functions such as SPI controller, I²C controller and timer/ counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I²C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

PFU Blocks

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.







Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

The tri-state register blocks on the right edge contain an additional register for DDR memory operation. In DDR memory mode, the register TS input is fed into another register that is clocked using the DQSW90 signal. The output of this register is used as a tri-state control.

Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

Table 2-9.	Input	Gearbox	Sianal List
14010 2 01	mpat	acaison	orginal Eloc

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3



Figure 2-18. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 Banks



Figure 2-19. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks





For more details on these embedded functions, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

User Flash Memory (UFM)

MachXO2-640/U and higher density devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I²C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

Standby Mode and Power Saving Options

MachXO2 devices are available in three options for maximum flexibility: ZE, HC and HE devices. The ZE devices have ultra low static and dynamic power consumption. These devices use a 1.2 V core voltage that further reduces power consumption. The HC and HE devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the HE devices operate at 1.2 V V_{CC}.

MachXO2 devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO2 devices support an ultra low power Stand-by mode. While most of these features are available in all three device types, these features are mainly intended for use with MachXO2 ZE devices to manage power consumption.

In the stand-by mode the MachXO2 devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I²C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned "off" or go into a low power consumption state to save power when the device enters this state. Note that the MachXO2 devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.



Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe V_{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1198, Power Estimation and Management for MachXO2 Devices.

Power On Reset

MachXO2 devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the V_{PORUP} level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices), V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators (HC devices), V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time (t_{REFRESH}) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tristate. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min) they should not shut down the bandgap or POR circuit.



sysIO Recommended Operating Conditions

		V _{CCIO} (V)			V _{REF} (V)	
Standard	Min.	Тур.	Max.	Min.	Тур.	Max.
LVCMOS 3.3	3.135	3.3	3.6	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.6	—	—	—
PCI ³	3.135	3.3	3.6	—	—	—
SSTL25	2.375	2.5	2.625	1.15	1.25	1.35
SSTL18	1.71	1.8	1.89	0.833	0.9	0.969
HSTL18	1.71	1.8	1.89	0.816	0.9	1.08
LVCMOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVCMOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVCMOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVCMOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVCMOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVCMOS12R334	3.135	3.3	3.6	0.45	0.6	0.75
LVCMOS12R254	2.375	2.5	2.625	0.45	0.6	0.75
LVCMOS10R334	3.135	3.3	3.6	0.35	0.5	0.65
LVCMOS10R254	2.375	2.5	2.625	0.35	0.5	0.65
LVDS25 ^{1, 2}	2.375	2.5	2.625	—	—	—
LVDS33 ^{1, 2}	3.135	3.3	3.6	—	—	—
LVPECL ¹	3.135	3.3	3.6	—	—	—
BLVDS ¹	2.375	2.5	2.625	—	—	—
RSDS ¹	2.375	2.5	2.625	—	—	—
SSTL18D	1.71	1.8	1.89	—	—	—
SSTL25D	2.375	2.5	2.625	—	—	—
HSTL18D	1.71	1.8	1.89	—	—	—

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.

2. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.

3. Input on the bottom bank of the MachXO2-640U, MachXO2-1200/U and larger devices only.

4. Supported only for inputs and BIDIs for all ZE devices, and -6 speed grade for HE and HC devices.



			-6		-5		-4		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Generic DDR	X2 Outputs with Clock and Data	Centered at Pin Using P	CLK Pin	for Cloc	k Input –	GDDRX	2_TX.EC	CLK.Cen	tered ^{9, 12}
t _{DVB}	Output Data Valid Before CLK Output		0.535	_	0.670	_	0.830	_	ns
t _{DVA}	Output Data Valid After CLK Output	MachXO2-640U,	0.535	_	0.670		0.830	_	ns
f _{DATA}	DDRX2 Serial Output Data Speed	MacnXO2-1200/U and larger devices, top side	_	664	_	554	_	462	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		_	332	_	277	_	231	MHz
f _{SCLK}	SCLK Frequency			166		139	—	116	MHz
Generic DDF	X4 Outputs with Clock and Data	a Aligned at Pin Using P	CLK Pin	for Cloc	k Input -	- GDDR	X4_TX.E	CLK.Ali	gned ^{9, 12}
t _{DIA}	Output Data Invalid After CLK Output			0.200		0.215	_	0.230	ns
t _{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and		0.200		0.215	_	0.230	ns
f _{DATA}	DDRX4 Serial Output Data Speed	larger devices, top side only.	_	756	_	630	_	524	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency			378		315	—	262	MHz
f _{SCLK}	SCLK Frequency		_	95	_	79	—	66	MHz
Generic DDF	X4 Outputs with Clock and Data	Centered at Pin Using P	CLK Pin	for Cloc	k Input –	GDDRX	4_TX.EC	CLK.Cen	tered ^{9, 12}
t _{DVB}	Output Data Valid Before CLK Output		0.455	_	0.570		0.710	_	ns
t _{DVA}	Output Data Valid After CLK Output	MachXO2-640U,	0.455	_	0.570	_	0.710	_	ns
f _{DATA}	DDRX4 Serial Output Data Speed	larger devices, top side		756	_	630	_	524	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)			378		315	_	262	MHz
f _{SCLK}	SCLK Frequency		_	95	_	79	—	66	MHz
7:1 LVDS Ou	utputs - GDDR71_TX.ECLK.7:1	1 ^{9, 12}							
t _{DIB}	Output Data Invalid Before CLK Output		_	0.160	_	0.180	_	0.200	ns
t _{DIA}	Output Data Invalid After CLK Output	MachXO2-640U.		0.160		0.180	_	0.200	ns
f _{DATA}	DDR71 Serial Output Data Speed	MachXO2-1200/U and larger devices, top side	_	756	_	630	_	524	Mbps
f _{DDR71}	DDR71 ECLK Frequency	only.		378	_	315	—	262	MHz
fclkout	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		_	108	_	90	_	75	MHz



MachXO2 External Switching Characteristics – ZE Devices^{1, 2, 3, 4, 5, 6, 7}

			-3		-2		-1		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Clocks			1						
Primary Cloo	cks								
f _{MAX_PRI} ⁸	Frequency for Primary Clock Tree	All MachXO2 devices	_	150	_	125	_	104	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	1.00	_	1.20	_	1.40	_	ns
		MachXO2-256ZE	_	1250	—	1272		1296	ps
		MachXO2-640ZE		1161		1183		1206	ps
	Primary Clock Skew Within a	MachXO2-1200ZE	_	1213		1267		1322	ps
^t SKEW_PRI	Device	MachXO2-2000ZE		1204		1250		1296	ps
		MachXO2-4000ZE		1195		1233		1269	ps
		MachXO2-7000ZE		1243		1268		1296	ps
Edge Clock									
f _{MAX_EDGE} ⁸	Frequency for Edge Clock	MachXO2-1200 and larger devices	_	210	_	175	_	146	MHz
Pin-LUT-Pin	Propagation Delay	-	1		1			1	
t _{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	_	9.35	_	9.78	_	10.21	ns
General I/O	Pin Parameters (Using Primary	Clock without PLL)	I	I	I	I	I		
		MachXO2-256ZE		10.46	—	10.86	—	11.25	ns
		MachXO2-640ZE	_	10.52	—	10.92		11.32	ns
	Clock to Output – PIO Output	MachXO2-1200ZE	_	11.24		11.68		12.12	ns
^t CO	Register	MachXO2-2000ZE	_	11.27		11.71		12.16	ns
		MachXO2-4000ZE	_	11.28		11.78		12.28	ns
		MachXO2-7000ZE		11.22		11.76		12.30	ns
		MachXO2-256ZE	-0.21		-0.21		-0.21		ns
		MachXO2-640ZE	-0.22		-0.22		-0.22	—	ns
	Clock to Data Setup – PIO	MachXO2-1200ZE	-0.25	—	-0.25		-0.25	_	ns
t _{SU}	Input Register	MachXO2-2000ZE	-0.27		-0.27		-0.27	_	ns
		MachXO2-4000ZE	-0.31		-0.31		-0.31	_	ns
		MachXO2-7000ZE	-0.33		-0.33		-0.33	_	ns
		MachXO2-256ZE	3.96	—	4.25	—	4.65	—	ns
		MachXO2-640ZE	4.01		4.31		4.71	_	ns
+	Clock to Data Hold – PIO Input	MachXO2-1200ZE	3.95		4.29		4.73	—	ns
Ч	Register	MachXO2-2000ZE	3.94		4.29		4.74	_	ns
		MachXO2-4000ZE	3.96		4.36		4.87	_	ns
		MachXO2-7000ZE	3.93	_	4.37	_	4.91		ns

Over Recommended Operating Conditions



			-3		-	-2	-1		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
		MachXO2-1200ZE	0.66	—	0.68		0.80		ns
	Clock to Data Hold – PIO Input	MachXO2-2000ZE	0.68	—	0.70		0.83		ns
^I HPLL	Register	MachXO2-4000ZE	0.68	—	0.71		0.84		ns
		MachXO2-7000ZE	0.73	—	0.74	—	0.87	—	ns
		MachXO2-1200ZE	5.14	—	5.69	—	6.20	—	ns
	Clock to Data Setup – PIO	MachXO2-2000ZE	5.11	—	5.67	—	6.17	—	ns
^I SU_DELPLL	Delav	MachXO2-4000ZE	5.27	—	5.84		6.35	—	ns
		MachXO2-7000ZE	5.15	—	5.71	—	6.23	—	ns
		MachXO2-1200ZE	-1.36	—	-1.36	—	-1.36	—	ns
	Clock to Data Hold – PIO Input	MachXO2-2000ZE	-1.35	—	-1.35		-1.35	—	ns
^I H_DELPLL	Register with Input Data Delay	MachXO2-4000ZE	-1.43	—	-1.43	—	-1.43	—	ns
		MachXO2-7000ZE	-1.41	—	-1.41	—	-1.41	—	ns
Generic DDR	X1 Inputs with Clock and Data A	ligned at Pin Using PO	LK Pin	for Cloc	k Input -	GDDR	(1_RX.S	CLK.Ali	gned ^{9, 12}
t _{DVA}	Input Data Valid After CLK		_	0.382		0.401		0.417	UI
t _{DVE}	Input Data Hold After CLK	All MachXO2	0.670	—	0.684		0.693	—	UI
f _{DATA}	DDRX1 Input Data Speed	devices, all sides	_	140		116	—	98	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency		_	70		58	—	49	MHz
Generic DDR	X1 Inputs with Clock and Data Ce	entered at Pin Using PC	LK Pin f	for Clock	Input –	GDDRX	1_RX.SC	LK.Cen	tered ^{9, 12}
t _{SU}	Input Data Setup Before CLK		1.319	—	1.412		1.462	—	ns
t _{HO}	Input Data Hold After CLK	All MachXO2	0.717	—	1.010	—	1.340	—	ns
f _{DATA}	DDRX1 Input Data Speed	devices, all sides	—	140	—	116	—	98	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDR	X2 Inputs with Clock and Data A	ligned at Pin Using PO	CLK Pin	for Cloc	k Input -	GDDR)	(2_RX.E	CLK.Ali	gned ^{9, 12}
t _{DVA}	Input Data Valid After CLK		_	0.361		0.346	_	0.334	UI
t _{DVE}	Input Data Hold After CLK	MachXO2-640U,	0.602	—	0.625		0.648	—	UI
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO2-1200/U and larger devices,	—	280	—	234	—	194	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency	bottom side only ¹¹		140	—	117		97	MHz
f _{SCLK}	SCLK Frequency			70		59		49	MHz
Generic DDR	X2 Inputs with Clock and Data Ce	entered at Pin Using PC	LK Pin f	for Clock	Input –	GDDRX	2_RX.EC	LK.Cen	tered ^{9, 12}
t _{SU}	Input Data Setup Before CLK		0.472	—	0.672		0.865		ns
t _{HO}	Input Data Hold After CLK	MachXO2-640U,	0.363	—	0.501	—	0.743	—	ns
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	280	_	234	_	194	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency	bottom side only"		140	—	117		97	MHz
f _{SCLK}	SCLK Frequency			70		59		49	MHz
Generic DDR	4 Inputs with Clock and Data A	ligned at Pin Using PC	LK Pin	for Cloc	k Input -	GDDRX	4_RX.E	CLK.Ali	gned ^{9, 12}
t _{DVA}	Input Data Valid After ECLK		—	0.307		0.316		0.326	UI
t _{DVE}	Input Data Hold After ECLK	MachXO2-640U.	0.662	—	0.650		0.649	—	UI
f _{DATA}	DDRX4 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	420	_	352	_	292	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency	bottom side only ¹¹	—	210	—	176	—	146	MHz
f _{SCLK}	SCLK Frequency	1	—	53	—	44	—	37	MHz



			-3		-2		-1		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Generic DDR4	Inputs with Clock and Data Cer	ntered at Pin Using PC	LK Pin fo	or Clock	Input –	GDDRX4	LRX.EC	LK.Cent	ered ^{9, 12}
t _{SU}	Input Data Setup Before ECLK		0.434		0.535		0.630	—	ns
t _{HO}	Input Data Hold After ECLK	MachXO2-640U,	0.385		0.395		0.463	—	ns
f _{DATA}	DDRX4 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	420	_	352	_	292	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency	bottom side only'		210		176	—	146	MHz
f _{SCLK}	SCLK Frequency		—	53		44	—	37	MHz
7:1 LVDS Inp	uts – GDDR71_RX.ECLK.7.1 ^{9, 1}	2							
t _{DVA}	Input Data Valid After ECLK		—	0.307		0.316	—	0.326	UI
t _{DVE}	Input Data Hold After ECLK		0.662		0.650		0.649	—	UI
f _{DATA}	DDR71 Serial Input Data Speed	MachXO2-640U, MachXO2-1200/U	—	420	_	352	_	292	Mbps
f _{DDR71}	DDR71 ECLK Frequency	and larger devices,		210		176	—	146	MHz
f _{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		_	60	_	50	_	42	MHz
Generic DDR	Outputs with Clock and Data A	ligned at Pin Using PC	LK Pin f	for Clock	k Input –	GDDRX	(1_TX.S	CLK.Aliç	gned ^{9, 12}
t _{DIA}	Output Data Invalid After CLK Output		—	0.850	—	0.910	—	0.970	ns
t _{DIB}	Output Data Invalid Before CLK Output	All MachXO2 devices, all sides		0.850	_	0.910	_	0.970	ns
f _{DATA}	DDRX1 Output Data Speed			140	—	116		98	Mbps
f _{DDRX1}	DDRX1 SCLK frequency			70		58		49	MHz
Generic DDR	Outputs with Clock and Data Ce	ntered at Pin Using PC	LK Pin f	or Clock	Input –	GDDRX	1_TX.SC	LK.Cen	tered ^{9, 12}
t _{DVB}	Output Data Valid Before CLK Output		2.720	_	3.380	_	4.140	_	ns
t _{DVA}	Output Data Valid After CLK Output	All MachXO2	2.720	_	3.380	_	4.140	_	ns
f _{DATA}	DDRX1 Output Data Speed	devices, all sides		140	—	116		98	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)			70	_	58	_	49	MHz
Generic DDR	X2 Outputs with Clock and Data	Aligned at Pin Using P	CLK Pin	for Cloc	k Input	- GDDR	X2_TX.E	CLK.Ali	gned ^{9, 12}
t _{DIA}	Output Data Invalid After CLK Output			0.270	_	0.300	_	0.330	ns
t _{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U	_	0.270	_	0.300	_	0.330	ns
f _{DATA}	DDRX2 Serial Output Data Speed	and larger devices, top side only		280	_	234	_	194	Mbps
f _{DDRX2}	DDRX2 ECLK frequency	1	—	140	—	117	—	97	MHz
f _{SCLK}	SCLK Frequency			70		59	_	49	MHz







Figure 3-6. Receiver RX.CLK.Centered Waveforms



Figure 3-7. Transmitter TX.CLK.Aligned Waveforms



Figure 3-8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms





sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Modes			1		
t _{PRGM}	PROGRAMN low p	ulse accept	55		ns
t _{PRGMJ}	PROGRAMN low p	ulse rejection	—	25	ns
t _{INITL}	INITN low time	LCMXO2-256	—	30	μs
		LCMXO2-640	—	35	μs
		LCMXO2-640U/ LCMXO2-1200	_	55	μs
		LCMXO2-1200U/ LCMXO2-2000	—	70	μs
		LCMXO2-2000U/ LCMXO2-4000	—	105	μs
		LCMXO2-7000	—	130	μs
t _{DPPINIT}	PROGRAMN low to	D INITN Iow	—	150	ns
t _{DPPDONE}	PROGRAMN low to	DONE low	—	150	ns
t _{IODISS}	PROGRAMN low to	—	120	ns	
Slave SPI	·				
f _{MAX}	CCLK clock freque	CCLK clock frequency		66	MHz
t _{ССLКН}	CCLK clock pulse v	CCLK clock pulse width high		—	ns
t _{CCLKL}	CCLK clock pulse v	width low	7.5	_	ns
t _{STSU}	CCLK setup time		2	—	ns
t _{STH}	CCLK hold time		0	—	ns
t _{STCO}	CCLK falling edge	to valid output	—	10	ns
t _{STOZ}	CCLK falling edge	to valid disable	—	10	ns
t _{STOV}	CCLK falling edge	to valid enable	—	10	ns
t _{SCS}	Chip select high tim	ne	25	—	ns
t _{SCSS}	Chip select setup ti	me	3	—	ns
t _{SCSH}	Chip select hold tim	ne	3	—	ns
Master SPI					
f _{MAX}	MCLK clock freque	ncy	—	133	MHz
t _{MCLKH}	MCLK clock pulse v	width high	3.75	—	ns
t _{MCLKL}	MCLK clock pulse v	width low	3.75	—	ns
t _{STSU}	MCLK setup time		5		ns
t _{STH}	MCLK hold time		1		ns
t _{CSSPI}	INITN high to chip	select low	100	200	ns
t _{MCLK}	INITN high to first N	MCLK edge	0.75	1	μs



MachXO2 Family Data Sheet Pinout Information

March 2017

Data Sheet DS1035

Signal Descriptions

Signal Name	I/O	Descriptions				
General Purpose						
		[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).				
		[Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.				
		[A/B/C/D] indicates the PIO within the group to which the pad is connected.				
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic.				
		During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.				
NC	—	No connect.				
GND	_	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together. For QFN 48 package, the exposed die pad is the device ground.				
VCC	_	V_{CC} – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.				
VCCIOx	_	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.				
PLL and Clock Functi	ons (Us	ed as user-programmable I/O pins when not used for PLL or clock pins)				
[LOC]_GPLL[T, C]_IN	_	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.				
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.				
PCLK [n]_[2:0]		Primary Clock pads. One to three clock pads per side.				
Test and Programming	g (Dual t	function pins used for test access port and during sysCONFIG™)				
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.				
ТСК	I	Test Clock input pin, used to clock the 1149.1 state machine.				
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.				
TDO	0	Output pin – Test Data output pin used to shift data out of the device using 1149.1.				
		Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then:				
JTAGENB	I	If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O.				
		If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.				
		For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.				
Configuration (Dual fu	nction p	ins used during sysCONFIG)				
PROGRAMN	I	Initiates configuration sequence when asserted low. During configuration, or when reserved as PROGRAMN in user mode, this pin always has an active pull-up.				

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	MachXO2-4000							
	84 QFN	132 csBGA	144 TQFP	184 csBGA	256 caBGA	256 ftBGA	332 caBGA	484 fpBGA
General Purpose I/O per Bank								
Bank 0	27	25	27	37	50	50	68	70
Bank 1	10	26	29	37	52	52	68	68
Bank 2	22	28	29	39	52	52	70	72
Bank 3	0	7	9	10	16	16	24	24
Bank 4	9	8	10	12	16	16	16	16
Bank 5	0	10	10	15	20	20	28	28
Total General Purpose Single Ended I/O	68	104	114	150	206	206	274	278
Differential I/O per Bank								
Bank 0	13	13	14	18	25	25	34	35
Bank 1	4	13	14	18	26	26	34	34
Bank 2	11	14	14	19	26	26	35	36
Bank 3	0	3	4	4	8	8	12	12
Bank 4	4	4	5	6	8	8	8	8
Bank 5	0	5	5	7	10	10	14	14
Total General Purpose Differential I/O	32	52	56	72	103	103	137	139
Dual Function I/O	28	37	37	37	37	37	37	37
High-speed Differential I/O								
Bank 0	8	8	9	8	18	18	18	18
Gearboxes					-			-
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	8	8	9	9	18	18	18	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	11	14	14	12	18	18	18	18
DQS Groups				-				
Bank 1	1	2	2	2	2	2	2	2
VCCIO Pins								
Bank 0	3	3	3	3	4	4	4	10
Bank 1	1	3	3	3	4	4	4	10
Bank 2	2	3	3	3	4	4	4	10
Bank 3	1	1	1	1	1	1	2	3
Bank 4	1	1	1	1	2	2	1	4
Bank 5	1	1	1	1	1	1	2	3
		1						
VCC	4	4	4	4	8	8	8	12
GND	4	10	12	16	24	24	27	48
NC	1	1	1	1	1	1	5	105
Reserved for configuration	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	84	132	144	184	256	256	332	484



For Further Information

For further information regarding logic signal connections for various packages please refer to the MachXO2 Device Pinout Files.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Users must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1198, Power Estimation and Management for MachXO2 Devices
- The Power Calculator tool is included with the Lattice design tools, or as a standalone download from www.latticesemi.com/software



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484C	2112	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-5FG484C	2112	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-6FG484C	2112	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84C	4320	2.5 V / 3.3 V	-4	Halogen-Free QFN	84	COM
LCMXO2-4000HC-5QN84C	4320	2.5 V / 3.3 V	-5	Halogen-Free QFN	84	COM
LCMXO2-4000HC-6QN84C	4320	2.5 V / 3.3 V	-6	Halogen-Free QFN	84	COM
LCMXO2-4000HC-4MG132C	4320	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-5MG132C	4320	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-6MG132C	4320	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-4TG144C	4320	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-5TG144C	4320	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-6TG144C	4320	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-4BG256C	4320	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-5BG256C	4320	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-6BG256C	4320	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-4FTG256C	4320	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-5FTG256C	4320	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-6FTG256C	4320	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-4BG332C	4320	2.5 V / 3.3 V	-4	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-5BG332C	4320	2.5 V / 3.3 V	-5	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-6BG332C	4320	2.5 V / 3.3 V	-6	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-4FG484C	4320	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-5FG484C	4320	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-6FG484C	4320	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	COM



R1 Device Specifications

The LCMXO2-1200ZE/HC "R1" devices have the same specifications as their Standard (non-R1) counterparts except as listed below. For more details on the R1 to Standard migration refer to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard Non-R1) Devices.

- The User Flash Memory (UFM) cannot be programmed through the internal WISHBONE interface. It can still be programmed through the JTAG/SPI/I²C ports.
- The on-chip differential input termination resistor value is higher than intended. It is approximately 200Ω as opposed to the intended 100Ω. It is recommended to use external termination resistors for differential inputs. The on-chip termination resistors can be disabled through Lattice design software.
- Soft Error Detection logic may not produce the correct result when it is run for the first time after configuration. To use this feature, discard the result from the first operation. Subsequent operations will produce the correct result.
- Under certain conditions, IIH exceeds data sheet specifications. The following table provides more details:

Condition	Clamp	Pad Rising IIH Max.	Pad Falling IIH Min.	Steady State Pad High IIH	Steady State Pad Low IIL
VPAD > VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD = VCCIO	ON	10 µA	–10 μA	10 µA	10 µA
VPAD = VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD < VCCIO	OFF	10 µA	–10 μA	10 µA	10 µA

- The user SPI interface does not operate correctly in some situations. During master read access and slave write access, the last byte received does not generate the RRDY interrupt.
- In GDDRX2, GDDRX4 and GDDR71 modes, ECLKSYNC may have a glitch in the output under certain conditions, leading to possible loss of synchronization.
- When using the hard I²C IP core, the I²C status registers I2C_1_SR and I2C_2_SR may not update correctly.
- PLL Lock signal will glitch high when coming out of standby. This glitch lasts for about 10 μsec before returning low.
- Dual boot only available on HC devices, requires tying VCC and VCCIO2 to the same 3.3 V or 2.5 V supply.



Date	Version	Section	Change Summary
May 2016	3.2	All	Moved designation for 84 QFN package information from 'Advanced' to 'Final'.
	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 'Advanced' 48 QFN package. — Revised footnote 6. — Added footnote 9.	
		DC and Switching Characteristics	Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Added footnote 12.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Added footnote 12.
		Pinout Information	Updated the Signal Descriptions section. Added information on GND signal.
			Updated the Pinout Information Summary section. — Added 'Advanced' MachXO2-256 48 QFN values. — Added 'Advanced' MachXO2-640 48 QFN values. — Added footnote to GND. — Added footnotes 2 and 3.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added 'Advanced' SG48 package and revised footnote.
			Updated the Ordering Information section. — Added part numbers for 'Advanced' QFN 48 package.
March 2016 3.1	3.1	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 32 QFN value for XO2-1200. — Added 84 QFN (7 mm x 7 mm, 0.5 mm) package. — Modified package name to 100-pin TQFP. — Modified package name to 144-pin TQFP. — Added footnote.
		Architecture	Updated the Typical I/O Behavior During Power-up section. Removed reference to TN1202.
		DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications section. Revised t _{DPPDONE} and t _{DPPINIT} Max. values per PCN 03A-16, released March 2016.
		Pinout Information Ordering Information	Updated the Pinout Information Summary section. — Added MachXO2-1200 32 QFN values. — Added 'Advanced' MachXO2-4000 84 QFN values.
			Updated the MachXO2 Part Number Description section. Added 'Advanced' QN84 package and footnote.
			Updated the Ordering Information section. — Added part numbers for 1280 LUTs QFN 32 package. — Added part numbers for 4320 LUTs QFN 84 package.
March 2015	3.0	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Changed 64-ball ucBGA dimension.
		Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.



Date	Version	Section	Change Summary				
January 2013	02.0	Introduction	Updated the total number IOs to include JTAGENB.				
		Architecture	Supported Output Standards table – Added 3.3 $\rm V_{\rm CCIO}$ (Typ.) to LVDS row.				
			Changed SRAM CRC Error Detection to Soft Error Detection.				
		DC and Switching Characteristics	Power Supply Ramp Rates table – Updated Units column for t _{RAMP} symbol.				
			Added new Maximum sysIO Buffer Performance table.				
			sysCLOCK PLL Timing table – Updated Min. column values for f_{IN} ,				
			f_{OUT},f_{OUT2} and f_{PFD} parameters. Added t_{SPO} parameter. Updated footnote 6.				
			MachXO2 Oscillator Output Frequency table – Updated symbol name for t _{STABLEOSC} .				
			DC Electrical Characteristics table – Updated conditions for ${\rm I}_{\rm IL,}~{\rm I}_{\rm IH}$ symbols.				
			Corrected parameters tDQVBS and tDQVAS				
			Corrected MachXO2 ZE parameters tDVADQ and tDVEDQ				
		Pinout Information	Included the MachXO2-4000HE 184 csBGA package.				
		Ordering Information	Updated part number.				
April 2012	01.9	Architecture	Removed references to TN1200.				
		Ordering Information	Updated the Device Status portion of the MachXO2 Part Number Description to include the 50 parts per reel for the WLCSP package.				
			Added new part number and footnote 2 for LCMXO2-1200ZE- 1UWG25ITR50.				
			Updated footnote 1 for LCMXO2-1200ZE-1UWG25ITR.				
		Supplemental Information	Removed references to TN1200.				
March 2012	01.8	Introduction	Added 32 QFN packaging information to Features bullets and MachXO2 Family Selection Guide table.				
		DC and Switching Characteristics	Changed 'STANDBY' to 'USERSTDBY' in Standby Mode timing dia- gram.				
		Pinout Information	Removed footnote from Pin Information Summary tables.				
			Added 32 QFN package to Pin Information Summary table.				
		Ordering Information	Updated Part Number Description and Ordering Information tables for 32 QFN package.				
			Updated topside mark diagram in the Ordering Information section.				



Date	Version	Section	Change Summary
February 2012	01.7	All	Updated document with new corporate logo.
	01.6	—	Data sheet status changed from preliminary to final.
		Introduction	MachXO2 Family Selection Guide table – Removed references to 49-ball WLCSP.
		DC and Switching Characteristics	Updated Flash Download Time table.
			Modified Storage Temperature in the Absolute Maximum Ratings section.
			Updated I _{DK} max in Hot Socket Specifications table.
			Modified Static Supply Current tables for ZE and HC/HE devices.
			Updated Power Supply Ramp Rates table.
			Updated Programming and Erase Supply Current tables.
			Updated data in the External Switching Characteristics table.
			Corrected Absolute Maximum Ratings for Dedicated Input Voltage Applied for LCMXO2 HC.
			DC Electrical Characteristics table – Minor corrections to conditions for $\mathbf{I}_{IL}, \mathbf{I}_{IH.}$
		Pinout Information	Removed references to 49-ball WLCSP.
			Signal Descriptions table – Updated description for GND, VCC, and VCCIOx.
			Updated Pin Information Summary table – Number of VCCIOs, GNDs, VCCs, and Total Count of Bonded Pins for MachXO2-256, 640, and 640U and Dual Function I/O for MachXO2-4000 332caBGA.
		Ordering Information	Removed references to 49-ball WLCSP
August 2011	01.5	DC and Switching Characteristics	Updated ESD information.
		Ordering Information	Updated footnote for ordering WLCSP devices.
	01.4	Architecture	Updated information in Clock/Control Distribution Network and sys- CLOCK Phase Locked Loops (PLLs).
		DC and Switching Characteristics	Updated ${\rm I}_{\rm IL}$ and ${\rm I}_{\rm IH}$ conditions in the DC Electrical Characteristics table.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Updated Pin Information Summary table: Dual Function I/O, DQS Groups Bank 1, Total General Purpose Single-Ended I/O, Differential I/O Per Bank, Total Count of Bonded Pins, Gearboxes.
			Added column of data for MachXO2-2000 49 WLCSP.
		Ordering Information	Updated R1 Device Specifications text section with information on migration from MachXO2-1200-R1 to Standard (non-R1) devices.
			Corrected Supply Voltage typo for part numbers: LCMX02-2000UHE- 4FG484I, LCMX02-2000UHE-5FG484I, LCMX02-2000UHE- 6FG484I.
			Added footnote for WLCSP package parts.
		Supplemental Information	Removed reference to Stand-alone Power Calculator for MachXO2 Devices. Added reference to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices.