# E. K Hattice Semiconductor Corporation - LCMX02-2000HE-6TG100I Datasheet



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	264
Number of Logic Elements/Cells	2112
Total RAM Bits	75776
Number of I/O	79
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-2000he-6tg100i

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# MachXO2 Family Data Sheet Introduction

May 2016

### Features

- Flexible Logic Architecture
  - Six devices with 256 to 6864 LUT4s and 18 to 334 I/Os
- Ultra Low Power Devices
  - Advanced 65 nm low power process
  - As low as 22  $\mu$ W standby power
  - Programmable low swing differential I/Os
  - · Stand-by mode and other power saving options

### Embedded and Distributed Memory

- Up to 240 kbits sysMEM™ Embedded Block RAM
- Up to 54 kbits Distributed RAM
- Dedicated FIFO control logic
- On-Chip User Flash Memory
  - Up to 256 kbits of User Flash Memory
  - 100,000 write cycles
  - Accessible through WISHBONE, SPI, I<sup>2</sup>C and JTAG interfaces
  - Can be used as soft processor PROM or as Flash memory

### Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/Os
- Generic DDR, DDRX2, DDRX4
- Dedicated DDR/DDR2/LPDDR memory with DQS support

### ■ High Performance, Flexible I/O Buffer

- Programmable sysIO<sup>™</sup> buffer supports wide range of interfaces:
  - LVCMOS 3.3/2.5/1.8/1.5/1.2
  - LVTTL
  - PCI
  - LVDS, Bus-LVDS, MLVDS, RSDS, LVPECL
  - SSTL 25/18
  - HSTL 18
  - Schmitt trigger inputs, up to 0.5 V hysteresis
- I/Os support hot socketing
- On-chip differential termination
- · Programmable pull-up or pull-down mode

- Flexible On-Chip Clocking
  - · Eight primary clocks
  - Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
  - Up to two analog PLLs per device with fractional-n frequency synthesis
    - Wide input frequency range (7 MHz to 400 MHz)

Data Sheet DS1035

- Non-volatile, Infinitely Reconfigurable
  - Instant-on powers up in microseconds
  - Single-chip, secure solution
  - Programmable through JTAG, SPI or I<sup>2</sup>C
  - Supports background programming of non-volatile memory
  - Optional dual boot with external SPI memory
- TransFR<sup>™</sup> Reconfiguration
  - In-field logic update while system operates

### Enhanced System Level Support

- On-chip hardened functions: SPI, I<sup>2</sup>C, timer/ counter
- On-chip oscillator with 5.5% accuracy
- Unique TraceID for system tracking
- One Time Programmable (OTP) mode
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming
- Broad Range of Package Options
  - TQFP, WLCSP, ucBGA, csBGA, caBGA, ftBGA, fpBGA, QFN package options
  - Small footprint package options
     As small as 2.5 mm x 2.5 mm
  - · Density migration supported
  - · Advanced halogen-free packaging



### **ROM Mode**

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

## Routing

There are many resources provided in the MachXO2 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

## **Clock/Control Distribution Network**

Each MachXO2 device has eight clock inputs (PCLK [T, C] [Banknum]\_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO2 architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO2-640U, MachXO2-1200/U and higher density devices have two edge clocks each on the top and bottom edges. Lower density devices have no edge clocks. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO2 devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO2 External Switching Characteristics table.

The primary clock signals for the MachXO2-256 and MachXO2-640 are generated from eight 17:1 muxes The available clock sources include eight I/O sources and 9 routing inputs. Primary clock signals for the MachXO2-640U, MachXO2-1200/U and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.



Figure 2-11. Group of Four Programmable I/O Cells



Notes:

1. Input gearbox is available only in PIC on the bottom edge of MachXO2-640U, MachXO2-1200/U and larger devices. 2. Output gearbox is available only in PIC on the top edge of MachXO2-640U, MachXO2-1200/U and larger devices.



### Figure 2-17. Output Gearbox



More information on the output gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.



### Figure 2-21. PC Core Block Diagram



Table 2-15 describes the signals interfacing with the I<sup>2</sup>C cores.

 Table 2-15.
 PC Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I <sup>2</sup> C core. The signal is an output if the I <sup>2</sup> C core is in master mode. The signal is an input if the I <sup>2</sup> C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I <sup>2</sup> C ports in each MachXO2 device.
i2c_sda	Bi-directional	Bi-directional data line of the $l^2C$ core. The signal is an output when data is transmitted from the $l^2C$ core. The signal is an input when data is received into the $l^2C$ core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of $l^2C$ ports in each MachXO2 device.
i2c_irqo	Output	Interrupt request output signal of the I <sup>2</sup> C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I <sup>2</sup> C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, $I^2C$ Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, $I^2C$ Tab.

### Hardened SPI IP Core

Every MachXO2 device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO2 devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface



Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe $V_{CC}$ drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1198, Power Estimation and Management for MachXO2 Devices.

### Power On Reset

MachXO2 devices have power-on reset circuitry to monitor  $V_{CCINT}$  and  $V_{CCIO}$  voltage levels during power-up and operation. At power-up, the POR circuitry monitors  $V_{CCINT}$  and  $V_{CCIO0}$  (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the  $V_{PORUP}$  level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices),  $V_{CCINT}$  is the same as the  $V_{CC}$  supply voltage. For devices with voltage regulators (HC devices),  $V_{CCINT}$  is regulated from the  $V_{CC}$  supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time (t<sub>REFRESH</sub>) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tristate. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external  $V_{CC}$  voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor  $V_{CCINT}$  levels. If  $V_{CCINT}$  drops below  $V_{PORDNBG}$  level (with the bandgap circuitry switched on) or below  $V_{PORDNSRAM}$  level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the  $V_{CCINT}$  and  $V_{CCIO}$  voltage levels.  $V_{PORDNBG}$  and  $V_{PORDNSRAM}$  are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the  $V_{PORDNSRAM}$  reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the  $V_{CC}$  supply dropping below  $V_{CC}$  (min) they should not shut down the bandgap or POR circuit.



## **Configuration and Testing**

This section describes the configuration and testing features of the MachXO2 family.

### IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V<sub>CCIO</sub> Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

### **Device Configuration**

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I<sup>2</sup>C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

- 1. Internal Flash Download
- 2. JTAG
- 3. Standard Serial Peripheral Interface (Master SPI mode) interface to boot PROM memory
- 4. System microprocessor to drive a serial slave SPI port (SSPI mode)
- 5. Standard I<sup>2</sup>C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, MachXO2 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

#### TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.



# Static Supply Current – HC/HE Devices<sup>1, 2, 3, 6</sup>

Symbol	Parameter	Device	Typ. <sup>4</sup>	Units
		LCMXO2-256HC	1.15	mA
		LCMXO2-640HC	1.84	mA
		LCMXO2-640UHC	3.48	mA
		LCMXO2-1200HC	3.49	mA
	Core Power Supply	LCMXO2-1200UHC	4.80	mA
1		LCMXO2-2000HC	4.80	mA
'CC		LCMXO2-2000UHC	8.44	mA
		LCMXO2-4000HC	8.45	mA
		LCMXO2-7000HC	12.87	mA
		LCMXO2-2000HE	1.39	mA
		LCMXO2-4000HE	2.55	mA
		LCMXO2-7000HE	4.06	mA
I <sub>CCIO</sub>	Bank Power Supply <sup>5</sup> $V_{CCIO} = 2.5 V$	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.

2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V<sub>CCIO</sub> or GND, on-chip oscillator is off, on-chip PLL is off.

3. Frequency = 0 MHz.

4.  $T_J = 25$  °C, power supplies at nominal voltage.

5. Does not include pull-up/pull-down.

6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

# Programming and Erase Flash Supply Current – HC/HE Devices<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Device	Typ.⁵	Units
		LCMXO2-256HC	14.6	mA
		LCMXO2-640HC	16.1	mA
		LCMXO2-640UHC	18.8	mA
		LCMXO2-1200HC	18.8	mA
		LCMXO2-1200UHC	22.1	mA
		LCMXO2-2000HC	22.1	mA
I <sub>CC</sub>	Core Power Supply	LCMXO2-2000UHC	26.8	mA
		LCMXO2-4000HC	26.8	mA
		LCMXO2-7000HC	33.2	mA
		LCMXO2-2000HE	18.3	mA
		LCMXO2-2000UHE	20.4	mA
		LCMXO2-4000HE	20.4	mA
		LCMXO2-7000HE	23.9	mA
I <sub>CCIO</sub>	Bank Power Supply <sup>6</sup>	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.

2. Assumes all inputs are held at  $V_{CCIO}$  or GND and all outputs are tri-stated.

3. Typical user pattern.

4. JTAG programming is at 25 MHz.

5.  $T_J = 25$  °C, power supplies at nominal voltage.

6. Per bank.  $V_{CCIO} = 2.5$  V. Does not include pull-up/pull-down.



# sysIO Recommended Operating Conditions

		V <sub>CCIO</sub> (V)		V <sub>REF</sub> (V)		
Standard	Min.	Тур.	Max.	Min.	Тур.	Max.
LVCMOS 3.3	3.135	3.3	3.6	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.6	—	—	—
PCI <sup>3</sup>	3.135	3.3	3.6	—	—	—
SSTL25	2.375	2.5	2.625	1.15	1.25	1.35
SSTL18	1.71	1.8	1.89	0.833	0.9	0.969
HSTL18	1.71	1.8	1.89	0.816	0.9	1.08
LVCMOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVCMOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVCMOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVCMOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVCMOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVCMOS12R334	3.135	3.3	3.6	0.45	0.6	0.75
LVCMOS12R254	2.375	2.5	2.625	0.45	0.6	0.75
LVCMOS10R334	3.135	3.3	3.6	0.35	0.5	0.65
LVCMOS10R254	2.375	2.5	2.625	0.35	0.5	0.65
LVDS25 <sup>1, 2</sup>	2.375	2.5	2.625	—	—	—
LVDS33 <sup>1, 2</sup>	3.135	3.3	3.6	—	—	—
LVPECL <sup>1</sup>	3.135	3.3	3.6	—	—	—
BLVDS <sup>1</sup>	2.375	2.5	2.625	—	—	—
RSDS <sup>1</sup>	2.375	2.5	2.625	—	—	—
SSTL18D	1.71	1.8	1.89	—	—	—
SSTL25D	2.375	2.5	2.625	—	—	—
HSTL18D	1.71	1.8	1.89	—	—	—

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.

2. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.

3. Input on the bottom bank of the MachXO2-640U, MachXO2-1200/U and larger devices only.

4. Supported only for inputs and BIDIs for all ZE devices, and -6 speed grade for HE and HC devices.



# sysIO Single-Ended DC Electrical Characteristics<sup>1, 2</sup>

Input/Output	V <sub>IL</sub>		V <sub>IH</sub>		Vo. Max.	Vou Min.	lo Max.4	Iou Max. <sup>4</sup>
Standard	Min. (V) <sup>3</sup>	Max. (V)	Min. (V)	Max. (V)	(V)	(V)	(mA)	(mA)
							4	-4
	-0.3	0.8					8	-8
LVCMOS 3.3			2.0	3.6	0.4	$V_{CCIO} - 0.4$	12	-12
LVTTL	-0.0	0.0	2.0	0.0			16	-16
							24	-24
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
							4	-4
					04	$V_{000} = 0.4$	8	-8
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	VCCI0 0.4	12	-12
							16	-16
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
							4	-4
LVCMOS 1.8	-0.3	0.25\/	0.65V <sub>CCIO</sub>	3.6	0.4	$V_{CCIO} - 0.4$	8	-8
		0.35V <sub>CCIO</sub>					12	-12
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.5	-0.3	0.35V <sub>CCIO</sub>	0.65V <sub>CCIO</sub>	3.6	0.4	V <sub>CCIO</sub> - 0.4	4	-4
							8	-8
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
	-0.3	0.35V <sub>CCIO</sub>	0.65V <sub>CCIO</sub>	3.6	0.4	V 04	4	-2
LVCMOS 1.2						VCCIO - 0.4	8	-6
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
PCI	-0.3	0.3V <sub>CCIO</sub>	0.5V <sub>CCIO</sub>	3.6	0.1V <sub>CCIO</sub>	0.9V <sub>CCIO</sub>	1.5	-0.5
SSTL25 Class I	-0.3	V <sub>REF</sub> - 0.18	V <sub>REF</sub> + 0.18	3.6	0.54	V <sub>CCIO</sub> - 0.62	8	8
SSTL25 Class II	-0.3	V <sub>REF</sub> - 0.18	V <sub>REF</sub> + 0.18	3.6	NA	NA	NA	NA
SSTL18 Class I	-0.3	V <sub>REF</sub> – 0.125	V <sub>REF</sub> + 0.125	3.6	0.40	V <sub>CCIO</sub> - 0.40	8	8
SSTL18 Class II	-0.3	V <sub>REF</sub> – 0.125	V <sub>REF</sub> + 0.125	3.6	NA	NA	NA	NA
HSTL18 Class I	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	0.40	V <sub>CCIO</sub> - 0.40	8	8
HSTL18 Class II	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	NA	NA	NA	NA
LVCMOS25R33	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R33	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R25	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R33	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R25	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	NA	NA	NA	NA
LVCMOS12R33	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain



Input/Output	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub> Max.	V <sub>OH</sub> Min.	I <sub>OL</sub> Max. <sup>4</sup>	I <sub>OH</sub> Max.⁴
Standard	Min. (V) <sup>3</sup>	Max. (V)	Min. (V)	Max. (V)	ς(Λ)	(V)	ິ(mA)	(mA)
LVCMOS10R25	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain

MachXO2 devices allow LVCMOS inputs to be placed in I/O banks where V<sub>CCIO</sub> is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO2 devices do not meet the relevant JEDEC specification are documented in the table below.

2. MachXO2 devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1202, MachXO2 sysIO Usage Guide.

3. The dual function I<sup>2</sup>C pins SCL and SDA are limited to a  $V_{IL}$  min of -0.25 V or to -0.3 V with a duration of <10 ns.

4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive VCCIO or GND pad connections, or between the last VCCIO or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n \* 8 mA. "n" is the number of I/O pads between the two consecutive bank VCCIO or GND connections or between the last VCCIO and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

Input Standard	V <sub>CCIO</sub> (V)	V <sub>IL</sub> Max. (V)
LVCMOS 33	1.5	0.685
LVCMOS 25	1.5	0.687
LVCMOS 18	1.5	0.655

### sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of MachXO2-640U, MachXO2-1200/U and higher density devices in the MachXO2 PLD family.

### LVDS

### Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Тур.	Max.	Units
V	Input Voltage	V <sub>CCIO</sub> = 3.3 V	0		2.605	V
VINB VINM	input voltage	V <sub>CCIO</sub> = 2.5 V	0		2.05	V
V <sub>THD</sub>	Differential Input Threshold		±100			mV
V	Input Common Mode Voltage	V <sub>CCIO</sub> = 3.3 V	0.05		2.6	V
VCM	input common mode voltage	V <sub>CCIO</sub> = 2.5 V	0.05		2.0	V
I <sub>IN</sub>	Input current	Power on	_		±10	μΑ
V <sub>OH</sub>	Output high voltage for $V_{OP}$ or $V_{OM}$	R <sub>T</sub> = 100 Ohm	_	1.375	_	V
V <sub>OL</sub>	Output low voltage for $V_{OP}$ or $V_{OM}$	R <sub>T</sub> = 100 Ohm	0.90	1.025	_	V
V <sub>OD</sub>	Output voltage differential	(V <sub>OP</sub> - V <sub>OM</sub> ), R <sub>T</sub> = 100 Ohm	250	350	450	mV
$\Delta V_{OD}$	Change in V <sub>OD</sub> between high and low		_		50	mV
V <sub>OS</sub>	Output voltage offset	$(V_{OP} + V_{OM})/2, R_{T} = 100 \text{ Ohm}$	1.125	1.20	1.395	V
$\Delta V_{OS}$	Change in V <sub>OS</sub> between H and L		_	_	50	mV
I <sub>OSD</sub>	Output short circuit current	V <sub>OD</sub> = 0 V driver outputs shorted	_		24	mA



### BLVDS

The MachXO2 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

### Figure 3-2. BLVDS Multi-point Output Example



#### Table 3-2. BLVDS DC Conditions<sup>1</sup>

Over Recommended	Operating	Conditions
	operating	oonantions

		Nor	ninal	
Symbol	Description	Zo = 45	Zo = 90	Units
Z <sub>OUT</sub>	Output impedance	20	20	Ohms
R <sub>S</sub>	Driver series resistance	80	80	Ohms
R <sub>TLEFT</sub>	Left end termination	45	90	Ohms
R <sub>TRIGHT</sub>	Right end termination	45	90	Ohms
V <sub>OH</sub>	Output high voltage	1.376	1.480	V
V <sub>OL</sub>	Output low voltage	1.124	1.020	V
V <sub>OD</sub>	Output differential voltage	0.253	0.459	V
V <sub>CM</sub>	Output common mode voltage	1.250	1.250	V
I <sub>DC</sub>	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.



# Typical Building Block Function Performance – ZE Devices<sup>1</sup>

### Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–3 Timing	Units
Basic Functions		
16-bit decoder	13.9	ns
4:1 MUX	10.9	ns
16:1 MUX	12.0	ns

### **Register-to-Register Performance**

Function	–3 Timing	Units
Basic Functions		·
16:1 MUX	191	MHz
16-bit adder	134	MHz
16-bit counter	148	MHz
64-bit counter	77	MHz
Embedded Memory Functions	·	
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	90	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	214	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

### **Derating Logic Timing**

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.



			_	-3	-	2	_	-1	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
LPDDR <sup>9, 12</sup>			1						
t <sub>DVADQ</sub>	Input Data Valid After DQS Input			0.349	_	0.381	_	0.396	UI
t <sub>DVEDQ</sub>	Input Data Hold After DQS Input		0.665	_	0.630		0.613	_	UI
t <sub>DQVBS</sub>	Output Data Invalid Before DQS Output	MachXO2-1200/U	0.25	_	0.25		0.25	_	UI
t <sub>DQVAS</sub>	Output Data Invalid After DQS Output	and larger devices, right side only. <sup>13</sup>	0.25	_	0.25	_	0.25	_	UI
f <sub>DATA</sub>	MEM LPDDR Serial Data Speed		_	120	_	110	_	96	Mbps
f <sub>SCLK</sub>	SCLK Frequency		—	60		55		48	MHz
f <sub>LPDDR</sub>	LPDDR Data Transfer Rate		0	120	0	110	0	96	Mbps
DDR <sup>9, 12</sup>	•	•							
t <sub>DVADQ</sub>	Input Data Valid After DQS Input			0.347	_	0.374	_	0.393	UI
t <sub>DVEDQ</sub>	Input Data Hold After DQS Input	-	0.665	_	0.637		0.616	_	UI
t <sub>DQVBS</sub>	Output Data Invalid Before DQS Output	MachXO2-1200/U	0.25	_	0.25		0.25	_	UI
t <sub>DQVAS</sub>	Output Data Invalid After DQS Output	right side only. <sup>13</sup>	0.25	_	0.25	_	0.25	_	UI
f <sub>DATA</sub>	MEM DDR Serial Data Speed			140	_	116		98	Mbps
f <sub>SCLK</sub>	SCLK Frequency			70		58	—	49	MHz
f <sub>MEM DDR</sub>	MEM DDR Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps
DDR2 <sup>9, 12</sup>		ı	1	1	1		1	1	
t <sub>DVADQ</sub>	Input Data Valid After DQS Input		_	0.372	_	0.394	_	0.410	UI
t <sub>DVEDQ</sub>	Input Data Hold After DQS Input		0.690	_	0.658	_	0.618	_	UI
t <sub>DQVBS</sub>	Output Data Invalid Before DQS Output	MachXO2-1200/U	0.25	_	0.25	_	0.25	_	UI
t <sub>DQVAS</sub>	Output Data Invalid After DQS Output	and larger devices, right side only. <sup>13</sup>	0.25	_	0.25	_	0.25	_	UI
f <sub>DATA</sub>	MEM DDR Serial Data Speed	1	—	140	—	116		98	Mbps
f <sub>SCLK</sub>	SCLK Frequency	1	<u> </u>	70	—	58		49	MHz
f <sub>MEM_DDR2</sub>	MEM DDR2 Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pf load, fast slew rate.

3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).

4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.

5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).

6. For Generic DDRX1 mode  $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$ .

7. The  $t_{SU_{DEL}}$  and  $t_{H_{DEL}}$  values use the SCLK\_ZERHOLD default step size. Each step is 167 ps (-3), 182 ps (-2), 195 ps (-1).

8. This number for general purpose usage. Duty cycle tolerance is +/-10%.

9. Duty cycle is +/-5% for system usage.

10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.

11. High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.

12. Advance information for MachXO2 devices in 48 QFN packages.

13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.



## Flash Download Time<sup>1, 2</sup>

Symbol	Parameter	Device	Тур.	Units
		LCMXO2-256	0.6	ms
		LCMXO2-640	1.0	ms
		LCMXO2-640U	1.9	ms
		LCMXO2-1200	1.9	ms
t <sub>REFRESH</sub>	POR to Device I/O Active	LCMXO2-1200U	1.4	ms
		LCMXO2-2000	1.4	ms
		LCMXO2-2000U	2.4	ms
		LCMXO2-4000	2.4	ms
		LCMXO2-7000	3.8	ms

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.

2. The Flash download time is measured starting from the maximum voltage of POR trip point.

### **JTAG Port Timing Specifications**

Symbol	Parameter	Min.	Max.	Units
f <sub>MAX</sub>	TCK clock frequency	—	25	MHz
t <sub>BTCPH</sub>	TCK [BSCAN] clock pulse width high	20	—	ns
t <sub>BTCPL</sub>	TCK [BSCAN] clock pulse width low	20	—	ns
t <sub>BTS</sub>	TCK [BSCAN] setup time	10	—	ns
t <sub>BTH</sub>	TCK [BSCAN] hold time	8	—	ns
t <sub>BTCO</sub>	TAP controller falling edge of clock to valid output	—	10	ns
t <sub>BTCODIS</sub>	TAP controller falling edge of clock to valid disable	—	10	ns
t <sub>BTCOEN</sub>	TAP controller falling edge of clock to valid enable	—	10	ns
t <sub>BTCRS</sub>	BSCAN test capture register setup time	8	—	ns
t <sub>BTCRH</sub>	BSCAN test capture register hold time	20	—	ns
t <sub>BUTCO</sub>	BSCAN test update register, falling edge of clock to valid output	—	25	ns
t <sub>BTUODIS</sub>	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
t <sub>BTUPOEN</sub>	BSCAN test update register, falling edge of clock to valid enable	—	25	ns





	MachXO2-1200				MachXO2-1200U	
	100 TQFP	132 csBGA	144 TQFP	25 WLCSP	32 QFN <sup>1</sup>	256 ftBGA
General Purpose I/O per Bank						
Bank 0	18	25	27	11	9	50
Bank 1	21	26	26	0	2	52
Bank 2	20	28	28	7	9	52
Bank 3	20	25	26	0	2	16
Bank 4	0	0	0	0	0	16
Bank 5	0	0	0	0	0	20
Total General Purpose Single Ended I/O	79	104	107	18	22	206
Differential I/O per Bank						
Bank 0	9	13	14	5	4	25
Bank 1	10	13	13	0	1	26
Bank 2	10	14	14	2	4	26
Bank 3	10	12	13	0	1	8
Bank 4	0	0	0	0	0	8
Bank 5	0	0	0	0	0	10
Total General Purpose Differential I/O	39	52	54	7	10	103
Dual Function I/O	31	33	33	18	22	33
High-speed Differential I/O						1
Bank 0	4	7	7	0	0	14
Gearboxes						1
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	4	7	7	0	0	14
Number of 7:1 or 8:1 Input Gearbox Avail- able (Bank 2)	5	7	7	0	2	14
DQS Groups						
Bank 1	1	2	2	0	0	2
VCCIO Pins	1	1				1
Bank 0	2	3	3	1	2	4
Bank 1	2	3	3	0	1	4
Bank 2	2	3	3	1	2	4
Bank 3	3	3	3	0	1	1
Bank 4	0	0	0	0	0	2
Bank 5	0	0	0	0	0	1
	I			Гг		Γ
VCC	2	4	4	2	2	8
GND	8	10	12	2	2	24
NC	1	1	8	0	0	1
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	100	132	144	25	32	256

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.



# High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32C	256	2.5 V / 3.3 V	-4	Halogen-Free QFN	32	COM
LCMXO2-256HC-5SG32C	256	2.5 V / 3.3 V	-5	Halogen-Free QFN	32	COM
LCMXO2-256HC-6SG32C	256	2.5 V / 3.3 V	-6	Halogen-Free QFN	32	COM
LCMXO2-256HC-4SG48C	256	2.5 V / 3.3 V	-4	Halogen-Free QFN	48	COM
LCMXO2-256HC-5SG48C	256	2.5 V / 3.3 V	-5	Halogen-Free QFN	48	COM
LCMXO2-256HC-6SG48C	256	2.5 V / 3.3 V	-6	Halogen-Free QFN	48	COM
LCMXO2-256HC-4UMG64C	256	2.5 V / 3.3 V	-4	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-5UMG64C	256	2.5 V / 3.3 V	-5	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-6UMG64C	256	2.5 V / 3.3 V	-6	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-4TG100C	256	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-256HC-5TG100C	256	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-256HC-6TG100C	256	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-256HC-4MG132C	256	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-256HC-5MG132C	256	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-256HC-6MG132C	256	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48C	640	2.5 V / 3.3 V	-4	Halogen-Free QFN	48	COM
LCMXO2-640HC-5SG48C	640	2.5 V / 3.3 V	-5	Halogen-Free QFN	48	COM
LCMXO2-640HC-6SG48C	640	2.5 V / 3.3 V	-6	Halogen-Free QFN	48	COM
LCMXO2-640HC-4TG100C	640	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-640HC-5TG100C	640	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-640HC-6TG100C	640	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-640HC-4MG132C	640	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-640HC-5MG132C	640	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-640HC-6MG132C	640	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144C	640	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-5TG144C	640	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-6TG144C	640	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	COM



# High Performance Industrial Grade Devices Without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100I	2112	1.2 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-5TG100I	2112	1.2 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-6TG100I	2112	1.2 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-4MG132I	2112	1.2 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-5MG132I	2112	1.2 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-6MG132I	2112	1.2 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-4TG144I	2112	1.2 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-5TG144I	2112	1.2 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-6TG144I	2112	1.2 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-4BG256I	2112	1.2 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-5BG256I	2112	1.2 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-6BG256I	2112	1.2 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-4FTG256I	2112	1.2 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-5FTG256I	2112	1.2 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-6FTG256I	2112	1.2 V	-6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484I	2112	1.2 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-5FG484I	2112	1.2 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-6FG484I	2112	1.2 V	-6	Halogen-Free fpBGA	484	IND



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4MG132I	4320	1.2 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-5MG132I	4320	1.2 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-6MG132I	4320	1.2 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-4TG144I	4320	1.2 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-5TG144I	4320	1.2 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-6TG144I	4320	1.2 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-4MG184I	4320	1.2 V	-4	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-5MG184I	4320	1.2 V	-5	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-6MG184I	4320	1.2 V	-6	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-4BG256I	4320	1.2 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-5BG256I	4320	1.2 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-6BG256I	4320	1.2 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-4FTG256I	4320	1.2 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-5FTG256I	4320	1.2 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-6FTG256I	4320	1.2 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-4BG332I	4320	1.2 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-5BG332I	4320	1.2 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-6BG332I	4320	1.2 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-4FG484I	4320	1.2 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-5FG484I	4320	1.2 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-6FG484I	4320	1.2 V	-6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144I	6864	1.2 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-5TG144I	6864	1.2 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-6TG144I	6864	1.2 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-4BG256I	6864	1.2 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-5BG256I	6864	1.2 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-6BG256I	6864	1.2 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-4FTG256I	6864	1.2 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-5FTG256I	6864	1.2 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-6FTG256I	6864	1.2 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-4BG332I	6864	1.2 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-5BG332I	6864	1.2 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-6BG332I	6864	1.2 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-4FG484I	6864	1.2 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-5FG484I	6864	1.2 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-6FG484I	6864	1.2 V	-6	Halogen-Free fpBGA	484	IND



Date	Version	Section	Change Summary			
December 2014	December 2014 2.9 Introduction		Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Removed XO2-4000U data. — Removed 400-ball ftBGA. — Removed 25-ball WLCSP value for XO2-2000U.			
P		DC and Switching Characteristics	Updated the Recommended Operating Conditions section. Adjusted Max. values for $V_{CC}$ and $V_{CCIO}$			
			Updated the sysIO Recommended Operating Conditions section. Adjusted Max. values for LVCMOS 3.3, LVTTL, PCI, LVDS33 and LVPECL.			
		Pinout Information	Updated the Pinout Information Summary section. Removed MachXO2-4000U.			
		Ordering Information	Updated the MachXO2 Part Number Description section. Removed BG400 package.			
			Updated the High-Performance Commercial Grade Devices with Volt- age Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.			
			Updated the High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.			
November 2014 2.8	Introduction	Updated the Features section. — Revised I/Os under Flexible Logic Architecture. — Revised standby power under Ultra Low Power Devices. — Revise input frequency range under Flexible On-Chip Clocking.				
		Updated Table 1-1, MachXO2 Family Selection Guide. — Added XO2-4000U data. — Removed HE and ZE device options for XO2-4000. — Added 400-ball ftBGA.				
	Pinout Information	Updated the Pinout Information Summary section. Added MachXO2- 4000U caBGA400 and MachXO2-7000 caBGA400.				
		Ordering Information	Updated the MachXO2 Part Number Description section. Added BG400 package.			
			Updated the Ordering Information section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400 part numbers.			
October 2014	2.7	Ordering Information	Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Fixed typo in LCMXO2-2000ZE- 1UWG49ITR part number package.			
	Architecture	Updated the Supported Standards section. Added MIPI information to Table 2-12. Supported Input Standards and Table 2-13. Supported Output Standards.				
	DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition.				
			Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition.			
			Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.			
July 2014 2.6 DC and Switch Characteristic Ordering Inform		DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics <sup>1, 2</sup> section. Updated footnote 4.			
			Updated Register-to-Register Performance section. Updated foot- note.			
		Ordering Information	Updated UW49 package to UWG49 in MachXO2 Part Number Description.			
			Updated LCMXO2-2000ZE-1UWG49CTR package in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging.			