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**Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

**Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

## Details

| | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 264 |
| Number of Logic Elements/Cells | 2112 |
| Total RAM Bits | 75776 |
| Number of I/O | 40 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 49-UFBGA, WLCSP |
| Supplier Device Package | 49-WLCSP (3.11x3.19) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-2000ze-1uwg49itr |

## Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

### Logic Mode
In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

### Ripple Mode
Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit

- Subtraction 2-bit

- Add/subtract 2-bit using dynamic control

- Up counter 2-bit

- Down counter 2-bit

- Up/down counter with asynchronous clear

- Up/down counter with preload (sync)

- Ripple mode multiplier building block

- Multiplier support

- Comparator functions of A and B inputs
  — A greater-than-or-equal-to B
  — A not-equal-to B
  — A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

## RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO2 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO2 devices, please see TN1201, Memory Usage Guide for MachXO2 Devices.

*Table 2-3. Number of Slices Required For Implementing Distributed RAM*

|  | SPR 16x4 | PDPR 16x4 |
|---|---|---|
| Number of slices | 3 | 3 |

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

*Figure 2-6. Secondary High Fanout Nets for MachXO2 Devices*
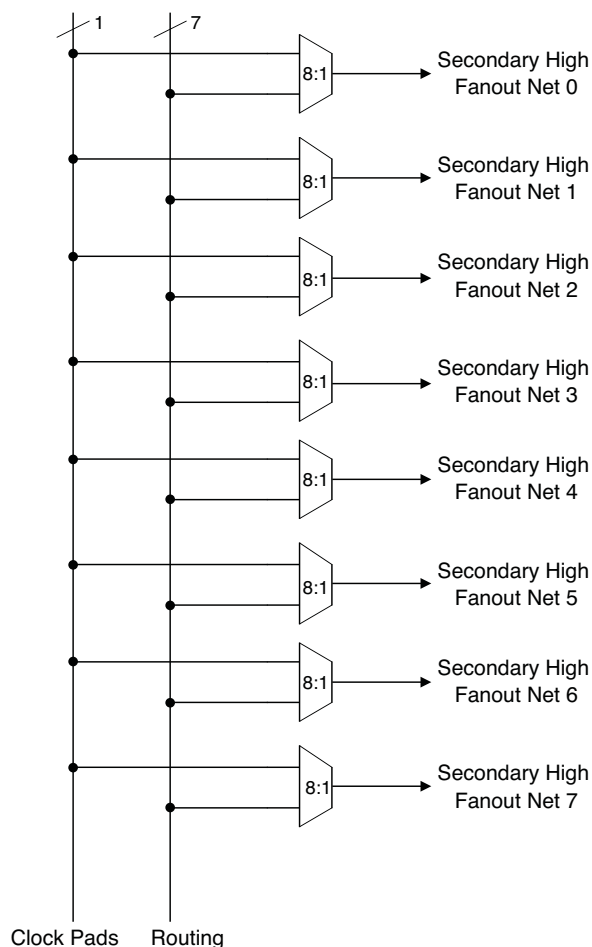


## sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The MachXO2-640U, MachXO2-1200/U and larger devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO2 sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO2 clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.

*Table 2-4. PLL Signal Descriptions (Continued)*

| Port Name | I/O | Description |
|---|---|---|
| CLKOP | O | Primary PLL output clock (with phase shift adjustment) |
| CLKOS | O | Secondary PLL output clock (with phase shift adjust) |
| CLKOS2 | O | Secondary PLL output clock2 (with phase shift adjust) |
| CLKOS3 | O | Secondary PLL output clock3 (with phase shift adjust) |
| LOCK | O | PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feedback signals. |
| DPHSRC | O | Dynamic Phase source – ports or WISHBONE is active |
| STDBY | I | Standby signal to power down the PLL |
| RST | I | PLL reset without resetting the M-divider. Active high reset. |
| RESETM | I | PLL reset - includes resetting the M-divider. Active high reset. |
| RESETC | I | Reset for CLKOS2 output divider only. Active high reset. |
| RESETD | I | Reset for CLKOS3 output divider only. Active high reset. |
| ENCLKOP | I | Enable PLL output CLKOP |
| ENCLKOS | I | Enable PLL output CLKOS when port is active |
| ENCLKOS2 | I | Enable PLL output CLKOS2 when port is active |
| ENCLKOS3 | I | Enable PLL output CLKOS3 when port is active |
| PLLCLK | I | PLL data bus clock input signal |
| PLLRST | I | PLL data bus reset. This resets only the data bus not any register values. |
| PLLSTB | I | PLL data bus strobe signal |
| PLLWE | I | PLL data bus write enable signal |
| PLLADDR [4:0] | I | PLL data bus address |
| PLLDATI [7:0] | I | PLL data bus data input |
| PLLDATO [7:0] | O | PLL data bus data output |
| PLLACK | O | PLL data bus acknowledge signal |

# sysMEM Embedded Block RAM Memory

The MachXO2-640/U and larger devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

**sysMEM Memory Block**
The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.

*Table 2-5. sysMEM Block Configurations*

| Memory Mode | Configurations |
|---|---|
| Single Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9 |
| True Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9 |
| Pseudo Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |
| FIFO | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |

**Bus Size Matching**
All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

**RAM Initialization and ROM Operation**
If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO2 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

**Memory Cascading**
Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

**Single, Dual, Pseudo-Dual Port and FIFO Modes**
Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.

3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

**FIFO Configuration**
The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

*Table 2-7. Programmable FIFO Flag Ranges*

| Flag Name | Programming Range |
|---|---|
| Full (FF) | 1 to max (up to $2^N$-1) |
| Almost Full (AF) | 1 to Full-1 |
| Almost Empty (AE) | 1 to Full-1 |
| Empty (EF) | 0 |

N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

**Memory Core Reset**
The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

## Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO2 devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO2 devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

The MachXO2-640U, MachXO2-1200/U and higher density devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these higher density devices have on-chip differential termination and also provide PCI support.

# PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

*Table 2-8. PIO Signal List*

| Pin Name | I/O Type | Description |
|---|---|---|
| CE | Input | Clock Enable |
| D | Input | Pin input from sysIO buffer. |
| INDD | Output | Register bypassed input. |
| INCK | Output | Clock input |
| Q0 | Output | DDR positive edge input |
| Q1 | Output | Registered input/DDR negative edge input |
| D0 | Input | Output signal from the core (SDR and DDR) |
| D1 | Input | Output signal from the core (DDR) |
| TD | Input | Tri-state signal from the core |
| Q | Output | Data output signals to sysIO Buffer |
| TQ | Output | Tri-state output signals to sysIO Buffer |
| DQSR90[1] | Input | DQS shift 90-degree read clock |
| DQSW90[1] | Input | DQS shift 90-degree write clock |
| DDRCLKPOL[1] | Input | DDR input register polarity control signal from DQS |
| SCLK | Input | System clock for input and output/tri-state blocks. |
| RST | Input | Local set reset signal |

1. Available in PIO on right edge only.

## Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition to this functionality, the input register blocks for the PIOs on the right edge include built-in logic to interface to DDR memory.

Figure 2-12 shows the input register block for the PIOs located on the left, top and bottom edges. Figure 2-13 shows the input register block for the PIOs on the right edge.

**Left, Top, Bottom Edges**
Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

## DDR Memory Support

Certain PICs on the right edge of MachXO2-640U, MachXO2-1200/U and larger devices, have additional circuitry to allow the implementation of DDR memory interfaces. There are two groups of 14 or 12 PIOs each on the right edge with additional circuitry to implement DDR memory interfaces. This capability allows the implementation of up to 16-bit wide memory interfaces. One PIO from each group contains a control element, the DQS Read/Write Block, to facilitate the generation of clock and control signals (DQSR90, DQSW90, DDRCLKPOL and DATAVALID). These clock and control signals are distributed to the other PIO in the group through dedicated low skew routing.

## DQS Read Write Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Read Write block provides the required clock alignment for DDR memory interfaces. DQSR90 and DQSW90 signals are generated by the DQS Read Write block from the DQS input.

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the read cycle) is unknown. The MachXO2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This circuit changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each read cycle for the correct clock polarity. Prior to the read operation in DDR memories, DQS is in tri-state (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit in the DQS Read Write block detects the first DQS rising edge after the preamble state and generates the DDRCLKPOL signal. This signal is used to control the polarity of the clock to the synchronizing registers.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration signals (6-bit bus) from a DLL on the right edge of the device. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, PCI, SSTL, HSTL, LVDS, BLVDS, MLVDS and LVPECL.

Each bank is capable of supporting multiple I/O standards. In the MachXO2 devices, single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS and PCI), differential (LVDS) and referenced input buffers (SSTL and HSTL) are powered using I/O supply voltage ($V_{CCIO}$). Each sysIO bank has its own $V_{CCIO}$. In addition, each bank has a voltage reference, $V_{REF}$, which allows the use of referenced input buffers independent of the bank $V_{CCIO}$.

MachXO2-256 and MachXO2-640 devices contain single-ended ratioed input buffers and single-ended output buffers with complementary outputs on all the I/O banks. Note that the single-ended input buffers on these devices do not contain PCI clamps. In addition to the single-ended I/O buffers these two devices also have differential and referenced input buffers on all I/Os. The I/Os are arranged in pairs, the two pads in the pair are described as "T" and "C", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

*Table 2-13. Supported Output Standards*

| Output Standard | $V_{CCIO}$ (Typ.) |
|---|---|
| **Single-Ended Interfaces** | |
| LVTTL | 3.3 |
| LVCMOS33 | 3.3 |
| LVCMOS25 | 2.5 |
| LVCMOS18 | 1.8 |
| LVCMOS15 | 1.5 |
| LVCMOS12 | 1.2 |
| LVCMOS33, Open Drain | — |
| LVCMOS25, Open Drain | — |
| LVCMOS18, Open Drain | — |
| LVCMOS15, Open Drain | — |
| LVCMOS12, Open Drain | — |
| PCI33 | 3.3 |
| SSTL25 (Class I) | 2.5 |
| SSTL18 (Class I) | 1.8 |
| HSTL18(Class I) | 1.8 |
| **Differential Interfaces** | |
| LVDS[1, 2] | 2.5, 3.3 |
| BLVDS, MLVDS, RSDS [2] | 2.5 |
| LVPECL[2] | 3.3 |
| MIPI[2] | 2.5 |
| Differential SSTL18 | 1.8 |
| Differential SSTL25 | 2.5 |
| Differential HSTL18 | 1.8 |

1. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.

## sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO2-1200U, MachXO2-2000/U and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO2-1200 and lower density devices have four banks (one bank per side). Figures 2-18 and 2-19 show the sysIO banks and their associated supplies for all devices.

# Hot Socketing

The MachXO2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO2 ideal for many multiple power supply and hot-swap applications.

# On-chip Oscillator

Every MachXO2 device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

1.  Device powers up with a nominal MCLK frequency of 2.08 MHz.

2.  During configuration, users select a different master clock frequency.

3.  The MCLK frequency changes to the selected frequency once the clock configuration bits are received.

4.  If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-14 lists all the available MCLK frequencies.

*Table 2-14. Available MCLK Frequencies*

| MCLK (MHz, Nominal) | MCLK (MHz, Nominal) | MCLK (MHz, Nominal) |
|:---:|:---:|:---:|
| 2.08 (default) | 9.17 | 33.25 |
| 2.46 | 10.23 | 38 |
| 3.17 | 13.3 | 44.33 |
| 4.29 | 14.78 | 53.2 |
| 5.54 | 20.46 | 66.5 |
| 7 | 26.6 | 88.67 |
| 8.31 | 29.56 | 133 |

# Embedded Hardened IP Functions and User Flash Memory

All MachXO2 devices provide embedded hardened functions such as SPI, I²C and Timer/Counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2-20.
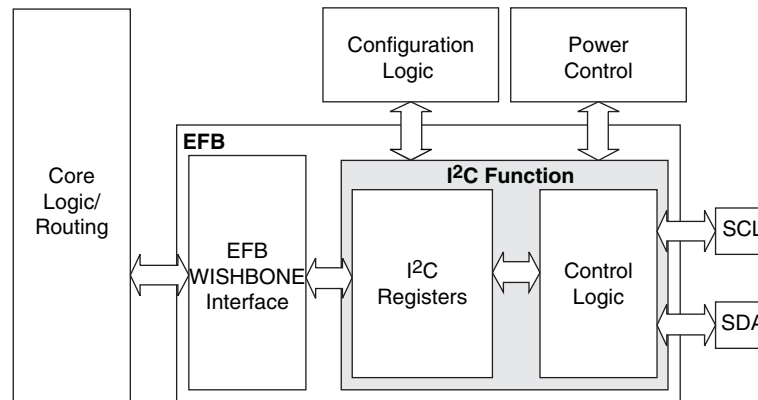
*Figure 2-21. I²C Core Block Diagram*



Table 2-15 describes the signals interfacing with the I²C cores.

*Table 2-15. I²C Core Signal Description*

| Signal Name | I/O | Description |
|---|---|---|
| i2c_scl | Bi-directional | Bi-directional clock line of the I²C core. The signal is an output if the I²C core is in master mode. The signal is an input if the I²C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device. |
| i2c_sda | Bi-directional | Bi-directional data line of the I²C core. The signal is an output when data is transmitted from the I²C core. The signal is an input when data is received into the I²C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device. |
| i2c_irqo | Output | Interrupt request output signal of the I²C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I²C register definitions. |
| cfg_wake | Output | Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, I²C Tab. |
| cfg_stdby | Output | Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, I²C Tab. |

## Hardened SPI IP Core

Every MachXO2 device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO2 devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface

# DC Electrical Characteristics

## Over Recommended Operating Conditions

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1, 4] | Input or I/O Leakage | Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX) | — | — | +175 | μA |
| | | Clamp OFF and $V_{IN} = V_{CCIO}$ | −10 | — | 10 | μA |
| | | Clamp OFF and $V_{CCIO}$ −0.97 V < $V_{IN}$ < $V_{CCIO}$ | −175 | — | — | μA |
| | | Clamp OFF and 0 V < $V_{IN}$ < $V_{CCIO}$ −0.97 V | — | — | 10 | μA |
| | | Clamp OFF and $V_{IN}$ = GND | — | — | 10 | μA |
| | | Clamp ON and 0 V < $V_{IN}$ < $V_{CCIO}$ | — | — | 10 | μA |
| $I_{PU}$ | I/O Active Pull-up Current | 0 < $V_{IN}$ < 0.7 $V_{CCIO}$ | −30 | — | -309 | μA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX) < $V_{IN}$ < $V_{CCIO}$ | 30 | — | 305 | μA |
| $I_{BHLS}$ | Bus Hold Low sustaining current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | μA |
| $I_{BHHS}$ | Bus Hold High sustaining current | $V_{IN} = 0.7V_{CCIO}$ | −30 | — | — | μA |
| $I_{BHLO}$ | Bus Hold Low Overdrive current | $0 \leq V_{IN} \leq V_{CCIO}$ | — | — | 305 | μA |
| $I_{BHHO}$ | Bus Hold High Overdrive current | $0 \leq V_{IN} \leq V_{CCIO}$ | — | — | −309 | μA |
| $V_{BHT}$[3] | Bus Hold Trip Points | | $V_{IL}$ (MAX) | — | $V_{IH}$ (MIN) | V |
| C1 | I/O Capacitance[2] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, $V_{CC}$ = Typ., $V_{IO}$ = 0 to $V_{IH}$ (MAX) | 3 | 5 | 9 | pF |
| C2 | Dedicated Input Capacitance[2] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, $V_{CC}$ = Typ., $V_{IO}$ = 0 to $V_{IH}$ (MAX) | 3 | 5.5 | 7 | pF |
| $V_{HYST}$ | Hysteresis for Schmitt Trigger Inputs[5] | $V_{CCIO}$ = 3.3 V, Hysteresis = Large | — | 450 | — | mV |
| | | $V_{CCIO}$ = 2.5 V, Hysteresis = Large | — | 250 | — | mV |
| | | $V_{CCIO}$ = 1.8 V, Hysteresis = Large | — | 125 | — | mV |
| | | $V_{CCIO}$ = 1.5 V, Hysteresis = Large | — | 100 | — | mV |
| | | $V_{CCIO}$ = 3.3 V, Hysteresis = Small | — | 250 | — | mV |
| | | $V_{CCIO}$ = 2.5 V, Hysteresis = Small | — | 150 | — | mV |
| | | $V_{CCIO}$ = 1.8 V, Hysteresis = Small | — | 60 | — | mV |
| | | $V_{CCIO}$ = 1.5 V, Hysteresis = Small | — | 40 | — | mV |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. $T_A$ 25 °C, f = 1.0 MHz.
3. Please refer to $V_{IL}$ and $V_{IH}$ in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. When $V_{IH}$ is higher than $V_{CCIO}$, a transient current typically of 30 ns in duration or less with a peak current of 6 mA can occur on the high-to-low transition. For true LVDS output pins in MachXO2-640U, MachXO2-1200/U and larger devices, $V_{IH}$ must be less than or equal to $V_{CCIO}$.
5. With bus keeper circuit turned on. For more details, refer to TN1202, MachXO2 sysIO Usage Guide.

| Parameter | Description | Device | −3 Min. | −3 Max. | −2 Min. | −2 Max. | −1 Min. | −1 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{SU\_DEL}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-256ZE | 2.62 | — | 2.91 | — | 3.14 | — | ns |
| | | MachXO2-640ZE | 2.56 | — | 2.85 | — | 3.08 | — | ns |
| | | MachXO2-1200ZE | 2.30 | — | 2.57 | — | 2.79 | — | ns |
| | | MachXO2-2000ZE | 2.25 | — | 2.50 | — | 2.70 | — | ns |
| | | MachXO2-4000ZE | 2.39 | — | 2.60 | — | 2.76 | — | ns |
| | | MachXO2-7000ZE | 2.17 | — | 2.33 | — | 2.43 | — | ns |
| $t_{H\_DEL}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-256ZE | −0.44 | — | −0.44 | — | −0.44 | — | ns |
| | | MachXO2-640ZE | −0.43 | — | −0.43 | — | −0.43 | — | ns |
| | | MachXO2-1200ZE | −0.28 | — | −0.28 | — | −0.28 | — | ns |
| | | MachXO2-2000ZE | −0.31 | — | −0.31 | — | −0.31 | — | ns |
| | | MachXO2-4000ZE | −0.34 | — | −0.34 | — | −0.34 | — | ns |
| | | MachXO2-7000ZE | −0.21 | — | −0.21 | — | −0.21 | — | ns |
| $f_{MAX\_IO}$ | Clock Frequency of I/O and PFU Register | All MachXO2 devices | — | 150 | — | 125 | — | 104 | MHz |
| **General I/O Pin Parameters (Using Edge Clock without PLL)** | | | | | | | | | |
| $t_{COE}$ | Clock to Output – PIO Output Register | MachXO2-1200ZE | — | 11.10 | — | 11.51 | — | 11.91 | ns |
| | | MachXO2-2000ZE | — | 11.10 | — | 11.51 | — | 11.91 | ns |
| | | MachXO2-4000ZE | — | 10.89 | — | 11.28 | — | 11.67 | ns |
| | | MachXO2-7000ZE | — | 11.10 | — | 11.51 | — | 11.91 | ns |
| $t_{SUE}$ | Clock to Data Setup – PIO Input Register | MachXO2-1200ZE | −0.23 | — | −0.23 | — | −0.23 | — | ns |
| | | MachXO2-2000ZE | −0.23 | — | −0.23 | — | −0.23 | — | ns |
| | | MachXO2-4000ZE | −0.15 | — | −0.15 | — | −0.15 | — | ns |
| | | MachXO2-7000ZE | −0.23 | — | −0.23 | — | −0.23 | — | ns |
| $t_{HE}$ | Clock to Data Hold – PIO Input Register | MachXO2-1200ZE | 3.81 | — | 4.11 | — | 4.52 | — | ns |
| | | MachXO2-2000ZE | 3.81 | — | 4.11 | — | 4.52 | — | ns |
| | | MachXO2-4000ZE | 3.60 | — | 3.89 | — | 4.28 | — | ns |
| | | MachXO2-7000ZE | 3.81 | — | 4.11 | — | 4.52 | — | ns |
| $t_{SU\_DELE}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-1200ZE | 2.78 | — | 3.11 | — | 3.40 | — | ns |
| | | MachXO2-2000ZE | 2.78 | — | 3.11 | — | 3.40 | — | ns |
| | | MachXO2-4000ZE | 3.11 | — | 3.48 | — | 3.79 | — | ns |
| | | MachXO2-7000ZE | 2.94 | — | 3.30 | — | 3.60 | — | ns |
| $t_{H\_DELE}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-1200ZE | −0.29 | — | -0.29 | — | −0.29 | — | ns |
| | | MachXO2-2000ZE | −0.29 | — | -0.29 | — | −0.29 | — | ns |
| | | MachXO2-4000ZE | −0.46 | — | -0.46 | — | −0.46 | — | ns |
| | | MachXO2-7000ZE | −0.37 | — | -0.37 | — | −0.37 | — | ns |
| **General I/O Pin Parameters (Using Primary Clock with PLL)** | | | | | | | | | |
| $t_{COPLL}$ | Clock to Output – PIO Output Register | MachXO2-1200ZE | — | 7.95 | — | 8.07 | — | 8.19 | ns |
| | | MachXO2-2000ZE | — | 7.97 | — | 8.10 | — | 8.22 | ns |
| | | MachXO2-4000ZE | — | 7.98 | — | 8.10 | — | 8.23 | ns |
| | | MachXO2-7000ZE | — | 8.02 | — | 8.14 | — | 8.26 | ns |
| $t_{SUPLL}$ | Clock to Data Setup – PIO Input Register | MachXO2-1200ZE | 0.85 | — | 0.85 | — | 0.89 | — | ns |
| | | MachXO2-2000ZE | 0.84 | — | 0.84 | — | 0.86 | — | ns |
| | | MachXO2-4000ZE | 0.84 | — | 0.84 | — | 0.85 | — | ns |
| | | MachXO2-7000ZE | 0.83 | — | 0.83 | — | 0.81 | — | ns |

*Figure 3-5. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms*

RX CLK Input
or DQS Input

RX Data Input
or DQ Input

RX.Aligned    $t_{DVA}$ or $t_{DVADQ}$

$t_{DVE}$ or $t_{DVEDQ}$
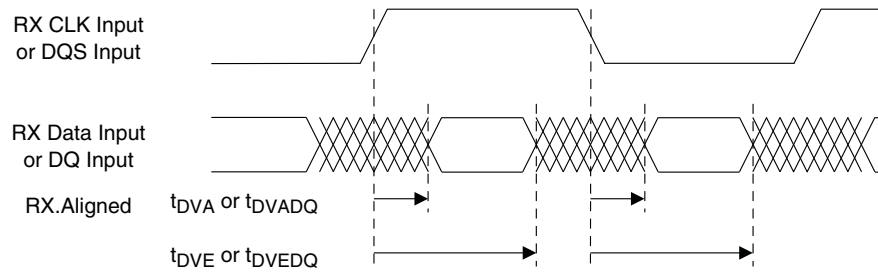
*Figure 3-6. Receiver RX.CLK.Centered Waveforms*

RX CLK Input

RX Data Input

RX.Centered

$t_{SU}$   $t_{HO}$      $t_{SU}$   $t_{HO}$
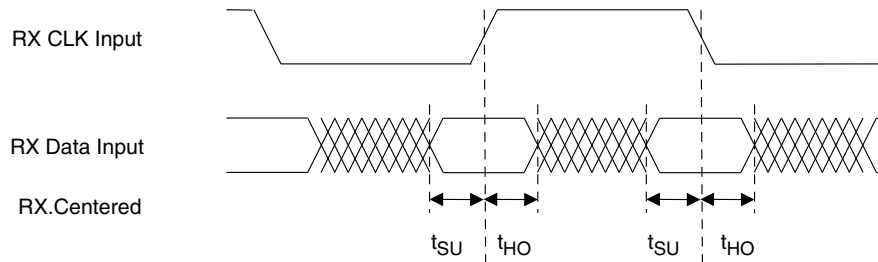
*Figure 3-7. Transmitter TX.CLK.Aligned Waveforms*

TX CLK Output

TX Data Output

TX.Aligned

$t_{DIB}$   $t_{DIA}$      $t_{DIB}$   $t_{DIA}$
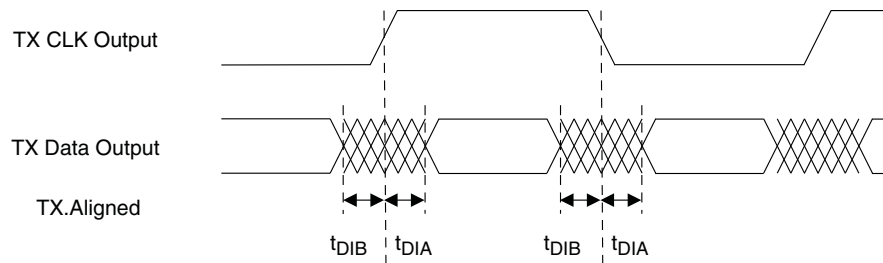
*Figure 3-8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms*

TX CLK Output
or DQS Output

TX Data Output
or DQ Output

TX.Centered

$t_{DVB}$ or      $t_{DVA}$ or      $t_{DVB}$ or      $t_{DVA}$ or
$t_{DQVBS}$      $t_{DQVAS}$      $t_{DQVBS}$      $t_{DQVAS}$
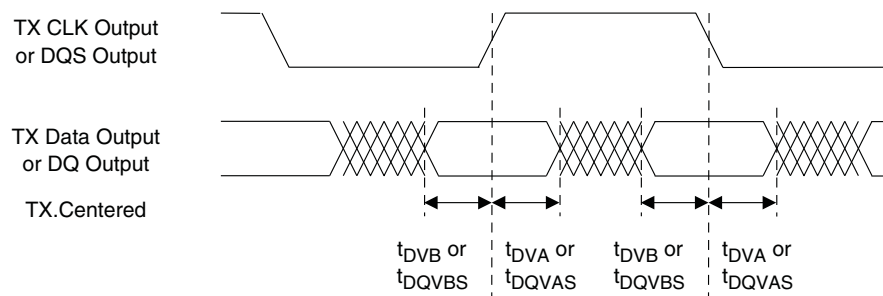
# sysCLOCK PLL Timing (Continued)

## Over Recommended Operating Conditions

| Parameter | Descriptions | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| t$_{ROTATE\_WD}$ | PHASESTEP Pulse Width | | 4 | — | VCO Cycles |

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t$_{LOCK}$ for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide for more details.
5. At minimum f$_{PFD}$. As the f$_{PFD}$ increases the time will decrease to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

# I²C Port Timing Specifications[1, 2]

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $f_{MAX}$ | Maximum SCL clock frequency | — | 400 | kHz |

1. MachXO2 supports the following modes:
    • Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
    • Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
2. Refer to the I²C specification for timing requirements.

# SPI Port Timing Specifications[1]

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $f_{MAX}$ | Maximum SCK clock frequency | — | 45 | MHz |

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

# Switching Test Conditions

Figure 3-13 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-5.

*Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards*
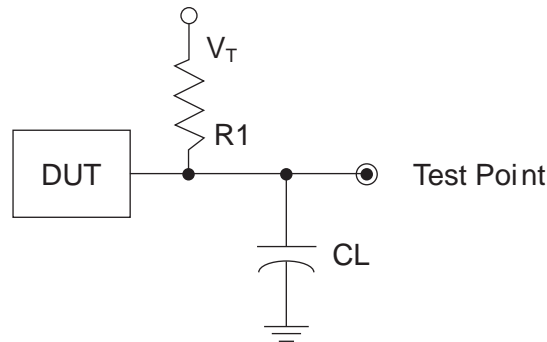


*Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces*

| Test Condition | R1 | CL | Timing Ref. | VT |
|---|---|---|---|---|
| LVTTL and LVCMOS settings (L -> H, H -> L) | ∞ | 0pF | LVTTL, LVCMOS 3.3 = 1.5 V | — |
| | | | LVCMOS 2.5 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.8 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.5 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.2 = $V_{CCIO}/2$ | — |
| LVTTL and LVCMOS 3.3 (Z -> H) | 188 | 0pF | 1.5 V | $V_{OL}$ |
| LVTTL and LVCMOS 3.3 (Z -> L) | | | 1.5 V | $V_{OH}$ |
| Other LVCMOS (Z -> H) | | | $V_{CCIO}/2$ | $V_{OL}$ |
| Other LVCMOS (Z -> L) | | | $V_{CCIO}/2$ | $V_{OH}$ |
| LVTTL + LVCMOS (H -> Z) | | | $V_{OH} - 0.15$ V | $V_{OL}$ |
| LVTTL + LVCMOS (L -> Z) | | | $V_{OL} - 0.15$ V | $V_{OH}$ |

*Note: Output test conditions for all other interfaces are determined by the respective standards.*

## MachXO2 Part Number Description

LCMXO2 – XXXX X X X – X XXXXXX X XX XX

**Device Family**
   MachXO2 PLD

**Logic Capacity**
   256 = 256 LUTs
   640 = 640 LUTs
   1200 = 1280 LUTs
   2000 = 2112 LUTs
   4000 = 4320 LUTs
   7000 = 6864 LUTs

**I/O Count**
   Blank = Standard Device
   U = Ultra High I/O Device

**Power/Performance**
   Z = Low Power
   H = High Performance

**Supply Voltage**
   C = 2.5 V / 3.3 V
   E = 1.2 V

**Speed**
   1 = Slowest  ⎫
   2            ⎬ Low Power
   3 = Fastest  ⎭

   4 = Slowest  ⎫
   5            ⎬ High Performance
   6 = Fastest  ⎭

**Device Status**
   Blank = Production Device
   ES = Engineering Sample
   R1 = Production Release 1 Device
   1K = WLCSP Package, 1,000 parts per reel

**Shipping Method**
   Blank = Trays
   TR = Tape and Reel

**Grade**
   C = Commercial
   I = Industrial

**Package**

   UWG25  = 25-Ball Halogen-Free WLCSP
              (0.4 mm Pitch)
   SG32   = 32-Pin Halogen-Free QFN
              (0.5 mm Pitch)
   SG48   = 48-Pin Halogen-Free QFN
              (0.5 mm Pitch)
   UWG49  = 49-ball Halogen-Free WLCSP
              (0.4 mm Pitch)
   UMG64  = 64-Ball Halogen-Free ucBGA
              (0.4 mm Pitch)
   QN84   = 84-Pin Halogen-Free QFN
              (0.5 mm Pitch)
   TG100  = 100-Pin Halogen-Free TQFP
   TG144  = 144-Pin Halogen-Free TQFP
   MG132  = 132-Ball Halogen-Free csBGA
              (0.5 mm Pitch)
   MG184  = 184-Ball Halogen-Free csBGA
              (0.5 mm Pitch)
   BG256  = 256-Ball Halogen-Free caBGA
              (0.8 mm Pitch)
   FTG256 = 256-Ball Halogen-Free ftBGA
              (1.0 mm Pitch)
   BG332  = 332-Ball Halogen-Free caBGA
              (0.8 mm Pitch)
   FG484  = 484-Ball Halogen-Free fpBGA
              (1.0 mm Pitch)

   * 48-pin QFN information is 'Advanced'.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000ZE-1TG100C | 2112 | 1.2 V | −1 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000ZE-2TG100C | 2112 | 1.2 V | −2 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000ZE-3TG100C | 2112 | 1.2 V | −3 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000ZE-1MG132C | 2112 | 1.2 V | −1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000ZE-2MG132C | 2112 | 1.2 V | −2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000ZE-3MG132C | 2112 | 1.2 V | −3 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000ZE-1TG144C | 2112 | 1.2 V | −1 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000ZE-2TG144C | 2112 | 1.2 V | −2 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000ZE-3TG144C | 2112 | 1.2 V | −3 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000ZE-1BG256C | 2112 | 1.2 V | −1 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000ZE-2BG256C | 2112 | 1.2 V | −2 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000ZE-3BG256C | 2112 | 1.2 V | −3 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000ZE-1FTG256C | 2112 | 1.2 V | −1 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000ZE-2FTG256C | 2112 | 1.2 V | −2 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000ZE-3FTG256C | 2112 | 1.2 V | −3 | Halogen-Free ftBGA | 256 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000ZE-1QN84C | 4320 | 1.2 V | −1 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000ZE-2QN84C | 4320 | 1.2 V | −2 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000ZE-3QN84C | 4320 | 1.2 V | −3 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000ZE-1MG132C | 4320 | 1.2 V | −1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000ZE-2MG132C | 4320 | 1.2 V | −2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000ZE-3MG132C | 4320 | 1.2 V | −3 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000ZE-1TG144C | 4320 | 1.2 V | −1 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000ZE-2TG144C | 4320 | 1.2 V | −2 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000ZE-3TG144C | 4320 | 1.2 V | −3 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000ZE-1BG256C | 4320 | 1.2 V | −1 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000ZE-2BG256C | 4320 | 1.2 V | −2 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000ZE-3BG256C | 4320 | 1.2 V | −3 | Halogen-Free caBGA | 256 | COM. |
| LCMXO2-4000ZE-1FTG256C | 4320 | 1.2 V | −1 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000ZE-2FTG256C | 4320 | 1.2 V | −2 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000ZE-3FTG256C | 4320 | 1.2 V | −3 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000ZE-1BG332C | 4320 | 1.2 V | −1 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000ZE-2BG332C | 4320 | 1.2 V | −2 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000ZE-3BG332C | 4320 | 1.2 V | −3 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000ZE-1FG484C | 4320 | 1.2 V | −1 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000ZE-2FG484C | 4320 | 1.2 V | −2 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000ZE-3FG484C | 4320 | 1.2 V | −3 | Halogen-Free fpBGA | 484 | COM |

## High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-256HC-4SG32C | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256HC-5SG32C | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256HC-6SG32C | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256HC-4SG48C | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 48 | COM |
| LCMXO2-256HC-5SG48C | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 48 | COM |
| LCMXO2-256HC-6SG48C | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 48 | COM |
| LCMXO2-256HC-4UMG64C | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256HC-5UMG64C | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256HC-6UMG64C | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256HC-4TG100C | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256HC-5TG100C | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256HC-6TG100C | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256HC-4MG132C | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-256HC-5MG132C | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-256HC-6MG132C | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640HC-4SG48C | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 48 | COM |
| LCMXO2-640HC-5SG48C | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 48 | COM |
| LCMXO2-640HC-6SG48C | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 48 | COM |
| LCMXO2-640HC-4TG100C | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640HC-5TG100C | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640HC-6TG100C | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640HC-4MG132C | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-640HC-5MG132C | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-640HC-6MG132C | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640UHC-4TG144C | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-640UHC-5TG144C | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-640UHC-6TG144C | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| January 2013 | 02.0 | Introduction | Updated the total number IOs to include JTAGENB. |
| | | Architecture | Supported Output Standards table – Added 3.3 $V_{CCIO}$ (Typ.) to LVDS row. |
| | | | Changed SRAM CRC Error Detection to Soft Error Detection. |
| | | DC and Switching Characteristics | Power Supply Ramp Rates table – Updated Units column for $t_{RAMP}$ symbol. |
| | | | Added new Maximum sysIO Buffer Performance table. |
| | | | sysCLOCK PLL Timing table – Updated Min. column values for $f_{IN}$, $f_{OUT}$, $f_{OUT2}$ and $f_{PFD}$ parameters. Added $t_{SPO}$ parameter. Updated footnote 6. |
| | | | MachXO2 Oscillator Output Frequency table – Updated symbol name for $t_{STABLEOSC}$. |
| | | | DC Electrical Characteristics table – Updated conditions for $I_{IL}$, $I_{IH}$ symbols. |
| | | | Corrected parameters tDQVBS and tDQVAS |
| | | | Corrected MachXO2 ZE parameters tDVADQ and tDVEDQ |
| | | Pinout Information | Included the MachXO2-4000HE 184 csBGA package. |
| | | Ordering Information | Updated part number. |
| April 2012 | 01.9 | Architecture | Removed references to TN1200. |
| | | Ordering Information | Updated the Device Status portion of the MachXO2 Part Number Description to include the 50 parts per reel for the WLCSP package. |
| | | | Added new part number and footnote 2 for LCMXO2-1200ZE-1UWG25ITR50. |
| | | | Updated footnote 1 for LCMXO2-1200ZE-1UWG25ITR. |
| | | Supplemental Information | Removed references to TN1200. |
| March 2012 | 01.8 | Introduction | Added 32 QFN packaging information to Features bullets and MachXO2 Family Selection Guide table. |
| | | DC and Switching Characteristics | Changed 'STANDBY' to 'USERSTDBY' in Standby Mode timing diagram. |
| | | Pinout Information | Removed footnote from Pin Information Summary tables. |
| | | | Added 32 QFN package to Pin Information Summary table. |
| | | Ordering Information | Updated Part Number Description and Ordering Information tables for 32 QFN package. |
| | | | Updated topside mark diagram in the Ordering Information section. |