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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

### Details

Product Status	Active
Number of LABs/CLBs	264
Number of Logic Elements/Cells	2112
Total RAM Bits	75776
Number of I/O	40
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C
Package / Case	49-UFBGA, WLCSP
Supplier Device Package	49-WLCSP (3.11x3.19)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmx02-2000ze-1uwg49itr1k">https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmx02-2000ze-1uwg49itr1k</a>

## Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I<sup>2</sup>C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external V<sub>CC</sub> supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V<sub>CC</sub> supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis.

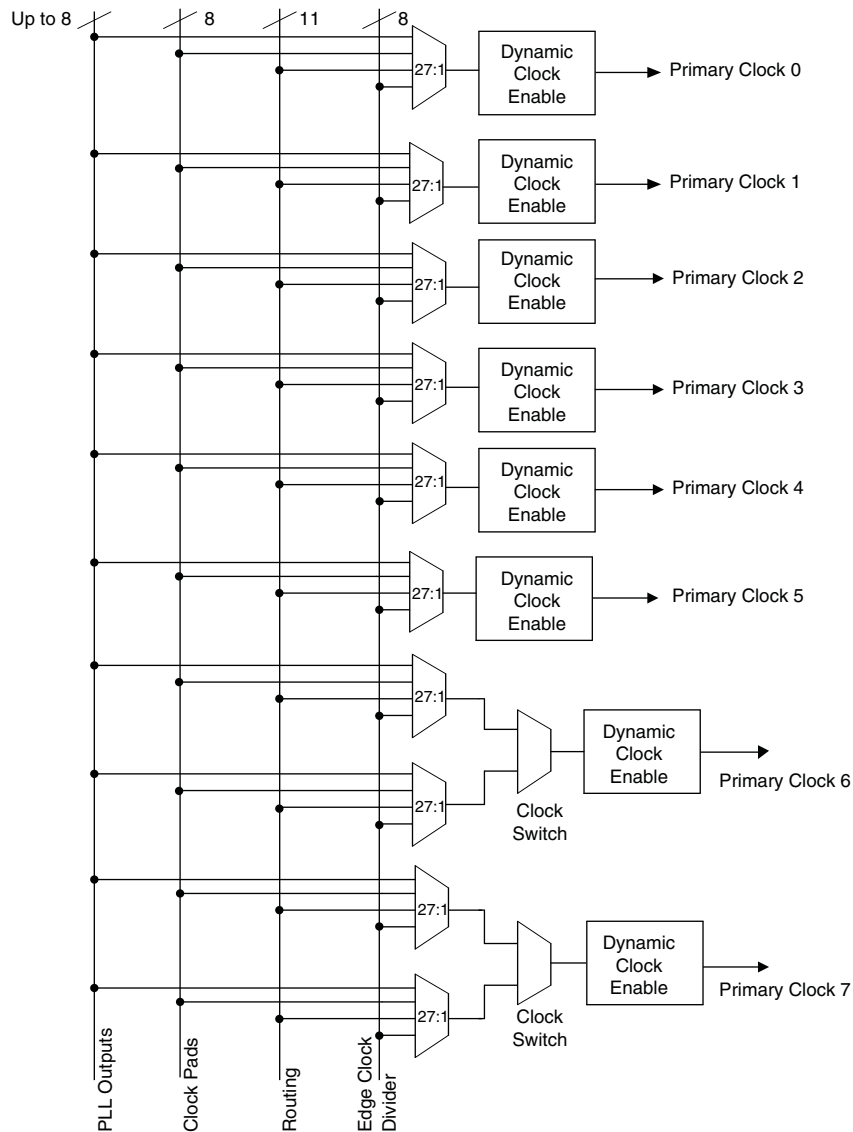
A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I<sup>2</sup>C port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

**Figure 2-5. Primary Clocks for MachXO2 Devices**



Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO2 External Switching Characteristics table.

**Table 2-4. PLL Signal Descriptions (Continued)**

Port Name	I/O	Description
CLKOP	O	Primary PLL output clock (with phase shift adjustment)
CLKOS	O	Secondary PLL output clock (with phase shift adjust)
CLKOS2	O	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	O	Secondary PLL output clock3 (with phase shift adjust)
LOCK	O	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feedback signals.
DPHSRC	O	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset - includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	O	PLL data bus data output
PLLACK	O	PLL data bus acknowledge signal

## sysMEM Embedded Block RAM Memory

The MachXO2-640/U and larger devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

### sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.

## PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

**Table 2-8. PIO Signal List**

Pin Name	I/O Type	Description
CE	Input	Clock Enable
D	Input	Pin input from sysIO buffer.
INDD	Output	Register bypassed input.
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysIO Buffer
TQ	Output	Tri-state output signals to sysIO Buffer
DQSR90 <sup>1</sup>	Input	DQS shift 90-degree read clock
DQSW90 <sup>1</sup>	Input	DQS shift 90-degree write clock
DDRCLKPOL <sup>1</sup>	Input	DDR input register polarity control signal from DQS
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

1. Available in PIO on right edge only.

### Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition to this functionality, the input register blocks for the PIOs on the right edge include built-in logic to interface to DDR memory.

Figure 2-12 shows the input register block for the PIOs located on the left, top and bottom edges. Figure 2-13 shows the input register block for the PIOs on the right edge.

#### Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

## Hot Socketing

The MachXO2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO2 ideal for many multiple power supply and hot-swap applications.

## On-chip Oscillator

Every MachXO2 device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
2. During configuration, users select a different master clock frequency.
3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-14 lists all the available MCLK frequencies.

**Table 2-14. Available MCLK Frequencies**

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

## Embedded Hardened IP Functions and User Flash Memory

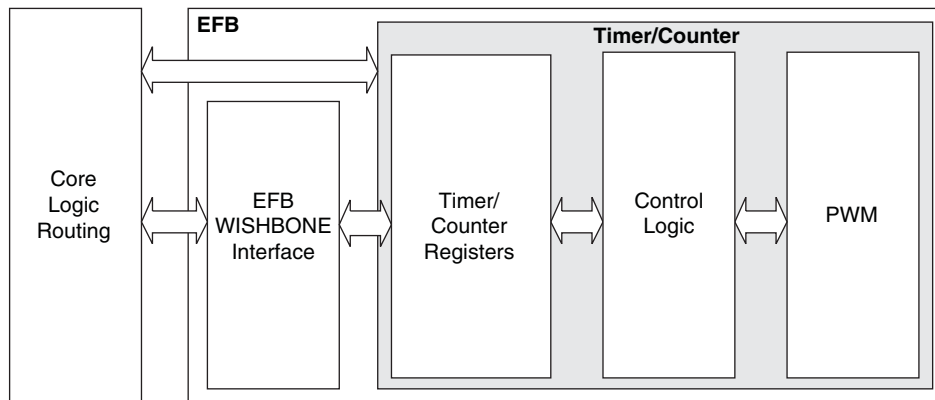
All MachXO2 devices provide embedded hardened functions such as SPI, I<sup>2</sup>C and Timer/Counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2-20.

## Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  - Watchdog timer
  - Clear timer on compare match
  - Fast PWM
  - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

**Figure 2-23. Timer/Counter Block Diagram**



**Table 2-17. Timer/Counter Signal Description**

Port	I/O	Description
tc_clk	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	O	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	O	Timer counter output signal

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## Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

### IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with  $V_{CCIO}$  Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, [Boundary Scan Testability with Lattice sysIO Capability](#) and TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#).

### Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I<sup>2</sup>C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

1. Internal Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I<sup>2</sup>C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, [MachXO2 Programming and Configuration Usage Guide](#) for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

### TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#) for details.



### Absolute Maximum Ratings<sup>1, 2, 3</sup>

	MachXO2 ZE/HE (1.2 V)	MachXO2 HC (2.5 V / 3.3 V)
Supply Voltage $V_{CC}$ . . . . .	-0.5 V to 1.32 V . . . . .	-0.5 V to 3.75 V . . . . .
Output Supply Voltage $V_{CCIO}$ . . . . .	-0.5 V to 3.75 V . . . . .	-0.5 V to 3.75 V . . . . .
I/O Tri-state Voltage Applied <sup>4, 5</sup> . . . . .	-0.5 V to 3.75 V . . . . .	-0.5 V to 3.75 V . . . . .
Dedicated Input Voltage Applied <sup>4</sup> . . . . .	-0.5 V to 3.75 V . . . . .	-0.5 V to 3.75 V . . . . .
Storage Temperature (Ambient) . . . . .	-55 °C to 125 °C . . . . .	-55 °C to 125 °C . . . . .
Junction Temperature ( $T_J$ ) . . . . .	-40 °C to 125 °C . . . . .	-40 °C to 125 °C . . . . .

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2 V to ( $V_{IHMAX} + 2$ ) volts is permitted for a duration of <20 ns.
5. The dual function I<sup>2</sup>C pins SCL and SDA are limited to -0.25 V to 3.75 V or to -0.3 V with a duration of <20 ns.

### Recommended Operating Conditions<sup>1</sup>

Symbol	Parameter	Min.	Max.	Units
$V_{CC}^1$	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V / 3.3 V Devices	2.375	3.6	V
$V_{CCIO}^{1, 2, 3}$	I/O Driver Supply Voltage	1.14	3.6	V
$t_{JCOM}$	Junction Temperature Commercial Operation	0	85	°C
$t_{JIND}$	Junction Temperature Industrial Operation	-40	100	°C

1. Like power supplies must be tied together. For example, if  $V_{CCIO}$  and  $V_{CC}$  are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3.  $V_{CCIO}$  pins of unused I/O banks should be connected to the  $V_{CC}$  power supply on boards.

### Power Supply Ramp Rates<sup>1</sup>

Symbol	Parameter	Min.	Typ.	Max.	Units
$t_{RAMP}$	Power supply ramp rates for all power supplies.	0.01	—	100	V/ms

1. Assumes monotonic ramp rates.

## Power-On-Reset Voltage Levels<sup>1, 2, 3, 4, 5</sup>

Symbol	Parameter	Min.	Typ.	Max.	Units
V <sub>PORUP</sub>	Power-On-Reset ramp up trip point (band gap based circuit monitoring V <sub>CCINT</sub> and V <sub>CCIO0</sub> )	0.9	—	1.06	V
V <sub>PORUPEXT</sub>	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V <sub>CC</sub> power supply)	1.5	—	2.1	V
V <sub>PORDNBG</sub>	Power-On-Reset ramp down trip point (band gap based circuit monitoring V <sub>CCINT</sub> )	0.75	—	0.93	V
V <sub>PORDNBGEXT</sub>	Power-On-Reset ramp down trip point (band gap based circuit monitoring V <sub>CC</sub> )	0.98	—	1.33	V
V <sub>PORDNSRAM</sub>	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V <sub>CCINT</sub> )	—	0.6	—	V
V <sub>PORDNSRAMEXT</sub>	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V <sub>CC</sub> )	—	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators V<sub>CCINT</sub> is the same as the V<sub>CC</sub> supply voltage. For devices with voltage regulators, V<sub>CCINT</sub> is regulated from the V<sub>CC</sub> supply voltage.
3. Note that V<sub>PORUP</sub> (min.) and V<sub>PORDNBG</sub> (max.) are in different process corners. For any given process corner V<sub>PORDNBG</sub> (max.) is always 12.0 mV below V<sub>PORUP</sub> (min.).
4. V<sub>PORUPEXT</sub> is for HC devices only. In these devices a separate POR circuit monitors the external V<sub>CC</sub> power supply.
5. V<sub>CCIO0</sub> does not have a Power-On-Reset ramp down trip point. V<sub>CCIO0</sub> must remain within the Recommended Operating Conditions to ensure proper operation.

## Programming/Erase Specifications

Symbol	Parameter	Min.	Max. <sup>1</sup>	Units
N <sub>PROGCYC</sub>	Flash Programming cycles per t <sub>RETENTION</sub>	—	10,000	Cycles
	Flash functional programming cycles	—	100,000	
t <sub>RETENTION</sub>	Data retention at 100 °C junction temperature	10	—	Years
	Data retention at 85 °C junction temperature	20	—	

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

## Hot Socketing Specifications<sup>1, 2, 3</sup>

Symbol	Parameter	Condition	Max.	Units
I <sub>DK</sub>	Input or I/O leakage Current	0 < V <sub>IN</sub> < V <sub>IH</sub> (MAX)	+/-1000	μA

1. Insensitive to sequence of V<sub>CC</sub> and V<sub>CCIO</sub>. However, assumes monotonic rise/fall rates for V<sub>CC</sub> and V<sub>CCIO</sub>.
2. 0 < V<sub>CC</sub> < V<sub>CC</sub> (MAX), 0 < V<sub>CCIO</sub> < V<sub>CCIO</sub> (MAX).
3. I<sub>DK</sub> is additive to I<sub>PU</sub>, I<sub>PD</sub> or I<sub>BH</sub>.

## ESD Performance

Please refer to the [MachXO2 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

## Typical Building Block Function Performance – HC/HE Devices<sup>1</sup>

### Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	-6 Timing	Units
<b>Basic Functions</b>		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

### Register-to-Register Performance

Function	-6 Timing	Units
<b>Basic Functions</b>		
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
<b>Embedded Memory Functions</b>		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
<b>Distributed Memory Functions</b>		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

## sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
$f_{IN}$	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
$f_{OUT}$	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)		1.5625	400	MHz
$f_{OUT2}$	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
$f_{VCO}$	PLL VCO Frequency		200	800	MHz
$f_{PFD}$	Phase Detector Input Frequency		7	400	MHz
<b>AC Characteristics</b>					
$t_{DT}$	Output Clock Duty Cycle	Without duty trim selected <sup>3</sup>	45	55	%
$t_{DT\_TRIM}^7$	Edge Duty Trim Accuracy		-75	75	%
$t_{PH}^4$	Output Phase Accuracy		-6	6	%
$t_{OPJIT}^{1,8}$	Output Clock Period Jitter	$f_{OUT} > 100$ MHz	—	150	ps p-p
		$f_{OUT} < 100$ MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	$f_{OUT} > 100$ MHz	—	180	ps p-p
		$f_{OUT} < 100$ MHz	—	0.009	UIPP
	Output Clock Phase Jitter	$f_{PFD} > 100$ MHz	—	160	ps p-p
		$f_{PFD} < 100$ MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	$f_{OUT} > 100$ MHz	—	230	ps p-p
		$f_{OUT} < 100$ MHz	—	0.12	UIPP
Output Clock Cycle-to-cycle Jitter (Fractional-N)	$f_{OUT} > 100$ MHz	—	230	ps p-p	
	$f_{OUT} < 100$ MHz	—	0.12	UIPP	
$t_{SPO}$	Static Phase Offset	Divider ratio = integer	-120	120	ps
$t_W$	Output Clock Pulse Width	At 90% or 10% <sup>3</sup>	0.9	—	ns
$t_{LOCK}^{2,5}$	PLL Lock-in Time		—	15	ms
$t_{UNLOCK}$	PLL Unlock Time		—	50	ns
$t_{IPJIT}^6$	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
$t_{HI}$	Input Clock High Time	90% to 90%	0.5	—	ns
$t_{LO}$	Input Clock Low Time	10% to 10%	0.5	—	ns
$t_{STABLE}^5$	STANDBY High to PLL Stable		—	15	ms
$t_{RST}$	RST/RESETM Pulse Width		1	—	ns
$t_{RSTREC}$	RST Recovery Time		1	—	ns
$t_{RST\_DIV}$	RESETC/D Pulse Width		10	—	ns
$t_{RSTREC\_DIV}$	RESETC/D Recovery Time		1	—	ns
$t_{ROTATE-SETUP}$	PHASESTEP Setup Time		10	—	ns

## I<sup>2</sup>C Port Timing Specifications<sup>1, 2</sup>

Symbol	Parameter	Min.	Max.	Units
f <sub>MAX</sub>	Maximum SCL clock frequency	—	400	kHz

- MachXO2 supports the following modes:
  - Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
  - Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
- Refer to the I<sup>2</sup>C specification for timing requirements.

## SPI Port Timing Specifications<sup>1</sup>

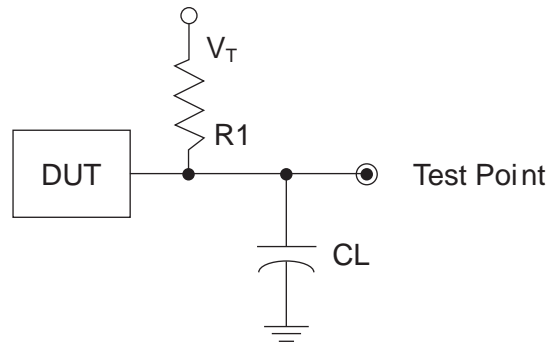
Symbol	Parameter	Min.	Max.	Units
f <sub>MAX</sub>	Maximum SCK clock frequency	—	45	MHz

- Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

## Switching Test Conditions

Figure 3-13 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-5.

**Figure 3-13. Output Test Load, LVTTTL and LVCMOS Standards**



**Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces**

Test Condition	R1	CL	Timing Ref.	VT
LVTTTL and LVCMOS settings (L -> H, H -> L)	$\infty$	0pF	LVTTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = V <sub>CCIO</sub> /2	—
			LVCMOS 1.8 = V <sub>CCIO</sub> /2	—
			LVCMOS 1.5 = V <sub>CCIO</sub> /2	—
			LVCMOS 1.2 = V <sub>CCIO</sub> /2	—
LVTTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5 V	V <sub>OL</sub>
LVTTTL and LVCMOS 3.3 (Z -> L)			1.5 V	V <sub>OH</sub>
Other LVCMOS (Z -> H)			V <sub>CCIO</sub> /2	V <sub>OL</sub>
Other LVCMOS (Z -> L)			V <sub>CCIO</sub> /2	V <sub>OH</sub>
LVTTTL + LVCMOS (H -> Z)			V <sub>OH</sub> - 0.15 V	V <sub>OL</sub>
LVTTTL + LVCMOS (L -> Z)			V <sub>OL</sub> - 0.15 V	V <sub>OH</sub>

Note: Output test conditions for all other interfaces are determined by the respective standards.

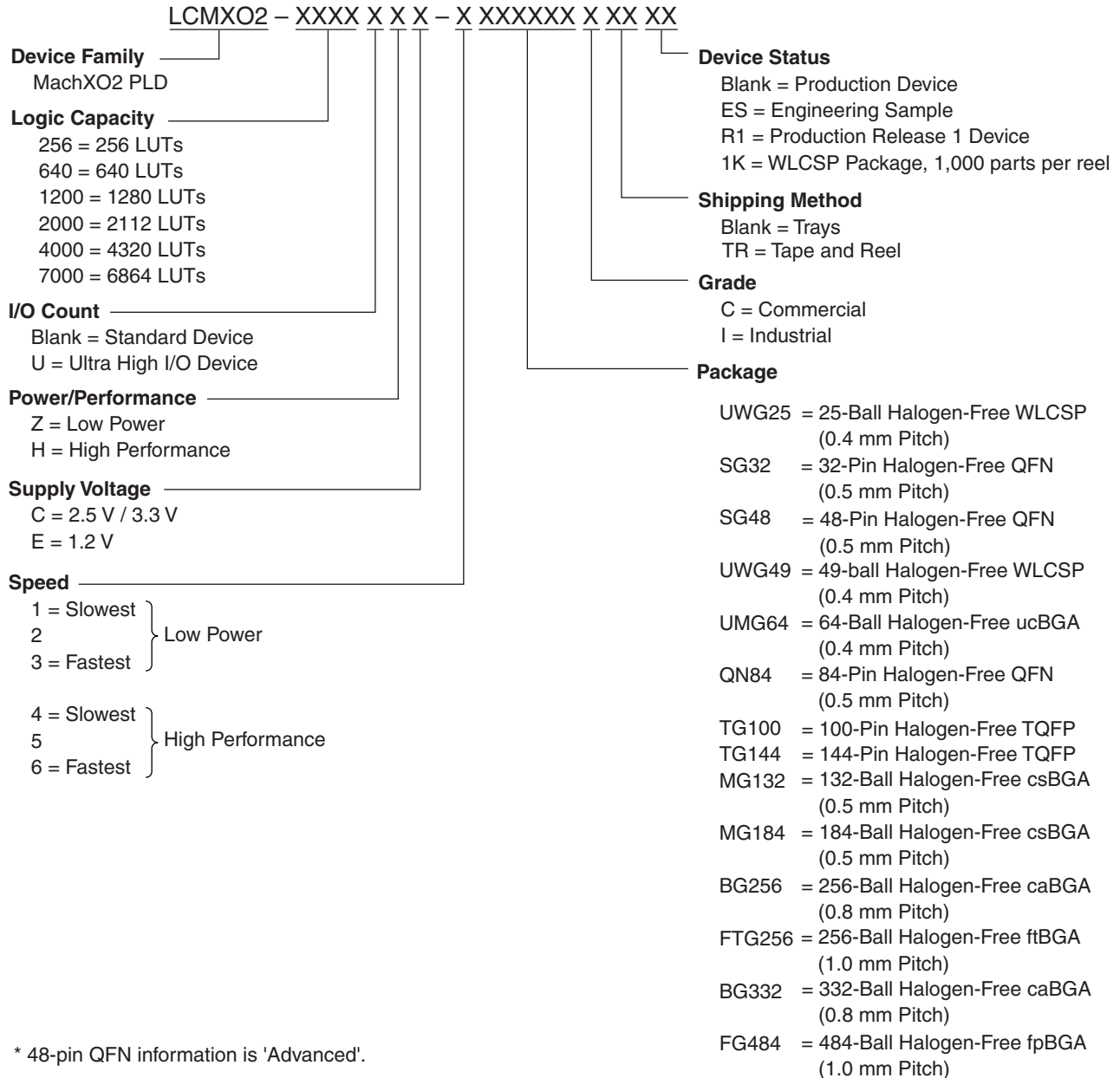
## Pinout Information Summary

	MachXO2-256					MachXO2-640			MachXO2-640U
	32 QFN <sup>1</sup>	48 QFN <sup>3</sup>	64 ucBGA	100 TQFP	132 csBGA	48 QFN <sup>3</sup>	100 TQFP	132 csBGA	144 TQFP
<b>General Purpose I/O per Bank</b>									
Bank 0	8	10	9	13	13	10	18	19	27
Bank 1	2	10	12	14	14	10	20	20	26
Bank 2	9	10	11	14	14	10	20	20	28
Bank 3	2	10	12	14	14	10	20	20	26
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Single Ended I/O	21	40	44	55	55	40	78	79	107
<b>Differential I/O per Bank</b>									
Bank 0	4	5	5	7	7	5	9	10	14
Bank 1	1	5	6	7	7	5	10	10	13
Bank 2	4	5	5	7	7	5	10	10	14
Bank 3	1	5	6	7	7	5	10	10	13
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Differential I/O	10	20	22	28	28	20	39	40	54
<b>Dual Function I/O</b>	22	25	27	29	29	25	29	29	33
<b>High-speed Differential I/O</b>									
Bank 0	0	0	0	0	0	0	0	0	7
<b>Gearboxes</b>									
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	0	0	0	0	0	0	0	0	7
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	0	0	0	0	0	0	0	0	7
<b>DQS Groups</b>									
Bank 1	0	0	0	0	0	0	0	0	2
<b>VCCIO Pins</b>									
Bank 0	2	2	2	2	2	2	2	2	3
Bank 1	1	1	2	2	2	1	2	2	3
Bank 2	2	2	2	2	2	2	2	2	3
Bank 3	1	1	2	2	2	1	2	2	3
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
VCC	2	2	2	2	2	2	2	2	4
GND <sup>2</sup>	2	1	8	8	8	1	8	10	12
NC	0	0	1	26	58	0	3	32	8
Reserved for Configuration	1	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	32	49	64	100	132	49	100	132	144

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.
2. For 48 QFN package, exposed die pad is the device ground.
3. 48-pin QFN information is 'Advanced'.

	MachXO2-7000					
	144 TQFP	256 caBGA	256 ftBGA	332 caBGA	400 caBGA	484 fpBGA
<b>General Purpose I/O per Bank</b>						
Bank 0	27	50	50	68	83	82
Bank 1	29	52	52	70	84	84
Bank 2	29	52	52	70	84	84
Bank 3	9	16	16	24	28	28
Bank 4	10	16	16	16	24	24
Bank 5	10	20	20	30	32	32
Total General Purpose Single Ended I/O	114	206	206	278	335	334
<b>Differential I/O per Bank</b>						
Bank 0	14	25	25	34	42	41
Bank 1	14	26	26	35	42	42
Bank 2	14	26	26	35	42	42
Bank 3	4	8	8	12	14	14
Bank 4	5	8	8	8	12	12
Bank 5	5	10	10	15	16	16
Total General Purpose Differential I/O	56	103	103	139	168	167
<b>Dual Function I/O</b>						
	37	37	37	37	37	37
<b>High-speed Differential I/O</b>						
Bank 0	9	20	20	21	21	21
<b>Gearboxes</b>						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	9	20	20	21	21	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	14	20	20	21	21	21
<b>DQS Groups</b>						
Bank 1	2	2	2	2	2	2
<b>VCCIO Pins</b>						
Bank 0	3	4	4	4	5	10
Bank 1	3	4	4	4	5	10
Bank 2	3	4	4	4	5	10
Bank 3	1	1	1	2	2	3
Bank 4	1	2	2	1	2	4
Bank 5	1	1	1	2	2	3
VCC	4	8	8	8	10	12
GND	12	24	24	27	33	48
NC	1	1	1	1	0	49
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	144	256	256	332	400	484

### MachXO2 Part Number Description





Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144C	6864	1.2 V	-1	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-2TG144C	6864	1.2 V	-2	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-3TG144C	6864	1.2 V	-3	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-1BG256C	6864	1.2 V	-1	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-2BG256C	6864	1.2 V	-2	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-3BG256C	6864	1.2 V	-3	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-1FTG256C	6864	1.2 V	-1	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-2FTG256C	6864	1.2 V	-2	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-3FTG256C	6864	1.2 V	-3	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-1BG332C	6864	1.2 V	-1	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-2BG332C	6864	1.2 V	-2	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-3BG332C	6864	1.2 V	-3	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-1FG484C	6864	1.2 V	-1	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-2FG484C	6864	1.2 V	-2	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-3FG484C	6864	1.2 V	-3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100CR1 <sup>1</sup>	1280	1.2 V	-1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100CR1 <sup>1</sup>	1280	1.2 V	-2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100CR1 <sup>1</sup>	1280	1.2 V	-3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132CR1 <sup>1</sup>	1280	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132CR1 <sup>1</sup>	1280	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132CR1 <sup>1</sup>	1280	1.2 V	-3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144CR1 <sup>1</sup>	1280	1.2 V	-1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144CR1 <sup>1</sup>	1280	1.2 V	-2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144CR1 <sup>1</sup>	1280	1.2 V	-3	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200ZE-speed package CR1” are the same as the “LCMXO2-1200ZE-speed package C” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000ZE-1QN84I	4320	1.2 V	-1	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-2QN84I	4320	1.2 V	-2	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-3QN84I	4320	1.2 V	-3	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-1MG132I	4320	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-2MG132I	4320	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-3MG132I	4320	1.2 V	-3	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-1TG144I	4320	1.2 V	-1	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-2TG144I	4320	1.2 V	-2	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-3TG144I	4320	1.2 V	-3	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-1BG256I	4320	1.2 V	-1	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-2BG256I	4320	1.2 V	-2	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-3BG256I	4320	1.2 V	-3	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-1FTG256I	4320	1.2 V	-1	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-2FTG256I	4320	1.2 V	-2	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-3FTG256I	4320	1.2 V	-3	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-1BG332I	4320	1.2 V	-1	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-2BG332I	4320	1.2 V	-2	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-3BG332I	4320	1.2 V	-3	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-1FG484I	4320	1.2 V	-1	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-2FG484I	4320	1.2 V	-2	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-3FG484I	4320	1.2 V	-3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144I	6864	1.2 V	-1	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-2TG144I	6864	1.2 V	-2	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-3TG144I	6864	1.2 V	-3	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-1BG256I	6864	1.2 V	-1	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-2BG256I	6864	1.2 V	-2	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-3BG256I	6864	1.2 V	-3	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-1FTG256I	6864	1.2 V	-1	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-2FTG256I	6864	1.2 V	-2	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-3FTG256I	6864	1.2 V	-3	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-1BG332I	6864	1.2 V	-1	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-2BG332I	6864	1.2 V	-2	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-3BG332I	6864	1.2 V	-3	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-1FG484I	6864	1.2 V	-1	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-2FG484I	6864	1.2 V	-2	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-3FG484I	6864	1.2 V	-3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100IR1 <sup>1</sup>	1280	1.2 V	-1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100IR1 <sup>1</sup>	1280	1.2 V	-2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100IR1 <sup>1</sup>	1280	1.2 V	-3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132IR1 <sup>1</sup>	1280	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132IR1 <sup>1</sup>	1280	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132IR1 <sup>1</sup>	1280	1.2 V	-3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144IR1 <sup>1</sup>	1280	1.2 V	-1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144IR1 <sup>1</sup>	1280	1.2 V	-2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144IR1 <sup>1</sup>	1280	1.2 V	-3	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200ZE-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

## R1 Device Specifications

The LCMXO2-1200ZE/HC “R1” devices have the same specifications as their Standard (non-R1) counterparts except as listed below. For more details on the R1 to Standard migration refer to AN8086, [Designing for Migration from MachXO2-1200-R1 to Standard Non-R1\) Devices](#).

- The User Flash Memory (UFM) cannot be programmed through the internal WISHBONE interface. It can still be programmed through the JTAG/SPI/I<sup>2</sup>C ports.
- The on-chip differential input termination resistor value is higher than intended. It is approximately 200Ω as opposed to the intended 100Ω. It is recommended to use external termination resistors for differential inputs. The on-chip termination resistors can be disabled through Lattice design software.
- Soft Error Detection logic may not produce the correct result when it is run for the first time after configuration. To use this feature, discard the result from the first operation. Subsequent operations will produce the correct result.
- Under certain conditions, I<sub>IH</sub> exceeds data sheet specifications. The following table provides more details:

Condition	Clamp	Pad Rising I <sub>IH</sub> Max.	Pad Falling I <sub>IH</sub> Min.	Steady State Pad High I <sub>IH</sub>	Steady State Pad Low I <sub>IL</sub>
VPAD > VCCIO	OFF	1 mA	-1 mA	1 mA	10 μA
VPAD = VCCIO	ON	10 μA	-10 μA	10 μA	10 μA
VPAD = VCCIO	OFF	1 mA	-1 mA	1 mA	10 μA
VPAD < VCCIO	OFF	10 μA	-10 μA	10 μA	10 μA

- The user SPI interface does not operate correctly in some situations. During master read access and slave write access, the last byte received does not generate the RRDY interrupt.
- In GDDR2, GDDR4 and GDDR71 modes, ECLKSYNC may have a glitch in the output under certain conditions, leading to possible loss of synchronization.
- When using the hard I<sup>2</sup>C IP core, the I<sup>2</sup>C status registers I2C\_1\_SR and I2C\_2\_SR may not update correctly.
- PLL Lock signal will glitch high when coming out of standby. This glitch lasts for about 10 μsec before returning low.
- Dual boot only available on HC devices, requires tying VCC and VCCIO2 to the same 3.3 V or 2.5 V supply.

Date	Version	Section	Change Summary
May 2016	3.2	All	Moved designation for 84 QFN package information from 'Advanced' to 'Final'.
		Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 'Advanced' 48 QFN package. — Revised footnote 6. — Added footnote 9.
		DC and Switching Characteristics	Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Added footnote 12.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Added footnote 12.
		Pinout Information	Updated the Signal Descriptions section. Added information on GND signal.
			Updated the Pinout Information Summary section. — Added 'Advanced' MachXO2-256 48 QFN values. — Added 'Advanced' MachXO2-640 48 QFN values. — Added footnote to GND. — Added footnotes 2 and 3.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added 'Advanced' SG48 package and revised footnote.
Updated the Ordering Information section. — Added part numbers for 'Advanced' QFN 48 package.			
March 2016	3.1	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 32 QFN value for XO2-1200. — Added 84 QFN (7 mm x 7 mm, 0.5 mm) package. — Modified package name to 100-pin TQFP. — Modified package name to 144-pin TQFP. — Added footnote.
		Architecture	Updated the Typical I/O Behavior During Power-up section. Removed reference to TN1202.
		DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications section. Revised $t_{DPPDONE}$ and $t_{DPPINIT}$ Max. values per PCN 03A-16, released March 2016.
		Pinout Information	Updated the Pinout Information Summary section. — Added MachXO2-1200 32 QFN values. — Added 'Advanced' MachXO2-4000 84 QFN values.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added 'Advanced' QN84 package and footnote.
Updated the Ordering Information section. — Added part numbers for 1280 LUTs QFN 32 package. — Added part numbers for 4320 LUTs QFN 84 package.			
March 2015	3.0	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Changed 64-ball ucBGA dimension.
		Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.