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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	264
Number of Logic Elements/Cells	2112
Total RAM Bits	75776
Number of I/O	206
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-CABGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-2000ze-2bg256c

Features

■ Flexible Logic Architecture

- Six devices with 256 to 6864 LUT4s and 18 to 334 I/Os

■ Ultra Low Power Devices

- Advanced 65 nm low power process
- As low as 22 μ W standby power
- Programmable low swing differential I/Os
- Stand-by mode and other power saving options

■ Embedded and Distributed Memory

- Up to 240 kbits sysMEM™ Embedded Block RAM
- Up to 54 kbits Distributed RAM
- Dedicated FIFO control logic

■ On-Chip User Flash Memory

- Up to 256 kbits of User Flash Memory
- 100,000 write cycles
- Accessible through WISHBONE, SPI, I²C and JTAG interfaces
- Can be used as soft processor PROM or as Flash memory

■ Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/Os
- Generic DDR, DDRX2, DDRX4
- Dedicated DDR/DDR2/LPDDR memory with DQS support

■ High Performance, Flexible I/O Buffer

- Programmable sysIO™ buffer supports wide range of interfaces:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2
 - LVTTTL
 - PCI
 - LVDS, Bus-LVDS, MLVDS, RSDS, LVPECL
 - SSTL 25/18
 - HSTL 18
 - Schmitt trigger inputs, up to 0.5 V hysteresis
- I/Os support hot socketing
- On-chip differential termination
- Programmable pull-up or pull-down mode

■ Flexible On-Chip Clocking

- Eight primary clocks
- Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
- Up to two analog PLLs per device with fractional-n frequency synthesis
 - Wide input frequency range (7 MHz to 400 MHz)

■ Non-volatile, Infinitely Reconfigurable

- Instant-on – powers up in microseconds
- Single-chip, secure solution
- Programmable through JTAG, SPI or I²C
- Supports background programming of non-volatile memory
- Optional dual boot with external SPI memory

■ TransFR™ Reconfiguration

- In-field logic update while system operates

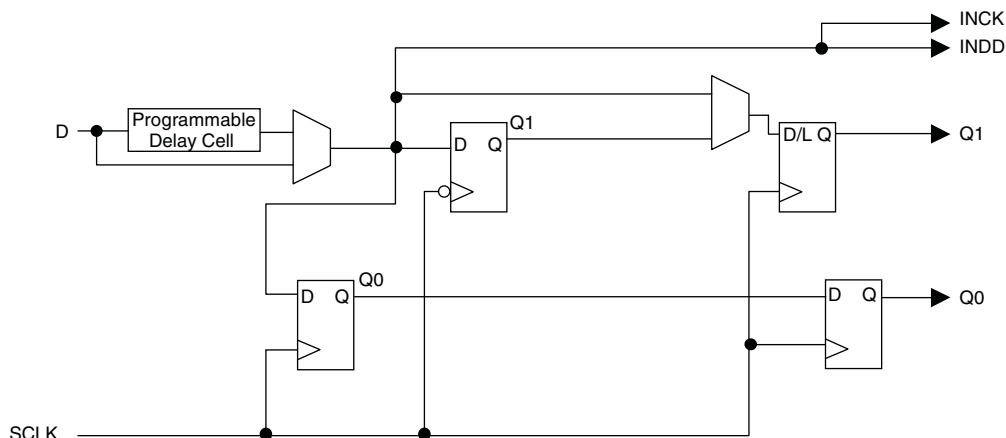
■ Enhanced System Level Support

- On-chip hardened functions: SPI, I²C, timer/counter
- On-chip oscillator with 5.5% accuracy
- Unique TraceID for system tracking
- One Time Programmable (OTP) mode
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming

■ Broad Range of Package Options

- TQFP, WLCSP, ucBGA, csBGA, caBGA, ftBGA, fpBGA, QFN package options
- Small footprint package options
 - As small as 2.5 mm x 2.5 mm
- Density migration supported
- Advanced halogen-free packaging

Figure 2-12. MachXO2 Input Register Block Diagram (PIO on Left, Top and Bottom Edges)



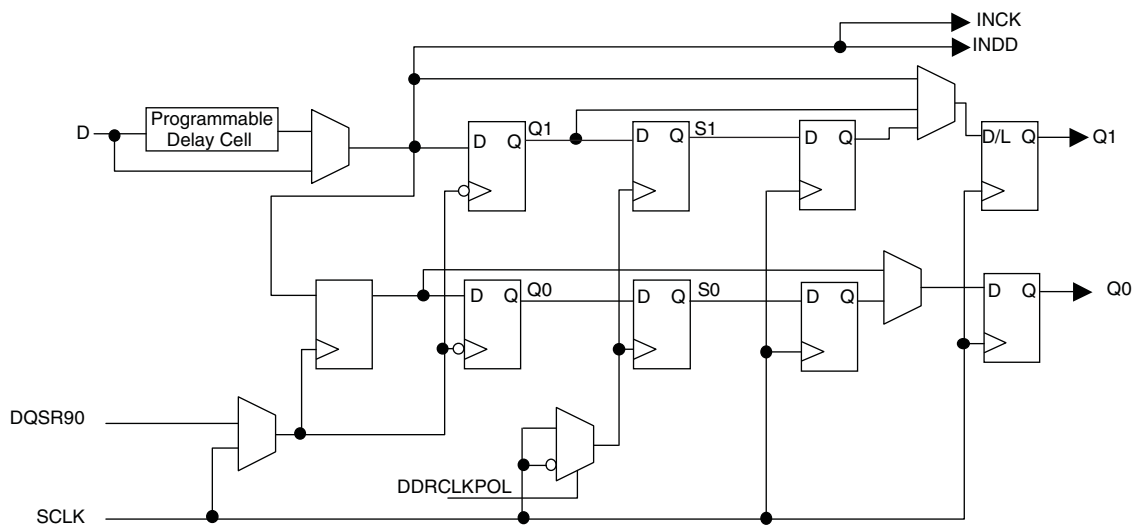
Right Edge

The input register block on the right edge is a superset of the same block on the top, bottom, and left edges. In addition to the modes described above, the input register block on the right edge also supports DDR memory mode.

In DDR memory mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (DQSR90) in the DDR Memory mode creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the DQS domain. The DQSR90 and DDRCLKPOL signals are generated in the DQS read-write block.

Figure 2-13. MachXO2 Input Register Block Diagram (PIO on Right Edge)



Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, [Boundary Scan Testability with Lattice sysIO Capability](#) and TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#).

Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I²C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

1. Internal Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I²C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, [MachXO2 Programming and Configuration Usage Guide](#) for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#) for details.

When implementing background programming of the on-chip Flash, care must be taken for the operation of the PLL. For devices that have two PLLs (XO2-2000U, -4000 and -7000), the system must put the RPLL (Right-side PLL) in reset state during the background Flash programming. More detailed description can be found in TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO2 devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile Flash memory spaces. The device can be in one of two modes:

1. Unlocked – Readback of the SRAM configuration and non-volatile Flash memory spaces is allowed.
2. Permanently Locked – The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

Dual Boot

MachXO2 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the on-chip Flash. The golden image MUST reside in an external SPI Flash. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1206, [MachXO2 Soft Error Detection Usage Guide](#).

TraceID

Each MachXO2 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I²C, or JTAG interfaces.

Density Shifting

The MachXO2 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the [MachXO2 migration files](#).

Static Supply Current – HC/HE Devices^{1, 2, 3, 6}

Symbol	Parameter	Device	Typ. ⁴	Units
I_{CC}	Core Power Supply	LCMXO2-256HC	1.15	mA
		LCMXO2-640HC	1.84	mA
		LCMXO2-640UHC	3.48	mA
		LCMXO2-1200HC	3.49	mA
		LCMXO2-1200UHC	4.80	mA
		LCMXO2-2000HC	4.80	mA
		LCMXO2-2000UHC	8.44	mA
		LCMXO2-4000HC	8.45	mA
		LCMXO2-7000HC	12.87	mA
		LCMXO2-2000HE	1.39	mA
		LCMXO2-4000HE	2.55	mA
		LCMXO2-7000HE	4.06	mA
I_{CCIO}	Bank Power Supply ⁵ $V_{CCIO} = 2.5\text{ V}$	All devices	0	mA

- For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).
- Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
- Frequency = 0 MHz.
- $T_J = 25\text{ }^{\circ}\text{C}$, power supplies at nominal voltage.
- Does not include pull-up/pull-down.
- To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Programming and Erase Flash Supply Current – HC/HE Devices^{1, 2, 3, 4}

Symbol	Parameter	Device	Typ. ⁵	Units
I_{CC}	Core Power Supply	LCMXO2-256HC	14.6	mA
		LCMXO2-640HC	16.1	mA
		LCMXO2-640UHC	18.8	mA
		LCMXO2-1200HC	18.8	mA
		LCMXO2-1200UHC	22.1	mA
		LCMXO2-2000HC	22.1	mA
		LCMXO2-2000UHC	26.8	mA
		LCMXO2-4000HC	26.8	mA
		LCMXO2-7000HC	33.2	mA
		LCMXO2-2000HE	18.3	mA
		LCMXO2-2000UHE	20.4	mA
		LCMXO2-4000HE	20.4	mA
		LCMXO2-7000HE	23.9	mA
I_{CCIO}	Bank Power Supply ⁶	All devices	0	mA

- For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).
- Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
- Typical user pattern.
- JTAG programming is at 25 MHz.
- $T_J = 25\text{ }^{\circ}\text{C}$, power supplies at nominal voltage.
- Per bank. $V_{CCIO} = 2.5\text{ V}$. Does not include pull-up/pull-down.

Programming and Erase Flash Supply Current – ZE Devices^{1, 2, 3, 4}

Symbol	Parameter	Device	Typ. ⁵	Units
I_{CC}	Core Power Supply	LCMXO2-256ZE	13	mA
		LCMXO2-640ZE	14	mA
		LCMXO2-1200ZE	15	mA
		LCMXO2-2000ZE	17	mA
		LCMXO2-4000ZE	18	mA
		LCMXO2-7000ZE	20	mA
I_{CCIO}	Bank Power Supply ⁶	All devices	0	mA

1. For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).

2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.

3. Typical user pattern.

4. JTAG programming is at 25 MHz.

5. $T_J = 25^\circ\text{C}$, power supplies at nominal voltage.

6. Per bank. $V_{CCIO} = 2.5\text{ V}$. Does not include pull-up/pull-down.

LVPECL

The MachXO2 family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

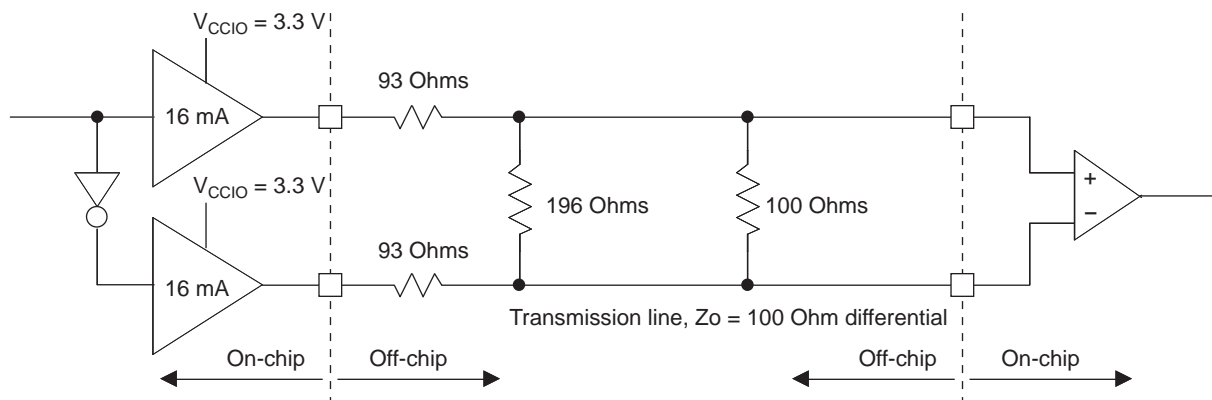


Table 3-3. LVPECL DC Conditions¹

Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	93	Ohms
R_P	Driver parallel resistor	196	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	2.05	V
V_{OL}	Output low voltage	1.25	V
V_{OD}	Output differential voltage	0.80	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	12.11	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

Typical Building Block Function Performance – ZE Devices¹

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–3 Timing	Units
Basic Functions		
16-bit decoder	13.9	ns
4:1 MUX	10.9	ns
16:1 MUX	12.0	ns

Register-to-Register Performance

Function	–3 Timing	Units
Basic Functions		
16:1 MUX	191	MHz
16-bit adder	134	MHz
16-bit counter	148	MHz
64-bit counter	77	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	90	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	214	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Parameter	Description	Device	-3		-2		-1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR ^{9, 12}									
t _{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. ¹³	—	0.349	—	0.381	—	0.396	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.630	—	0.613	—	UI
t _{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f _{DATA}	MEM LPDDR Serial Data Speed		—	120	—	110	—	96	Mbps
f _{SCLK}	SCLK Frequency		—	60	—	55	—	48	MHz
f _{LPDDR}	LPDDR Data Transfer Rate		0	120	0	110	0	96	Mbps
DDR ^{9, 12}									
t _{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. ¹³	—	0.347	—	0.374	—	0.393	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.637	—	0.616	—	UI
t _{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f _{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f _{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f _{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps
DDR2 ^{9, 12}									
t _{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. ¹³	—	0.372	—	0.394	—	0.410	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.690	—	0.658	—	0.618	—	UI
t _{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f _{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f _{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f _{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps

- Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
- General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pF load, fast slew rate.
- Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
- DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
- 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
- For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$.
- The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 167 ps (-3), 182 ps (-2), 195 ps (-1).
- This number for general purpose usage. Duty cycle tolerance is +/-10%.
- Duty cycle is +/- 5% for system usage.
- The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
- High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.
- Advance information for MachXO2 devices in 48 QFN packages.
- DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)		1.5625	400	MHz
f_{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f_{VCO}	PLL VCO Frequency		200	800	MHz
f_{PFD}	Phase Detector Input Frequency		7	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Without duty trim selected ³	45	55	%
$t_{DT_TRIM}^7$	Edge Duty Trim Accuracy		-75	75	%
t_{PH}^4	Output Phase Accuracy		-6	6	%
$t_{OPJIT}^{1,8}$	Output Clock Period Jitter	$f_{OUT} > 100$ MHz	—	150	ps p-p
		$f_{OUT} < 100$ MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	$f_{OUT} > 100$ MHz	—	180	ps p-p
		$f_{OUT} < 100$ MHz	—	0.009	UIPP
	Output Clock Phase Jitter	$f_{PFD} > 100$ MHz	—	160	ps p-p
		$f_{PFD} < 100$ MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	$f_{OUT} > 100$ MHz	—	230	ps p-p
		$f_{OUT} < 100$ MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N)	$f_{OUT} > 100$ MHz	—	230	ps p-p
		$f_{OUT} < 100$ MHz	—	0.12	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	-120	120	ps
t_W	Output Clock Pulse Width	At 90% or 10% ³	0.9	—	ns
$t_{LOCK}^{2,5}$	PLL Lock-in Time		—	15	ms
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}^6	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{STABLE}^5	STANDBY High to PLL Stable		—	15	ms
t_{RST}	RST/RESETM Pulse Width		1	—	ns
t_{RSTREC}	RST Recovery Time		1	—	ns
t_{RST_DIV}	RESETC/D Pulse Width		10	—	ns
t_{RSTREC_DIV}	RESETC/D Recovery Time		1	—	ns
$t_{ROTATE-SETUP}$	PHASESTEP Setup Time		10	—	ns

I²C Port Timing Specifications^{1, 2}

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCL clock frequency	—	400	kHz

- MachXO2 supports the following modes:
 - Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
 - Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
- Refer to the I²C specification for timing requirements.

SPI Port Timing Specifications¹

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCK clock frequency	—	45	MHz

- Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

Switching Test Conditions

Figure 3-13 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-5.

Figure 3-13. Output Test Load, LVTTTL and LVCMOS Standards

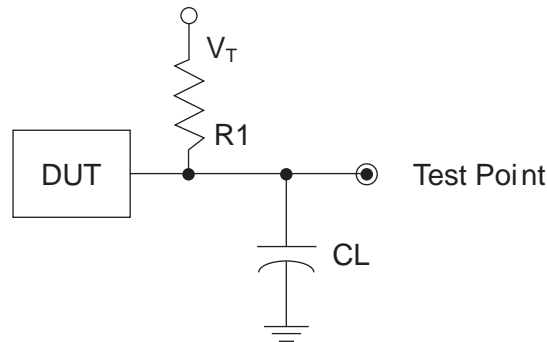


Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R1	CL	Timing Ref.	VT
LVTTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVTTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = V _{CCIO} /2	—
			LVCMOS 1.8 = V _{CCIO} /2	—
			LVCMOS 1.5 = V _{CCIO} /2	—
			LVCMOS 1.2 = V _{CCIO} /2	—
LVTTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5 V	V _{OL}
LVTTTL and LVCMOS 3.3 (Z -> L)			1.5 V	V _{OH}
Other LVCMOS (Z -> H)			V _{CCIO} /2	V _{OL}
Other LVCMOS (Z -> L)			V _{CCIO} /2	V _{OH}
LVTTTL + LVCMOS (H -> Z)			V _{OH} - 0.15 V	V _{OL}
LVTTTL + LVCMOS (L -> Z)			V _{OL} - 0.15 V	V _{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	<p>[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).</p> <p>[Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.</p> <p>[A/B/C/D] indicates the PIO within the group to which the pad is connected.</p> <p>Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic.</p> <p>During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.</p>
NC	—	No connect.
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together. For QFN 48 package, the exposed die pad is the device ground.
VCC	—	VCC – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIOx	—	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.
PLL and Clock Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)		
[LOC]_GPLL[T, C]_IN	—	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.
Test and Programming (Dual function pins used for test access port and during sysCONFIG™)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
JTAGENB	I	<p>Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then:</p> <p>If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O.</p> <p>If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.</p> <p>For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.</p>
Configuration (Dual function pins used during sysCONFIG)		
PROGRAMN	I	Initiates configuration sequence when asserted low. During configuration, or when reserved as PROGRAMN in user mode, this pin always has an active pull-up.

	MachXO2-2000						MachXO2-2000U
	49 WLCSP	100 TQFP	132 csBGA	144 TQFP	256 caBGA	256 ftBGA	484 ftBGA
General Purpose I/O per Bank							
Bank 0	19	18	25	27	50	50	70
Bank 1	0	21	26	28	52	52	68
Bank 2	13	20	28	28	52	52	72
Bank 3	0	6	7	8	16	16	24
Bank 4	0	6	8	10	16	16	16
Bank 5	6	8	10	10	20	20	28
Total General Purpose Single-Ended I/O	38	79	104	111	206	206	278
Differential I/O per Bank							
Bank 0	7	9	13	14	25	25	35
Bank 1	0	10	13	14	26	26	34
Bank 2	6	10	14	14	26	26	36
Bank 3	0	3	3	4	8	8	12
Bank 4	0	3	4	5	8	8	8
Bank 5	3	4	5	5	10	10	14
Total General Purpose Differential I/O	16	39	52	56	103	103	139
Dual Function I/O							
	24	31	33	33	33	33	37
High-speed Differential I/O							
Bank 0	5	4	8	9	14	14	18
Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	4	8	9	14	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	10	14	14	14	14	18
DQS Groups							
Bank 1	0	1	2	2	2	2	2
VCCIO Pins							
Bank 0	2	2	3	3	4	4	10
Bank 1	0	2	3	3	4	4	10
Bank 2	1	2	3	3	4	4	10
Bank 3	0	1	1	1	1	1	3
Bank 4	0	1	1	1	2	2	4
Bank 5	1	1	1	1	1	1	3
VCC	2	2	4	4	8	8	12
GND	4	8	10	12	24	24	48
NC	0	1	1	4	1	1	105
Reserved for Configuration	1	1	1	1	v	1	1
Total Count of Bonded Pins	39	100	132	144	256	256	484

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144C	6864	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-2TG144C	6864	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-3TG144C	6864	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-1BG256C	6864	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-2BG256C	6864	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-3BG256C	6864	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-1FTG256C	6864	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-2FTG256C	6864	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-3FTG256C	6864	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-1BG332C	6864	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-2BG332C	6864	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-3BG332C	6864	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-1FG484C	6864	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-2FG484C	6864	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-3FG484C	6864	1.2 V	–3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100CR1 ¹	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100CR1 ¹	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100CR1 ¹	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132CR1 ¹	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132CR1 ¹	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132CR1 ¹	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144CR1 ¹	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144CR1 ¹	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144CR1 ¹	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200ZE-speed package CR1” are the same as the “LCMXO2-1200ZE-speed package C” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32C	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	COM
LCMXO2-256HC-5SG32C	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	COM
LCMXO2-256HC-6SG32C	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	COM
LCMXO2-256HC-4SG48C	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	COM
LCMXO2-256HC-5SG48C	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	COM
LCMXO2-256HC-6SG48C	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	COM
LCMXO2-256HC-4UMG64C	256	2.5 V / 3.3 V	–4	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-5UMG64C	256	2.5 V / 3.3 V	–5	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-6UMG64C	256	2.5 V / 3.3 V	–6	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-4TG100C	256	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-256HC-5TG100C	256	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-256HC-6TG100C	256	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-256HC-4MG132C	256	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-256HC-5MG132C	256	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-256HC-6MG132C	256	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48C	640	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	COM
LCMXO2-640HC-5SG48C	640	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	COM
LCMXO2-640HC-6SG48C	640	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	COM
LCMXO2-640HC-4TG100C	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-640HC-5TG100C	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-640HC-6TG100C	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-640HC-4MG132C	640	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-640HC-5MG132C	640	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-640HC-6MG132C	640	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144C	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-5TG144C	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-6TG144C	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-6BG332C	4320	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-4FG484C	4320	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-5FG484C	4320	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-6FG484C	4320	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144C	6864	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-5TG144C	6864	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-6TG144C	6864	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-4BG256C	6864	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-5BG256C	6864	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-6BG256C	6864	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-4FTG256C	6864	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-5FTG256C	6864	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-6FTG256C	6864	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-4BG332C	6864	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-5BG332C	6864	1.2 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-6BG332C	6864	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-4FG484C	6864	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-5FG484C	6864	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-6FG484C	6864	1.2 V	–6	Halogen-Free fpBGA	484	COM

Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32I	256	1.2 V	–1	Halogen-Free QFN	32	IND
LCMXO2-256ZE-2SG32I	256	1.2 V	–2	Halogen-Free QFN	32	IND
LCMXO2-256ZE-3SG32I	256	1.2 V	–3	Halogen-Free QFN	32	IND
LCMXO2-256ZE-1UMG64I	256	1.2 V	–1	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-2UMG64I	256	1.2 V	–2	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-3UMG64I	256	1.2 V	–3	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-1TG100I	256	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-2TG100I	256	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-3TG100I	256	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-1MG132I	256	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-2MG132I	256	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-3MG132I	256	1.2 V	–3	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100I	640	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-2TG100I	640	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-3TG100I	640	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-1MG132I	640	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-2MG132I	640	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-3MG132I	640	1.2 V	–3	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1UWG25ITR ¹	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR50 ³	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR1K ²	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1SG32I	1280	1.2 V	–1	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-2SG32I	1280	1.2 V	–2	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-3SG32I	1280	1.2 V	–3	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-1TG100I	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100I	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100I	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132I	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132I	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132I	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144I	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144I	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144I	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000ZE-1QN84I	4320	1.2 V	–1	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-2QN84I	4320	1.2 V	–2	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-3QN84I	4320	1.2 V	–3	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-1MG132I	4320	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-2MG132I	4320	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-3MG132I	4320	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-1TG144I	4320	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-2TG144I	4320	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-3TG144I	4320	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-1BG256I	4320	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-2BG256I	4320	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-3BG256I	4320	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-1FTG256I	4320	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-2FTG256I	4320	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-3FTG256I	4320	1.2 V	–3	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-1BG332I	4320	1.2 V	–1	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-2BG332I	4320	1.2 V	–2	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-3BG332I	4320	1.2 V	–3	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-1FG484I	4320	1.2 V	–1	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-2FG484I	4320	1.2 V	–2	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-3FG484I	4320	1.2 V	–3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144I	6864	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-2TG144I	6864	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-3TG144I	6864	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-1BG256I	6864	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-2BG256I	6864	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-3BG256I	6864	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-1FTG256I	6864	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-2FTG256I	6864	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-3FTG256I	6864	1.2 V	–3	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-1BG332I	6864	1.2 V	–1	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-2BG332I	6864	1.2 V	–2	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-3BG332I	6864	1.2 V	–3	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-1FG484I	6864	1.2 V	–1	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-2FG484I	6864	1.2 V	–2	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-3FG484I	6864	1.2 V	–3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100IR1 ¹	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100IR1 ¹	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100IR1 ¹	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132IR1 ¹	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132IR1 ¹	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132IR1 ¹	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144IR1 ¹	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144IR1 ¹	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144IR1 ¹	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200ZE-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

Date	Version	Section	Change Summary
May 2011	01.3	Multiple	Replaced “SED” with “SRAM CRC Error Detection” throughout the document.
		DC and Switching Characteristics	Added footnote 1 to Program Erase Specifications table.
		Pinout Information	Updated Pin Information Summary tables.
			Signal name SO/SISPISO changed to SO/SPISO in the Signal Descriptions table.
April 2011	01.2	—	Data sheet status changed from Advance to Preliminary.
		Introduction	Updated MachXO2 Family Selection Guide table.
		Architecture	Updated Supported Input Standards table.
			Updated sysMEM Memory Primitives diagram.
			Added differential SSTL and HSTL IO standards.
		DC and Switching Characteristics	Updates following parameters: POR voltage levels, DC electrical characteristics, static supply current for ZE/HE/HC devices, static power consumption contribution of different components – ZE devices, programming and erase Flash supply current.
			Added VREF specifications to sysIO recommended operating conditions.
			Updating timing information based on characterization.
			Added differential SSTL and HSTL IO standards.
		Ordering Information	Added Ordering Part Numbers for R1 devices, and devices in WLCSP packages.
			Added R1 device specifications.
January 2011	01.1	All	Included ultra-high I/O devices.
		DC and Switching Characteristics	Recommended Operating Conditions table – Added footnote 3.
			DC Electrical Characteristics table – Updated data for I_{IL} , I_{IH} , V_{HYST} typical values updated.
			Generic DDRX2 Outputs with Clock and Data Aligned at Pin (GDDR2_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB} .
			Generic DDRX4 Outputs with Clock and Data Aligned at Pin (GDDR4_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB} .
			Power-On-Reset Voltage Levels table - clarified note 3.
			Clarified VCCIO related recommended operating conditions specifications.
			Added power supply ramp rate requirements.
			Added Power Supply Ramp Rates table.
			Updated Programming/Erase Specifications table.
			Removed references to V_{CCP} .
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Removed references to V_{CCP} .
November 2010	01.0	—	Initial release.