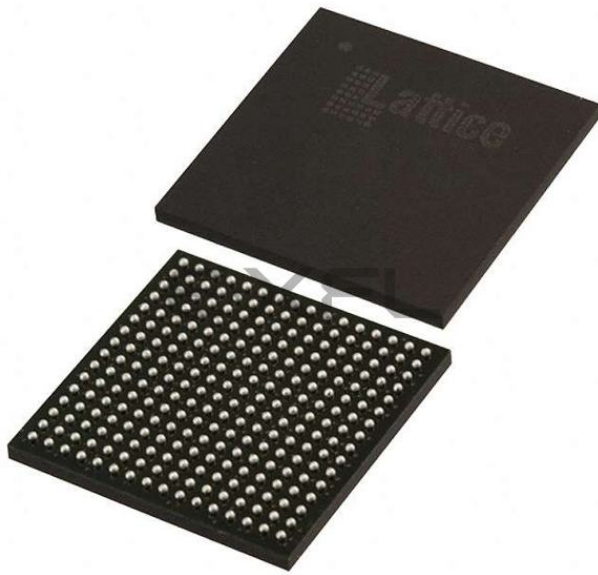




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	264
Number of Logic Elements/Cells	2112
Total RAM Bits	75776
Number of I/O	206
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (Tj)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-2000ze-3ftg256i

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO2 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

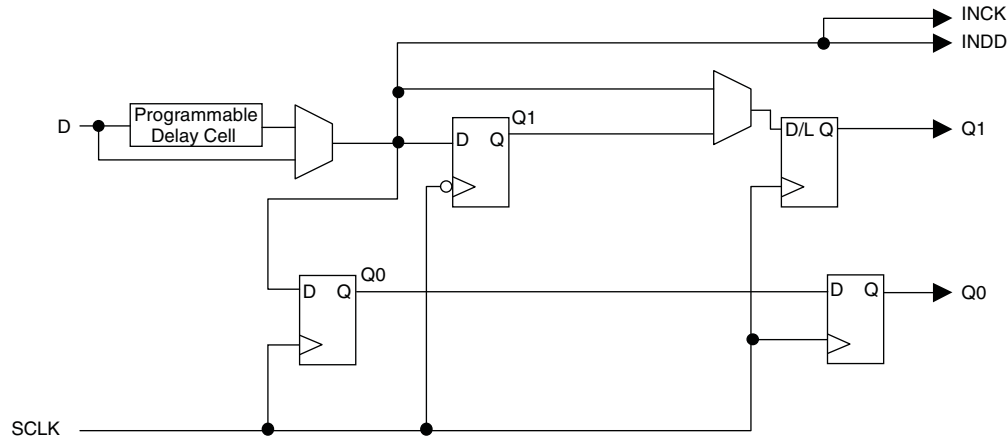
Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO2 devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO2 devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

The MachXO2-640U, MachXO2-1200/U and higher density devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these higher density devices have on-chip differential termination and also provide PCI support.

Figure 2-12. MachXO2 Input Register Block Diagram (PIO on Left, Top and Bottom Edges)



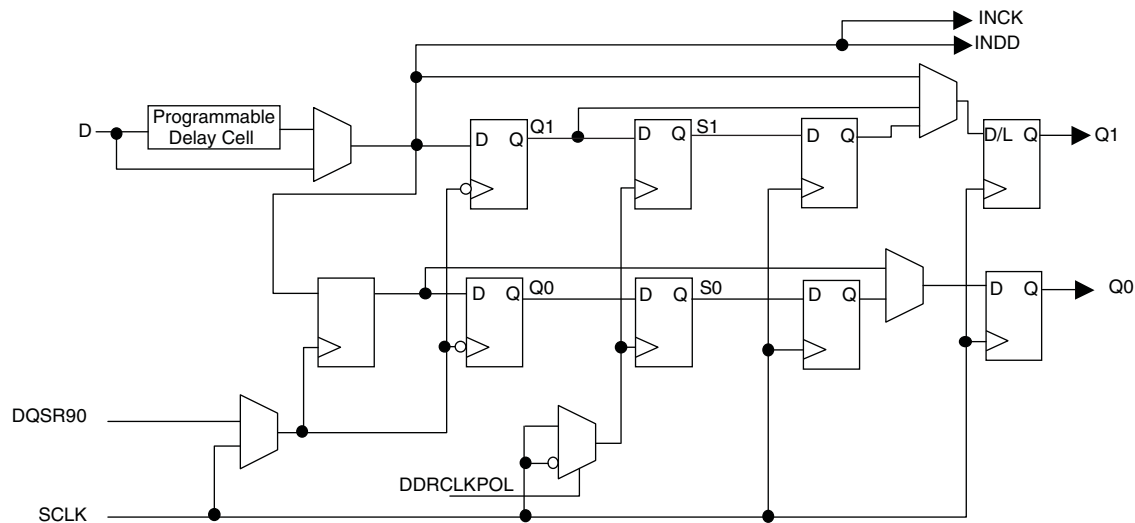
Right Edge

The input register block on the right edge is a superset of the same block on the top, bottom, and left edges. In addition to the modes described above, the input register block on the right edge also supports DDR memory mode.

In DDR memory mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (DQSR90) in the DDR Memory mode creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the DQS domain. The DQSR90 and DDRCLKPOL signals are generated in the DQS read-write block.

Figure 2-13. MachXO2 Input Register Block Diagram (PIO on Right Edge)



DDR Memory Support

Certain PICs on the right edge of MachXO2-640U, MachXO2-1200/U and larger devices, have additional circuitry to allow the implementation of DDR memory interfaces. There are two groups of 14 or 12 PIOs each on the right edge with additional circuitry to implement DDR memory interfaces. This capability allows the implementation of up to 16-bit wide memory interfaces. One PIO from each group contains a control element, the DQS Read/Write Block, to facilitate the generation of clock and control signals (DQSR90, DQSW90, DDRCLKPOL and DATAVALID). These clock and control signals are distributed to the other PIO in the group through dedicated low skew routing.

DQS Read Write Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Read Write block provides the required clock alignment for DDR memory interfaces. DQSR90 and DQSW90 signals are generated by the DQS Read Write block from the DQS input.

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the read cycle) is unknown. The MachXO2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This circuit changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each read cycle for the correct clock polarity. Prior to the read operation in DDR memories, DQS is in tri-state (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit in the DQS Read Write block detects the first DQS rising edge after the preamble state and generates the DDRCLKPOL signal. This signal is used to control the polarity of the clock to the synchronizing registers.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration signals (6-bit bus) from a DLL on the right edge of the device. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, PCI, SSTL, HSTL, LVDS, BLVDS, MLVDS and LVPECL.

Each bank is capable of supporting multiple I/O standards. In the MachXO2 devices, single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS and PCI), differential (LVDS) and referenced input buffers (SSTL and HSTL) are powered using I/O supply voltage (V_{CCIO}). Each sysIO bank has its own V_{CCIO} . In addition, each bank has a voltage reference, V_{REF} which allows the use of referenced input buffers independent of the bank V_{CCIO} .

MachXO2-256 and MachXO2-640 devices contain single-ended ratioed input buffers and single-ended output buffers with complementary outputs on all the I/O banks. Note that the single-ended input buffers on these devices do not contain PCI clamps. In addition to the single-ended I/O buffers these two devices also have differential and referenced input buffers on all I/Os. The I/Os are arranged in pairs, the two pads in the pair are described as "T" and "C", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Table 2-11. I/O Support Device by Device

	MachXO2-256, MachXO2-640	MachXO2-640U, MachXO2-1200	MachXO2-1200U MachXO2-2000/U, MachXO2-4000, MachXO2-7000
Number of I/O Banks	4	4	6
Type of Input Buffers	Single-ended (all I/O banks) Differential Receivers (all I/O banks)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)
Types of Output Buffers	Single-ended buffers with complementary outputs (all I/O banks)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)
Differential Output Emulation Capability	All I/O banks	All I/O banks	All I/O banks
PCI Clamp Support	No	Clamp on bottom side only	Clamp on bottom side only

Table 2-12. Supported Input Standards

Input Standard	VCCIO (Typ.)				
	3.3 V	2.5 V	1.8 V	1.5	1.2 V
Single-Ended Interfaces					
LVTTTL	✓	✓ ²	✓ ²	✓ ²	
LVC MOS33	✓	✓ ²	✓ ²	✓ ²	
LVC MOS25	✓ ²	✓	✓ ²	✓ ²	
LVC MOS18	✓ ²	✓ ²	✓	✓ ²	
LVC MOS15	✓ ²	✓ ²	✓ ²	✓	✓ ²
LVC MOS12	✓ ²	✓ ²	✓ ²	✓ ²	✓
PCI ¹	✓				
SSTL18 (Class I, Class II)	✓	✓	✓		
SSTL25 (Class I, Class II)	✓	✓			
HSTL18 (Class I, Class II)	✓	✓	✓		
Differential Interfaces					
LVDS	✓	✓			
BLVDS, MVDS, LVPECL, RS DS	✓	✓			
MIPI ³	✓	✓			
Differential SSTL18 Class I, II	✓	✓	✓		
Differential SSTL25 Class I, II	✓	✓			
Differential HSTL18 Class I, II	✓	✓	✓		

1. Bottom banks of MachXO2-640U, MachXO2-1200/U and higher density devices only.

2. Reduced functionality. Refer to TN1202, [MachXO2 sysIO Usage Guide](#) for more detail.

3. These interfaces can be emulated with external resistors in all devices.

Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
 - Watchdog timer
 - Clear timer on compare match
 - Fast PWM
 - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

Figure 2-23. Timer/Counter Block Diagram

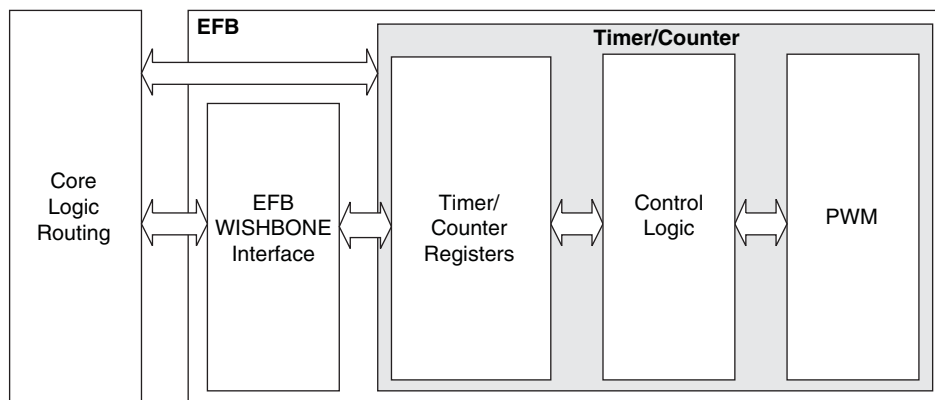


Table 2-17. Timer/Counter Signal Description

Port	I/O	Description
tc_clk	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	O	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	O	Timer counter output signal

BLVDS

The MachXO2 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

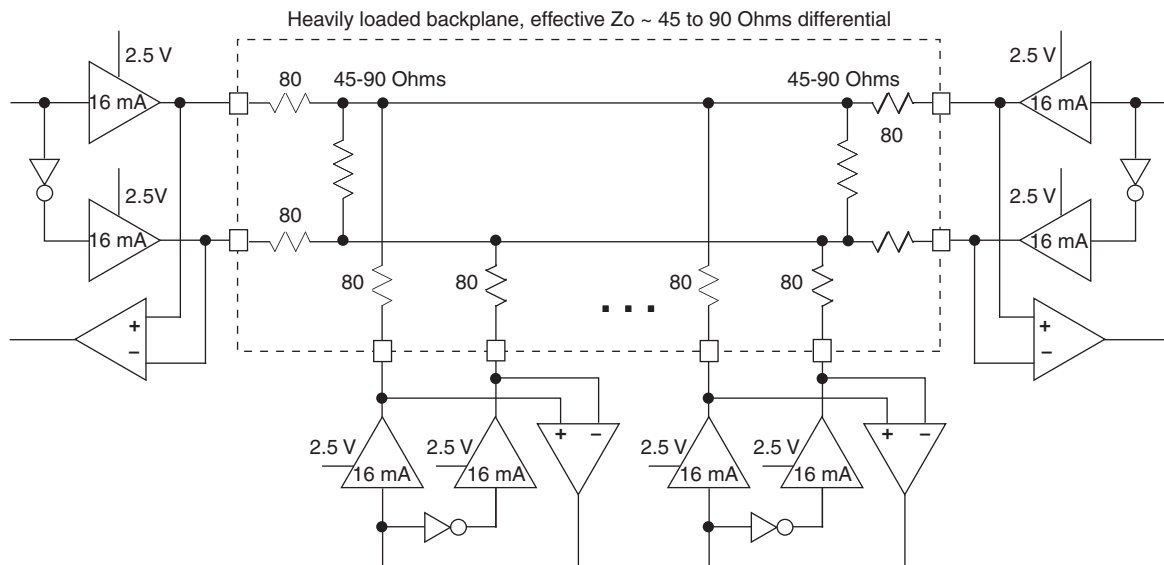


Table 3-2. BLVDS DC Conditions¹

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z _{OUT}	Output impedance	20	20	Ohms
R _S	Driver series resistance	80	80	Ohms
R _{TLEFT}	Left end termination	45	90	Ohms
R _{TRIGHT}	Right end termination	45	90	Ohms
V _{OH}	Output high voltage	1.376	1.480	V
V _{OL}	Output low voltage	1.124	1.020	V
V _{OD}	Output differential voltage	0.253	0.459	V
V _{CM}	Output common mode voltage	1.250	1.250	V
I _{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.

Typical Building Block Function Performance – ZE Devices¹

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–3 Timing	Units
Basic Functions		
16-bit decoder	13.9	ns
4:1 MUX	10.9	ns
16:1 MUX	12.0	ns

Register-to-Register Performance

Function	–3 Timing	Units
Basic Functions		
16:1 MUX	191	MHz
16-bit adder	134	MHz
16-bit counter	148	MHz
64-bit counter	77	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	90	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	214	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
LVDS25	400	MHz
LVDS25E	150	MHz
RSDS25	150	MHz
RSDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
SSTL25_I	150	MHz
SSTL25_II	150	MHz
SSTL25D_I	150	MHz
SSTL25D_II	150	MHz
SSTL18_I	150	MHz
SSTL18_II	150	MHz
SSTL18D_I	150	MHz
SSTL18D_II	150	MHz
HSTL18_I	150	MHz
HSTL18_II	150	MHz
HSTL18D_I	150	MHz
HSTL18D_II	150	MHz
PCI33	134	MHz
LVTTTL33	150	MHz
LVTTTL33D	150	MHz
LVC MOS33	150	MHz
LVC MOS33D	150	MHz
LVC MOS25	150	MHz
LVC MOS25D	150	MHz
LVC MOS25R33	150	MHz
LVC MOS18	150	MHz
LVC MOS18D	150	MHz
LVC MOS18R33	150	MHz
LVC MOS18R25	150	MHz
LVC MOS15	150	MHz
LVC MOS15D	150	MHz
LVC MOS15R33	150	MHz
LVC MOS15R25	150	MHz
LVC MOS12	91	MHz
LVC MOS12D	91	MHz

Parameter	Description	Device	-6		-5		-4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-256HC-HE	1.42	—	1.59	—	1.96	—	ns
		MachXO2-640HC-HE	1.41	—	1.58	—	1.96	—	ns
		MachXO2-1200HC-HE	1.63	—	1.79	—	2.17	—	ns
		MachXO2-2000HC-HE	1.61	—	1.76	—	2.13	—	ns
		MachXO2-4000HC-HE	1.66	—	1.81	—	2.19	—	ns
		MachXO2-7000HC-HE	1.53	—	1.67	—	2.03	—	ns
t _{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-256HC-HE	–0.24	—	–0.24	—	–0.24	—	ns
		MachXO2-640HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-1200HC-HE	–0.24	—	–0.24	—	–0.24	—	ns
		MachXO2-2000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000HC-HE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-7000HC-HE	–0.21	—	–0.21	—	–0.21	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices	—	388	—	323	—	269	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
t _{COE}	Clock to Output – PIO Output Register	MachXO2-1200HC-HE	—	7.53	—	7.76	—	8.10	ns
		MachXO2-2000HC-HE	—	7.53	—	7.76	—	8.10	ns
		MachXO2-4000HC-HE	—	7.45	—	7.68	—	8.00	ns
		MachXO2-7000HC-HE	—	7.53	—	7.76	—	8.10	ns
t _{SUE}	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
		MachXO2-2000HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
		MachXO2-4000HC-HE	–0.16	—	–0.16	—	–0.16	—	ns
		MachXO2-7000HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
t _{HE}	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	1.97	—	2.24	—	2.52	—	ns
		MachXO2-2000HC-HE	1.97	—	2.24	—	2.52	—	ns
		MachXO2-4000HC-HE	1.89	—	2.16	—	2.43	—	ns
		MachXO2-7000HC-HE	1.97	—	2.24	—	2.52	—	ns
t _{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	1.56	—	1.69	—	2.05	—	ns
		MachXO2-2000HC-HE	1.56	—	1.69	—	2.05	—	ns
		MachXO2-4000HC-HE	1.74	—	1.88	—	2.25	—	ns
		MachXO2-7000HC-HE	1.66	—	1.81	—	2.17	—	ns
t _{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-2000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000HC-HE	–0.34	—	–0.34	—	–0.34	—	ns
		MachXO2-7000HC-HE	–0.29	—	–0.29	—	–0.29	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t _{COPLL}	Clock to Output – PIO Output Register	MachXO2-1200HC-HE	—	5.97	—	6.00	—	6.13	ns
		MachXO2-2000HC-HE	—	5.98	—	6.01	—	6.14	ns
		MachXO2-4000HC-HE	—	5.99	—	6.02	—	6.16	ns
		MachXO2-7000HC-HE	—	6.02	—	6.06	—	6.20	ns
t _{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	0.36	—	0.36	—	0.65	—	ns
		MachXO2-2000HC-HE	0.36	—	0.36	—	0.63	—	ns
		MachXO2-4000HC-HE	0.35	—	0.35	—	0.62	—	ns
		MachXO2-7000HC-HE	0.34	—	0.34	—	0.59	—	ns

Parameter	Description	Device	-6		-5		-4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{HPLL}	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	0.41	—	0.48	—	0.55	—	ns
		MachXO2-2000HC-HE	0.42	—	0.49	—	0.56	—	ns
		MachXO2-4000HC-HE	0.43	—	0.50	—	0.58	—	ns
		MachXO2-7000HC-HE	0.46	—	0.54	—	0.62	—	ns
t _{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	2.88	—	3.19	—	3.72	—	ns
		MachXO2-2000HC-HE	2.87	—	3.18	—	3.70	—	ns
		MachXO2-4000HC-HE	2.96	—	3.28	—	3.81	—	ns
		MachXO2-7000HC-HE	3.05	—	3.35	—	3.87	—	ns
t _{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-2000HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-4000HC-HE	–0.87	—	–0.87	—	–0.87	—	ns
		MachXO2-7000HC-HE	–0.91	—	–0.91	—	–0.91	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Aligned ^{9, 12}									
t _{DVA}	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.317	—	0.344	—	0.368	UI
t _{DVE}	Input Data Hold After CLK		0.742	—	0.702	—	0.668	—	UI
f _{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Centered ^{9, 12}									
t _{SU}	Input Data Setup Before CLK	All MachXO2 devices, all sides	0.566	—	0.560	—	0.538	—	ns
t _{HO}	Input Data Hold After CLK		0.778	—	0.879	—	1.090	—	ns
f _{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Aligned ^{9, 12}									
t _{DVA}	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only ¹¹	—	0.316	—	0.342	—	0.364	UI
t _{DVE}	Input Data Hold After CLK		0.710	—	0.675	—	0.679	—	UI
f _{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Centered ^{9, 12}									
t _{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only ¹¹	0.233	—	0.219	—	0.198	—	ns
t _{HO}	Input Data Hold After CLK		0.287	—	0.287	—	0.344	—	ns
f _{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz

Parameter	Description	Device	-3		-2		-1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR ^{9, 12}									
t _{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. ¹³	—	0.349	—	0.381	—	0.396	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.630	—	0.613	—	UI
t _{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f _{DATA}	MEM LPDDR Serial Data Speed		—	120	—	110	—	96	Mbps
f _{SCLK}	SCLK Frequency		—	60	—	55	—	48	MHz
f _{LPDDR}	LPDDR Data Transfer Rate		0	120	0	110	0	96	Mbps
DDR ^{9, 12}									
t _{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. ¹³	—	0.347	—	0.374	—	0.393	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.637	—	0.616	—	UI
t _{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f _{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f _{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f _{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps
DDR2 ^{9, 12}									
t _{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. ¹³	—	0.372	—	0.394	—	0.410	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.690	—	0.658	—	0.618	—	UI
t _{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f _{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f _{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f _{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps

- Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
- General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pF load, fast slew rate.
- Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
- DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
- 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
- For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$.
- The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 167 ps (–3), 182 ps (–2), 195 ps (–1).
- This number for general purpose usage. Duty cycle tolerance is +/-10%.
- Duty cycle is +/- 5% for system usage.
- The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
- High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.
- Advance information for MachXO2 devices in 48 QFN packages.
- DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

Figure 3-9. GDDR71 Video Timing Waveforms

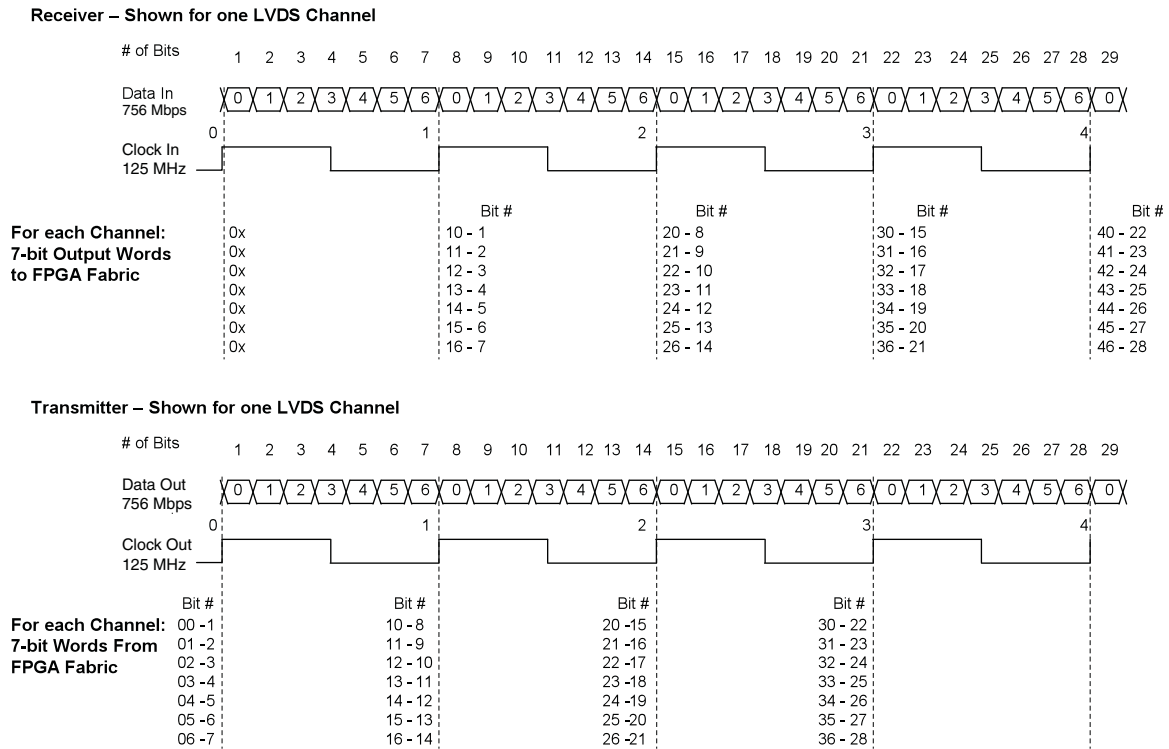


Figure 3-10. Receiver GDDR71_RX. Waveforms

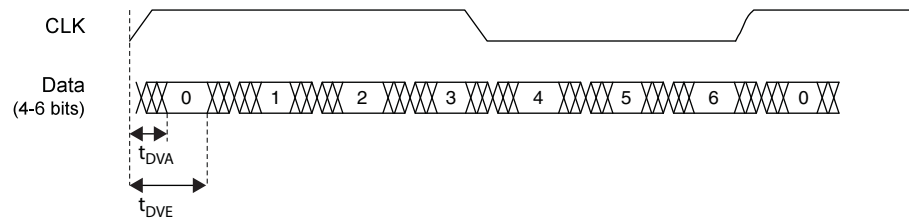
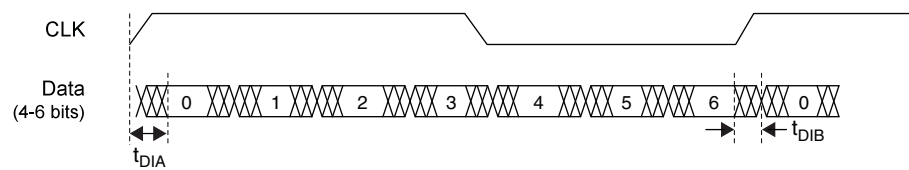


Figure 3-11. Transmitter GDDR71_TX. Waveforms



sysCLOCK PLL Timing (Continued)

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
$t_{\text{ROTATE_WD}}$	PHASESTEP Pulse Width		4	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1199, [MachXO2 sysCLOCK PLL Design and Usage Guide](#) for more details.
5. At minimum f_{PFD} . As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, or when reserved as INITn in user mode, this pin has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress. During configuration, or when reserved as DONE in user mode, this pin has an active pull-up.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.
SCL	I/O	Slave I ² C clock input and master I ² C clock output.
SDA	I/O	Slave I ² C data input and master I ² C data output.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484C	2112	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-5FG484C	2112	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-6FG484C	2112	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84C	4320	2.5 V / 3.3 V	–4	Halogen-Free QFN	84	COM
LCMXO2-4000HC-5QN84C	4320	2.5 V / 3.3 V	–5	Halogen-Free QFN	84	COM
LCMXO2-4000HC-6QN84C	4320	2.5 V / 3.3 V	–6	Halogen-Free QFN	84	COM
LCMXO2-4000HC-4MG132C	4320	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-5MG132C	4320	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-6MG132C	4320	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-4TG144C	4320	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-5TG144C	4320	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-6TG144C	4320	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-4BG256C	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-5BG256C	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-6BG256C	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-4FTG256C	4320	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-5FTG256C	4320	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-6FTG256C	4320	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-4BG332C	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-5BG332C	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-6BG332C	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-4FG484C	4320	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-5FG484C	4320	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-6FG484C	4320	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100C	2112	1.2 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-5TG100C	2112	1.2 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-6TG100C	2112	1.2 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-4TG144C	2112	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-5TG144C	2112	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-6TG144C	2112	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-4MG132C	2112	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-5MG132C	2112	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-6MG132C	2112	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-4BG256C	2112	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-5BG256C	2112	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-6BG256C	2112	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-4FTG256C	2112	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-5FTG256C	2112	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-6FTG256C	2112	1.2 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484C	2112	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-5FG484C	2112	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-6FG484C	2112	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4TG144C	4320	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-5TG144C	4320	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-6TG144C	4320	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-4MG132C	4320	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-5MG132C	4320	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-6MG132C	4320	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-4BG256C	4320	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4MG184C	4320	1.2 V	–4	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5MG184C	4320	1.2 V	–5	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-6MG184C	4320	1.2 V	–6	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5BG256C	4320	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-6BG256C	4320	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4FTG256C	4320	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-5FTG256C	4320	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-6FTG256C	4320	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-4BG332C	4320	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-5BG332C	4320	1.2 V	–5	Halogen-Free caBGA	332	COM

High Performance Industrial Grade Devices Without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100I	2112	1.2 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-5TG100I	2112	1.2 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-6TG100I	2112	1.2 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-4MG132I	2112	1.2 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-5MG132I	2112	1.2 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-6MG132I	2112	1.2 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-4TG144I	2112	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-5TG144I	2112	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-6TG144I	2112	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-4BG256I	2112	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-5BG256I	2112	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-6BG256I	2112	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-4FTG256I	2112	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-5FTG256I	2112	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-6FTG256I	2112	1.2 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484I	2112	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-5FG484I	2112	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-6FG484I	2112	1.2 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4MG132I	4320	1.2 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-5MG132I	4320	1.2 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-6MG132I	4320	1.2 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-4TG144I	4320	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-5TG144I	4320	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-6TG144I	4320	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-4MG184I	4320	1.2 V	–4	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-5MG184I	4320	1.2 V	–5	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-6MG184I	4320	1.2 V	–6	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-4BG256I	4320	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-5BG256I	4320	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-6BG256I	4320	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-4FTG256I	4320	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-5FTG256I	4320	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-6FTG256I	4320	1.2 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-4BG332I	4320	1.2 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-5BG332I	4320	1.2 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-6BG332I	4320	1.2 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-4FG484I	4320	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-5FG484I	4320	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-6FG484I	4320	1.2 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144I	6864	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-5TG144I	6864	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-6TG144I	6864	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-4BG256I	6864	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-5BG256I	6864	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-6BG256I	6864	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-4FTG256I	6864	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-5FTG256I	6864	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-6FTG256I	6864	1.2 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-4BG332I	6864	1.2 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-5BG332I	6864	1.2 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-6BG332I	6864	1.2 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-4FG484I	6864	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-5FG484I	6864	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-6FG484I	6864	1.2 V	–6	Halogen-Free fpBGA	484	IND

Date	Version	Section	Change Summary		
May 2016	3.2	All	Moved designation for 84 QFN package information from 'Advanced' to 'Final'.		
		Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 'Advanced' 48 QFN package. — Revised footnote 6. — Added footnote 9.		
		DC and Switching Characteristics	Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Added footnote 12.		
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Added footnote 12.		
		Pinout Information	Updated the Signal Descriptions section. Added information on GND signal.		
			Updated the Pinout Information Summary section. — Added 'Advanced' MachXO2-256 48 QFN values. — Added 'Advanced' MachXO2-640 48 QFN values. — Added footnote to GND. — Added footnotes 2 and 3.		
		Ordering Information	Updated the MachXO2 Part Number Description section. Added 'Advanced' SG48 package and revised footnote.		
			Updated the Ordering Information section. — Added part numbers for 'Advanced' QFN 48 package.		
March 2016	3.1	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 32 QFN value for XO2-1200. — Added 84 QFN (7 mm x 7 mm, 0.5 mm) package. — Modified package name to 100-pin TQFP. — Modified package name to 144-pin TQFP. — Added footnote.		
		Architecture	Updated the Typical I/O Behavior During Power-up section. Removed reference to TN1202.		
		DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications section. Revised t _{DPPDONE} and t _{DPPINIT} Max. values per PCN 03A-16, released March 2016.		
		Pinout Information	Updated the Pinout Information Summary section. — Added MachXO2-1200 32 QFN values. — Added 'Advanced' MachXO2-4000 84 QFN values.		
		Ordering Information	Updated the MachXO2 Part Number Description section. Added 'Advanced' QN84 package and footnote.		
			Updated the Ordering Information section. — Added part numbers for 1280 LUTs QFN 32 package. — Added part numbers for 4320 LUTs QFN 84 package.		
		March 2015	3.0	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Changed 64-ball ucBGA dimension.
				Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.