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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	32
Number of Logic Elements/Cells	256
Total RAM Bits	-
Number of I/O	40
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFNS (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-256hc-4sg48i

This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the t_{LOCK} parameter has been satisfied.

The MachXO2 also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the [sysCLOCK PLL Timing](#) table.

The MachXO2 PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the t_{LOCK} parameter has been satisfied. The timing parameters for the PLL are shown in the [sysCLOCK PLL Timing](#) table.

For more details on the PLL and the WISHBONE interface, see TN1199, [MachXO2 sysCLOCK PLL Design and Usage Guide](#).

Figure 2-7. PLL Diagram

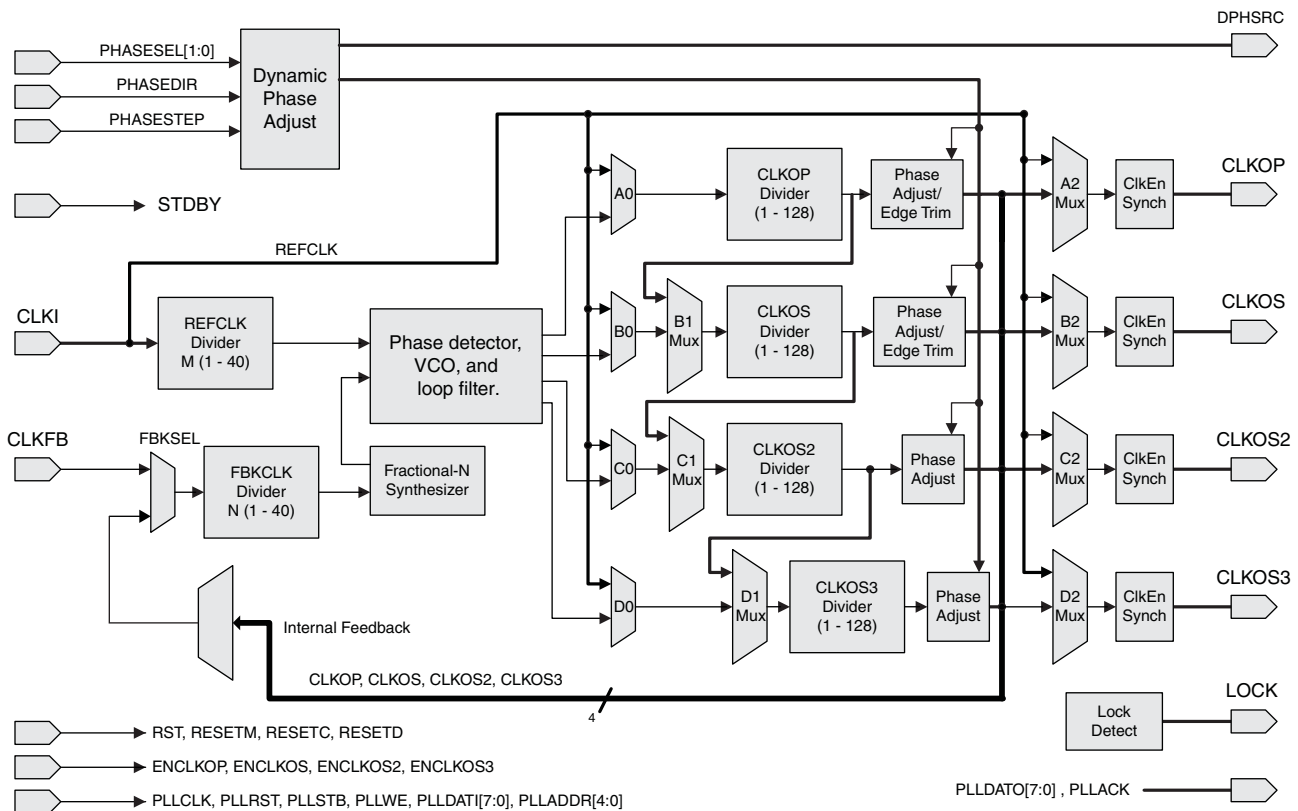


Table 2-4 provides signal descriptions of the PLL block.

Table 2-4. PLL Signal Descriptions

Port Name	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	I	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	I	Dynamic Phase step – toggle shifts VCO phase adjust by one step.

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO2 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Table 2-8. PIO Signal List

Pin Name	I/O Type	Description
CE	Input	Clock Enable
D	Input	Pin input from sysIO buffer.
INDD	Output	Register bypassed input.
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysIO Buffer
TQ	Output	Tri-state output signals to sysIO Buffer
DQSR90 ¹	Input	DQS shift 90-degree read clock
DQSW90 ¹	Input	DQS shift 90-degree write clock
DDRCLKPOL ¹	Input	DDR input register polarity control signal from DQS
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

1. Available in PIO on right edge only.

Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition to this functionality, the input register blocks for the PIOs on the right edge include built-in logic to interface to DDR memory.

Figure 2-12 shows the input register block for the PIOs located on the left, top and bottom edges. Figure 2-13 shows the input register block for the PIOs on the right edge.

Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

Table 2-18. MachXO2 Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors V _{CC} levels. In the event of unsafe V _{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).

Power On Reset

MachXO2 devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the V_{PORUP} level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices), V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators (HC devices), V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time (t_{REFRESH}) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below V_{PORDNBG} level (with the bandgap circuitry switched on) or below V_{PORDNSRAM} level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. V_{PORDNBG} and V_{PORDNSRAM} are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the V_{PORDNSRAM} reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min) they should not shut down the bandgap or POR circuit.

Power-On-Reset Voltage Levels^{1, 2, 3, 4, 5}

Symbol	Parameter	Min.	Typ.	Max.	Units
V _{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V _{CCINT} and V _{CCIO0})	0.9	—	1.06	V
V _{PORUPEXT}	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V _{CC} power supply)	1.5	—	2.1	V
V _{PORDNBG}	Power-On-Reset ramp down trip point (band gap based circuit monitoring V _{CCINT})	0.75	—	0.93	V
V _{PORDNBGEXT}	Power-On-Reset ramp down trip point (band gap based circuit monitoring V _{CC})	0.98	—	1.33	V
V _{PORDNSRAM}	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V _{CCINT})	—	0.6	—	V
V _{PORDNSRAMEXT}	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V _{CC})	—	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.
3. Note that V_{PORUP} (min.) and V_{PORDNBG} (max.) are in different process corners. For any given process corner V_{PORDNBG} (max.) is always 12.0 mV below V_{PORUP} (min.).
4. V_{PORUPEXT} is for HC devices only. In these devices a separate POR circuit monitors the external V_{CC} power supply.
5. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

Programming/Erase Specifications

Symbol	Parameter	Min.	Max. ¹	Units
N _{PROGCYC}	Flash Programming cycles per t _{RETENTION}	—	10,000	Cycles
	Flash functional programming cycles	—	100,000	
t _{RETENTION}	Data retention at 100 °C junction temperature	10	—	Years
	Data retention at 85 °C junction temperature	20	—	

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

Hot Socketing Specifications^{1, 2, 3}

Symbol	Parameter	Condition	Max.	Units
I _{DK}	Input or I/O leakage Current	0 < V _{IN} < V _{IH} (MAX)	+/-1000	μA

1. Insensitive to sequence of V_{CC} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO}.
2. 0 < V_{CC} < V_{CC} (MAX), 0 < V_{CCIO} < V_{CCIO} (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

ESD Performance

Please refer to the [MachXO2 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

Static Supply Current – ZE Devices^{1, 2, 3, 6}

Symbol	Parameter	Device	Typ. ⁴	Units
I _{CC}	Core Power Supply	LCMXO2-256ZE	18	μA
		LCMXO2-640ZE	28	μA
		LCMXO2-1200ZE	56	μA
		LCMXO2-2000ZE	80	μA
		LCMXO2-4000ZE	124	μA
		LCMXO2-7000ZE	189	μA
I _{CCIO}	Bank Power Supply ⁵ V _{CCIO} = 2.5 V	All devices	1	μA

- For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).
- Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off. To estimate the impact of turning each of these items on, please refer to the following table or for more detail with your specific design use the Power Calculator tool.
- Frequency = 0 MHz.
- T_J = 25 °C, power supplies at nominal voltage.
- Does not include pull-up/pull-down.
- To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Static Power Consumption Contribution of Different Components – ZE Devices

The table below can be used for approximating static power consumption. For a more accurate power analysis for your design please use the Power Calculator tool.

Symbol	Parameter	Typ.	Units
I _{DCBG}	Bandgap DC power contribution	101	μA
I _{DCPOR}	POR DC power contribution	38	μA
I _{DCIOBANKCONTROLLER}	DC power contribution per I/O bank controller	143	μA

sysIO Single-Ended DC Electrical Characteristics^{1, 2}

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. ⁴ (mA)	I_{OH} Max. ⁴ (mA)
	Min. (V) ³	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3 LVTTL	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
							8	-8
							12	-12
							16	-16
					24	-24		
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
							8	-8
							12	-12
							16	-16
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
							8	-8
					0.2	$V_{CCIO} - 0.2$	12	-12
							0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
							8	-8
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.2	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	4	-2
							8	-6
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5
SSTL25 Class I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCIO} - 0.62$	8	8
SSTL25 Class II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	NA	NA	NA	NA
SSTL18 Class I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.40	$V_{CCIO} - 0.40$	8	8
SSTL18 Class II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	NA	NA	NA	NA
HSTL18 Class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.40	$V_{CCIO} - 0.40$	8	8
HSTL18 Class II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS25R33	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS18R33	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS18R25	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS15R33	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS15R25	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS12R33	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain

RSDS

The MachXO2 family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

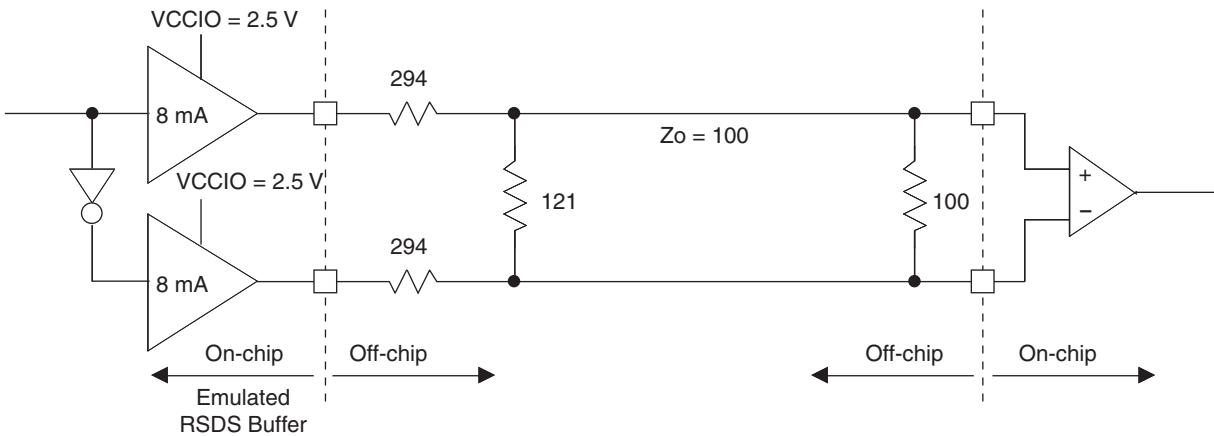


Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	294	Ohms
R_P	Driver parallel resistor	121	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	Ohms
I_{DC}	DC output current	3.66	mA

Parameter	Description	Device	-6		-5		-4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR4_RX.ECLK.Aligned^{9, 12}									
t _{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only. ¹¹	—	0.290	—	0.320	—	0.345	UI
t _{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	0.703	—	UI
f _{DATA}	DDR4 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f _{DDR4}	DDR4 ECLK Frequency		—	378	—	315	—	262	MHz
f _{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR4_RX.ECLK.Centered^{9, 12}									
t _{SU}	Input Data Setup Before ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only. ¹¹	0.233	—	0.219	—	0.198	—	ns
t _{HO}	Input Data Hold After ECLK		0.287	—	0.287	—	0.344	—	ns
f _{DATA}	DDR4 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f _{DDR4}	DDR4 ECLK Frequency		—	378	—	315	—	262	MHz
f _{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1)^{9, 12}									
t _{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only. ¹¹	—	0.290	—	0.320	—	0.345	UI
t _{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	0.703	—	UI
f _{DATA}	DDR71 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f _{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f _{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Aligned^{9, 12}									
t _{DIA}	Output Data Invalid After CLK Output	All MachXO2 devices, all sides.	—	0.520	—	0.550	—	0.580	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.520	—	0.550	—	0.580	ns
f _{DATA}	DDR1 Output Data Speed		—	300	—	250	—	208	Mbps
f _{DDR1}	DDR1 SCLK frequency		—	150	—	125	—	104	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Centered^{9, 12}									
t _{DVB}	Output Data Valid Before CLK Output	All MachXO2 devices, all sides.	1.210	—	1.510	—	1.870	—	ns
t _{DVA}	Output Data Valid After CLK Output		1.210	—	1.510	—	1.870	—	ns
f _{DATA}	DDR1 Output Data Speed		—	300	—	250	—	208	Mbps
f _{DDR1}	DDR1 SCLK Frequency (minimum limited by PLL)		—	150	—	125	—	104	MHz
Generic DDR2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_TX.ECLK.Aligned^{9, 12}									
t _{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f _{DATA}	DDR2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f _{DDR2}	DDR2 ECLK frequency		—	332	—	277	—	231	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz

Parameter	Description	Device	-6		-5		-4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR2_TX.ECLK.Centered^{9, 12}									
t _{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.535	—	0.670	—	0.830	—	ns
t _{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	0.830	—	ns
f _{DATA}	DDR2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f _{DDR2}	DDR2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	—	231	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR4_TX.ECLK.Aligned^{9, 12}									
t _{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f _{DATA}	DDR4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f _{DDR4}	DDR4 ECLK Frequency		—	378	—	315	—	262	MHz
f _{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR4_TX.ECLK.Centered^{9, 12}									
t _{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.455	—	0.570	—	0.710	—	ns
t _{DVA}	Output Data Valid After CLK Output		0.455	—	0.570	—	0.710	—	ns
f _{DATA}	DDR4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f _{DDR4}	DDR4 ECLK Frequency (minimum limited by PLL)		—	378	—	315	—	262	MHz
f _{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1^{9, 12}									
t _{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.160	—	0.180	—	0.200	ns
t _{DIA}	Output Data Invalid After CLK Output		—	0.160	—	0.180	—	0.200	ns
f _{DATA}	DDR71 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f _{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f _{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz

Parameter	Description	Device	-3		-2		-1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{HPLL}	Clock to Data Hold – PIO Input Register	MachXO2-1200ZE	0.66	—	0.68	—	0.80	—	ns
		MachXO2-2000ZE	0.68	—	0.70	—	0.83	—	ns
		MachXO2-4000ZE	0.68	—	0.71	—	0.84	—	ns
		MachXO2-7000ZE	0.73	—	0.74	—	0.87	—	ns
t _{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200ZE	5.14	—	5.69	—	6.20	—	ns
		MachXO2-2000ZE	5.11	—	5.67	—	6.17	—	ns
		MachXO2-4000ZE	5.27	—	5.84	—	6.35	—	ns
		MachXO2-7000ZE	5.15	—	5.71	—	6.23	—	ns
t _{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200ZE	-1.36	—	-1.36	—	-1.36	—	ns
		MachXO2-2000ZE	-1.35	—	-1.35	—	-1.35	—	ns
		MachXO2-4000ZE	-1.43	—	-1.43	—	-1.43	—	ns
		MachXO2-7000ZE	-1.41	—	-1.41	—	-1.41	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Aligned^{9,12}									
t _{DVA}	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.382	—	0.401	—	0.417	UI
t _{DVE}	Input Data Hold After CLK		0.670	—	0.684	—	0.693	—	UI
f _{DATA}	DDR1 Input Data Speed		—	140	—	116	—	98	Mbps
f _{DDR1}	DDR1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Centered^{9,12}									
t _{SU}	Input Data Setup Before CLK	All MachXO2 devices, all sides	1.319	—	1.412	—	1.462	—	ns
t _{HO}	Input Data Hold After CLK		0.717	—	1.010	—	1.340	—	ns
f _{DATA}	DDR1 Input Data Speed		—	140	—	116	—	98	Mbps
f _{DDR1}	DDR1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Aligned^{9,12}									
t _{DVA}	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only ¹¹	—	0.361	—	0.346	—	0.334	UI
t _{DVE}	Input Data Hold After CLK		0.602	—	0.625	—	0.648	—	UI
f _{DATA}	DDR2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f _{DDR2}	DDR2 ECLK Frequency		—	140	—	117	—	97	MHz
f _{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Centered^{9,12}									
t _{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only ¹¹	0.472	—	0.672	—	0.865	—	ns
t _{HO}	Input Data Hold After CLK		0.363	—	0.501	—	0.743	—	ns
f _{DATA}	DDR2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f _{DDR2}	DDR2 ECLK Frequency		—	140	—	117	—	97	MHz
f _{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input - GDDR4_RX.ECLK.Aligned^{9,12}									
t _{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only ¹¹	—	0.307	—	0.316	—	0.326	UI
t _{DVE}	Input Data Hold After ECLK		0.662	—	0.650	—	0.649	—	UI
f _{DATA}	DDR4 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f _{DDR4}	DDR4 ECLK Frequency		—	210	—	176	—	146	MHz
f _{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz

Figure 3-9. GDDR71 Video Timing Waveforms

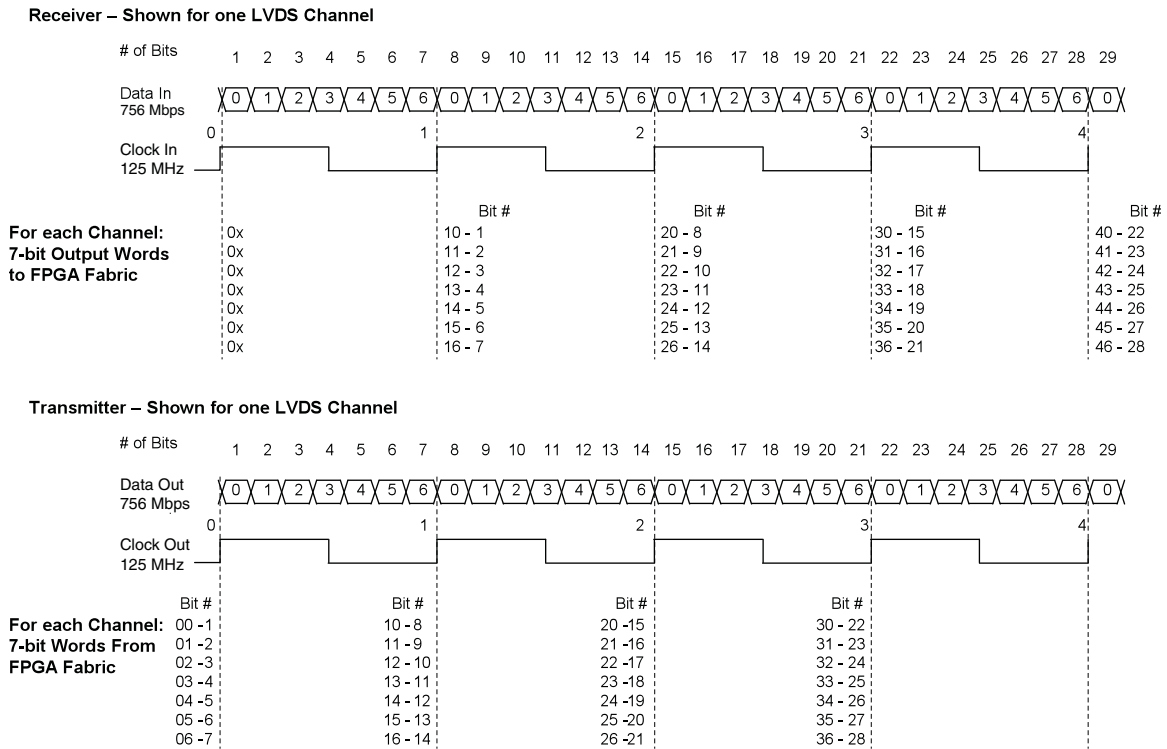


Figure 3-10. Receiver GDDR71_RX. Waveforms

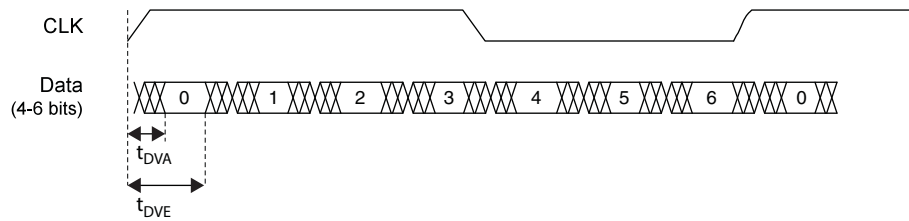
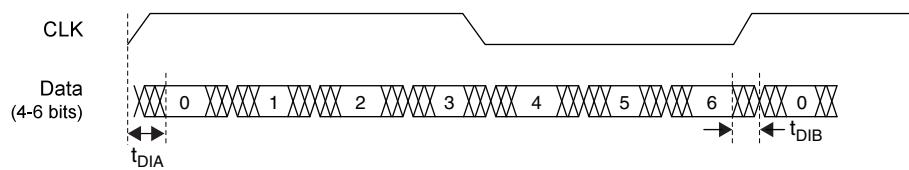


Figure 3-11. Transmitter GDDR71_TX. Waveforms



sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)		1.5625	400	MHz
f_{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f_{VCO}	PLL VCO Frequency		200	800	MHz
f_{PFD}	Phase Detector Input Frequency		7	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Without duty trim selected ³	45	55	%
$t_{DT_TRIM}^7$	Edge Duty Trim Accuracy		-75	75	%
t_{PH}^4	Output Phase Accuracy		-6	6	%
$t_{OPJIT}^{1,8}$	Output Clock Period Jitter	$f_{OUT} > 100$ MHz	—	150	ps p-p
		$f_{OUT} < 100$ MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	$f_{OUT} > 100$ MHz	—	180	ps p-p
		$f_{OUT} < 100$ MHz	—	0.009	UIPP
	Output Clock Phase Jitter	$f_{PFD} > 100$ MHz	—	160	ps p-p
		$f_{PFD} < 100$ MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	$f_{OUT} > 100$ MHz	—	230	ps p-p
		$f_{OUT} < 100$ MHz	—	0.12	UIPP
Output Clock Cycle-to-cycle Jitter (Fractional-N)	$f_{OUT} > 100$ MHz	—	230	ps p-p	
	$f_{OUT} < 100$ MHz	—	0.12	UIPP	
t_{SPO}	Static Phase Offset	Divider ratio = integer	-120	120	ps
t_W	Output Clock Pulse Width	At 90% or 10% ³	0.9	—	ns
$t_{LOCK}^{2,5}$	PLL Lock-in Time		—	15	ms
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}^6	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{STABLE}^5	STANDBY High to PLL Stable		—	15	ms
t_{RST}	RST/RESETM Pulse Width		1	—	ns
t_{RSTREC}	RST Recovery Time		1	—	ns
t_{RST_DIV}	RESETC/D Pulse Width		10	—	ns
t_{RSTREC_DIV}	RESETC/D Recovery Time		1	—	ns
$t_{ROTATE-SETUP}$	PHASESTEP Setup Time		10	—	ns

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144C	6864	1.2 V	-1	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-2TG144C	6864	1.2 V	-2	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-3TG144C	6864	1.2 V	-3	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-1BG256C	6864	1.2 V	-1	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-2BG256C	6864	1.2 V	-2	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-3BG256C	6864	1.2 V	-3	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-1FTG256C	6864	1.2 V	-1	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-2FTG256C	6864	1.2 V	-2	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-3FTG256C	6864	1.2 V	-3	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-1BG332C	6864	1.2 V	-1	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-2BG332C	6864	1.2 V	-2	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-3BG332C	6864	1.2 V	-3	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-1FG484C	6864	1.2 V	-1	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-2FG484C	6864	1.2 V	-2	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-3FG484C	6864	1.2 V	-3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100CR1 ¹	1280	1.2 V	-1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100CR1 ¹	1280	1.2 V	-2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100CR1 ¹	1280	1.2 V	-3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132CR1 ¹	1280	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132CR1 ¹	1280	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132CR1 ¹	1280	1.2 V	-3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144CR1 ¹	1280	1.2 V	-1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144CR1 ¹	1280	1.2 V	-2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144CR1 ¹	1280	1.2 V	-3	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200ZE-speed package CR1” are the same as the “LCMXO2-1200ZE-speed package C” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100C	2112	1.2 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-5TG100C	2112	1.2 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-6TG100C	2112	1.2 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-4TG144C	2112	1.2 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-5TG144C	2112	1.2 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-6TG144C	2112	1.2 V	-6	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-4MG132C	2112	1.2 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-5MG132C	2112	1.2 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-6MG132C	2112	1.2 V	-6	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-4BG256C	2112	1.2 V	-4	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-5BG256C	2112	1.2 V	-5	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-6BG256C	2112	1.2 V	-6	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-4FTG256C	2112	1.2 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-5FTG256C	2112	1.2 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-6FTG256C	2112	1.2 V	-6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484C	2112	1.2 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-5FG484C	2112	1.2 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-6FG484C	2112	1.2 V	-6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4TG144C	4320	1.2 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-5TG144C	4320	1.2 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-6TG144C	4320	1.2 V	-6	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-4MG132C	4320	1.2 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-5MG132C	4320	1.2 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-6MG132C	4320	1.2 V	-6	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-4BG256C	4320	1.2 V	-4	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4MG184C	4320	1.2 V	-4	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5MG184C	4320	1.2 V	-5	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-6MG184C	4320	1.2 V	-6	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5BG256C	4320	1.2 V	-5	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-6BG256C	4320	1.2 V	-6	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4FTG256C	4320	1.2 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-5FTG256C	4320	1.2 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-6FTG256C	4320	1.2 V	-6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-4BG332C	4320	1.2 V	-4	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-5BG332C	4320	1.2 V	-5	Halogen-Free caBGA	332	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32I	1280	2.5 V / 3.3 V	-4	Halogen-Free QFN	32	IND
LCMXO2-1200HC-5SG32I	1280	2.5 V / 3.3 V	-5	Halogen-Free QFN	32	IND
LCMXO2-1200HC-6SG32I	1280	2.5 V / 3.3 V	-6	Halogen-Free QFN	32	IND
LCMXO2-1200HC-4TG100I	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100I	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100I	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132I	1280	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132I	1280	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132I	1280	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144I	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144I	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144I	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256I	1280	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-5FTG256I	1280	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-6FTG256I	1280	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100I	2112	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-5TG100I	2112	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-6TG100I	2112	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-4MG132I	2112	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-5MG132I	2112	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-6MG132I	2112	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-4TG144I	2112	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-5TG144I	2112	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-6TG144I	2112	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-4BG256I	2112	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-5BG256I	2112	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-6BG256I	2112	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-4FTG256I	2112	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-5FTG256I	2112	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-6FTG256I	2112	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484I	2112	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-5FG484I	2112	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-6FG484I	2112	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	IND

R1 Device Specifications

The LCMXO2-1200ZE/HC “R1” devices have the same specifications as their Standard (non-R1) counterparts except as listed below. For more details on the R1 to Standard migration refer to AN8086, [Designing for Migration from MachXO2-1200-R1 to Standard Non-R1\) Devices](#).

- The User Flash Memory (UFM) cannot be programmed through the internal WISHBONE interface. It can still be programmed through the JTAG/SPI/I²C ports.
- The on-chip differential input termination resistor value is higher than intended. It is approximately 200Ω as opposed to the intended 100Ω. It is recommended to use external termination resistors for differential inputs. The on-chip termination resistors can be disabled through Lattice design software.
- Soft Error Detection logic may not produce the correct result when it is run for the first time after configuration. To use this feature, discard the result from the first operation. Subsequent operations will produce the correct result.
- Under certain conditions, I_{IH} exceeds data sheet specifications. The following table provides more details:

Condition	Clamp	Pad Rising I _{IH} Max.	Pad Falling I _{IH} Min.	Steady State Pad High I _{IH}	Steady State Pad Low I _{IL}
VPAD > VCCIO	OFF	1 mA	-1 mA	1 mA	10 μA
VPAD = VCCIO	ON	10 μA	-10 μA	10 μA	10 μA
VPAD = VCCIO	OFF	1 mA	-1 mA	1 mA	10 μA
VPAD < VCCIO	OFF	10 μA	-10 μA	10 μA	10 μA

- The user SPI interface does not operate correctly in some situations. During master read access and slave write access, the last byte received does not generate the RRDY interrupt.
- In GDDR2, GDDR4 and GDDR71 modes, ECLKSYNC may have a glitch in the output under certain conditions, leading to possible loss of synchronization.
- When using the hard I²C IP core, the I²C status registers I2C_1_SR and I2C_2_SR may not update correctly.
- PLL Lock signal will glitch high when coming out of standby. This glitch lasts for about 10 μsec before returning low.
- Dual boot only available on HC devices, requires tying VCC and VCCIO2 to the same 3.3 V or 2.5 V supply.

Date	Version	Section	Change Summary
December 2014	2.9	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Removed XO2-4000U data. — Removed 400-ball ftBGA. — Removed 25-ball WLCSP value for XO2-2000U.
		DC and Switching Characteristics	Updated the Recommended Operating Conditions section. Adjusted Max. values for V_{CC} and V_{CCIO} . Updated the sysIO Recommended Operating Conditions section. Adjusted Max. values for LVCMOS 3.3, LVTTTL, PCI, LVDS33 and LVPECL.
		Pinout Information	Updated the Pinout Information Summary section. Removed MachXO2-4000U.
		Ordering Information	Updated the MachXO2 Part Number Description section. Removed BG400 package.
			Updated the High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers. Updated the High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
November 2014	2.8	Introduction	Updated the Features section. — Revised I/Os under Flexible Logic Architecture. — Revised standby power under Ultra Low Power Devices. — Revise input frequency range under Flexible On-Chip Clocking.
			Updated Table 1-1, MachXO2 Family Selection Guide. — Added XO2-4000U data. — Removed HE and ZE device options for XO2-4000. — Added 400-ball ftBGA.
		Pinout Information	Updated the Pinout Information Summary section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added BG400 package.
Updated the Ordering Information section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400 part numbers.			
October 2014	2.7	Ordering Information	Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Fixed typo in LCMXO2-2000ZE-1UWG49ITR part number package.
		Architecture	Updated the Supported Standards section. Added MIPI information to Table 2-12. Supported Input Standards and Table 2-13. Supported Output Standards.
		DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition.
Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition. Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.			
July 2014	2.6	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics ^{1,2} section. Updated footnote 4.
			Updated Register-to-Register Performance section. Updated footnote.
		Ordering Information	Updated UW49 package to UWG49 in MachXO2 Part Number Description.
Updated LCMXO2-2000ZE-1UWG49CTR package in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging.			

Date	Version	Section	Change Summary
January 2013	02.0	Introduction	Updated the total number IOs to include JTAGENB.
		Architecture	Supported Output Standards table – Added 3.3 V _{CCIO} (Typ.) to LVDS row.
			Changed SRAM CRC Error Detection to Soft Error Detection.
		DC and Switching Characteristics	Power Supply Ramp Rates table – Updated Units column for t _{RAMP} symbol.
			Added new Maximum sysIO Buffer Performance table.
			sysCLOCK PLL Timing table – Updated Min. column values for f _{IN} , f _{OUT} , f _{OUT2} and f _{PFD} parameters. Added t _{SPO} parameter. Updated footnote 6.
			MachXO2 Oscillator Output Frequency table – Updated symbol name for t _{STABLEOSC} .
			DC Electrical Characteristics table – Updated conditions for I _{IL} , I _{IH} symbols.
			Corrected parameters tDQVBS and tDQVAS
			Corrected MachXO2 ZE parameters tDVADQ and tDVEDQ
		Pinout Information	Included the MachXO2-4000HE 184 csBGA package.
Ordering Information	Updated part number.		
April 2012	01.9	Architecture	Removed references to TN1200.
		Ordering Information	Updated the Device Status portion of the MachXO2 Part Number Description to include the 50 parts per reel for the WLCSP package.
			Added new part number and footnote 2 for LCMXO2-1200ZE-1UWG25ITR50.
			Updated footnote 1 for LCMXO2-1200ZE-1UWG25ITR.
Supplemental Information	Removed references to TN1200.		
March 2012	01.8	Introduction	Added 32 QFN packaging information to Features bullets and MachXO2 Family Selection Guide table.
		DC and Switching Characteristics	Changed ‘STANDBY’ to ‘USERSTDBY’ in Standby Mode timing diagram.
		Pinout Information	Removed footnote from Pin Information Summary tables.
			Added 32 QFN package to Pin Information Summary table.
		Ordering Information	Updated Part Number Description and Ordering Information tables for 32 QFN package.
	Updated topside mark diagram in the Ordering Information section.		

Date	Version	Section	Change Summary
February 2012	01.7	All	Updated document with new corporate logo.
		01.6	Data sheet status changed from preliminary to final.
	DC and Switching Characteristics	Introduction	MachXO2 Family Selection Guide table – Removed references to 49-ball WLCSP.
		Updated Flash Download Time table.	
		Modified Storage Temperature in the Absolute Maximum Ratings section.	
		Updated I _{DK} max in Hot Socket Specifications table.	
		Modified Static Supply Current tables for ZE and HC/HE devices.	
		Updated Power Supply Ramp Rates table.	
		Updated Programming and Erase Supply Current tables.	
		Updated data in the External Switching Characteristics table.	
		Corrected Absolute Maximum Ratings for Dedicated Input Voltage Applied for LCMXO2 HC.	
		DC Electrical Characteristics table – Minor corrections to conditions for I _{IL} , I _{IH} .	
	Pinout Information	Removed references to 49-ball WLCSP.	
Signal Descriptions table – Updated description for GND, VCC, and VCCIOx.			
Updated Pin Information Summary table – Number of VCCIOs, GNDs, VCCs, and Total Count of Bonded Pins for MachXO2-256, 640, and 640U and Dual Function I/O for MachXO2-4000 332caBGA.			
Ordering Information	Removed references to 49-ball WLCSP		
August 2011	01.5	DC and Switching Characteristics	Updated ESD information.
		Ordering Information	Updated footnote for ordering WLCSP devices.
	01.4	Architecture	Updated information in Clock/Control Distribution Network and sys-CLOCK Phase Locked Loops (PLLs).
		DC and Switching Characteristics	Updated I _{IL} and I _{IH} conditions in the DC Electrical Characteristics table.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Updated Pin Information Summary table: Dual Function I/O, DQS Groups Bank 1, Total General Purpose Single-Ended I/O, Differential I/O Per Bank, Total Count of Bonded Pins, Gearboxes.
			Added column of data for MachXO2-2000 49 WLCSP.
		Ordering Information	Updated R1 Device Specifications text section with information on migration from MachXO2-1200-R1 to Standard (non-R1) devices.
			Corrected Supply Voltage typo for part numbers: LCMX02-2000UHE-4FG484I, LCMX02-2000UHE-5FG484I, LCMX02-2000UHE-6FG484I.
			Added footnote for WLCSP package parts.
Supplemental Information	Removed reference to Stand-alone Power Calculator for MachXO2 Devices. Added reference to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices.		