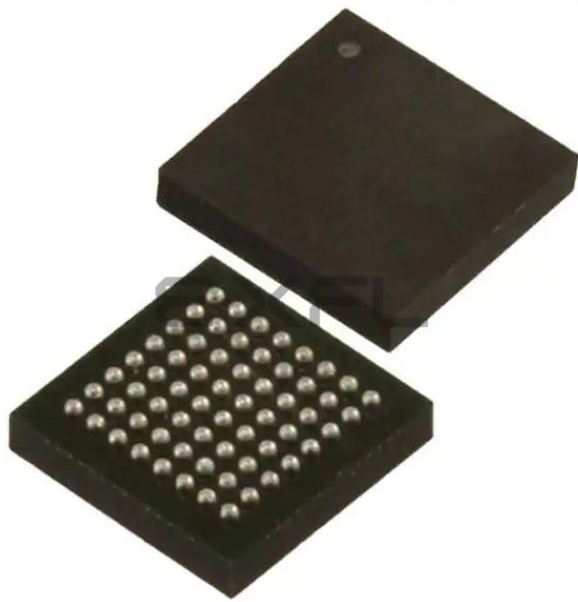




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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details                        |                                                                                                                                                                               |
|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Active                                                                                                                                                                        |
| Number of LABs/CLBs            | 32                                                                                                                                                                            |
| Number of Logic Elements/Cells | 256                                                                                                                                                                           |
| Total RAM Bits                 | -                                                                                                                                                                             |
| Number of I/O                  | 44                                                                                                                                                                            |
| Number of Gates                | -                                                                                                                                                                             |
| Voltage - Supply               | 2.375V ~ 3.465V                                                                                                                                                               |
| Mounting Type                  | Surface Mount                                                                                                                                                                 |
| Operating Temperature          | 0°C ~ 85°C (TJ)                                                                                                                                                               |
| Package / Case                 | 64-VFBGA                                                                                                                                                                      |
| Supplier Device Package        | 64-UCBGA (4x4)                                                                                                                                                                |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmx02-256hc-4umg64c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmx02-256hc-4umg64c</a> |

**Table 1-1. MachXO2™ Family Selection Guide**

|                                                         |                 | XO2-256   | XO2-640 | XO2-640U <sup>1</sup> | XO2-1200 | XO2-1200U <sup>1</sup> | XO2-2000 | XO2-2000U <sup>1</sup> | XO2-4000 | XO2-7000 |
|---------------------------------------------------------|-----------------|-----------|---------|-----------------------|----------|------------------------|----------|------------------------|----------|----------|
| LUTs                                                    |                 | 256       | 640     | 640                   | 1280     | 1280                   | 2112     | 2112                   | 4320     | 6864     |
| Distributed RAM (kbits)                                 |                 | 2         | 5       | 5                     | 10       | 10                     | 16       | 16                     | 34       | 54       |
| EBR SRAM (kbits)                                        |                 | 0         | 18      | 64                    | 64       | 74                     | 74       | 92                     | 92       | 240      |
| Number of EBR SRAM Blocks (9 kbits/block)               |                 | 0         | 2       | 7                     | 7        | 8                      | 8        | 10                     | 10       | 26       |
| UFM (kbits)                                             |                 | 0         | 24      | 64                    | 64       | 80                     | 80       | 96                     | 96       | 256      |
| Device Options:                                         | HC <sup>2</sup> | Yes       | Yes     | Yes                   | Yes      | Yes                    | Yes      | Yes                    | Yes      | Yes      |
|                                                         | HE <sup>3</sup> |           |         |                       |          |                        | Yes      | Yes                    | Yes      | Yes      |
|                                                         | ZE <sup>4</sup> | Yes       | Yes     |                       | Yes      |                        | Yes      |                        | Yes      | Yes      |
| Number of PLLs                                          |                 | 0         | 0       | 1                     | 1        | 1                      | 1        | 2                      | 2        | 2        |
| Hardened Functions:                                     | I2C             | 2         | 2       | 2                     | 2        | 2                      | 2        | 2                      | 2        | 2        |
|                                                         | SPI             | 1         | 1       | 1                     | 1        | 1                      | 1        | 1                      | 1        | 1        |
|                                                         | Timer/Counter   | 1         | 1       | 1                     | 1        | 1                      | 1        | 1                      | 1        | 1        |
| <b>Packages</b>                                         |                 | <b>IO</b> |         |                       |          |                        |          |                        |          |          |
| 25-ball WLCSP <sup>5</sup><br>(2.5 mm x 2.5 mm, 0.4 mm) |                 |           |         |                       | 18       |                        |          |                        |          |          |
| 32 QFN <sup>6</sup><br>(5 mm x 5 mm, 0.5 mm)            |                 | 21        |         |                       | 21       |                        |          |                        |          |          |
| 48 QFN <sup>8,9</sup><br>(7 mm x 7 mm, 0.5 mm)          |                 | 40        | 40      |                       |          |                        |          |                        |          |          |
| 49-ball WLCSP <sup>5</sup><br>(3.2 mm x 3.2 mm, 0.4 mm) |                 |           |         |                       |          |                        | 38       |                        |          |          |
| 64-ball ucBGA<br>(4 mm x 4 mm, 0.4 mm)                  |                 | 44        |         |                       |          |                        |          |                        |          |          |
| 84 QFN <sup>7</sup><br>(7 mm x 7 mm, 0.5 mm)            |                 |           |         |                       |          |                        |          |                        | 68       |          |
| 100-pin TQFP<br>(14 mm x 14 mm)                         |                 | 55        | 78      |                       | 79       |                        | 79       |                        |          |          |
| 132-ball csBGA<br>(8 mm x 8 mm, 0.5 mm)                 |                 | 55        | 79      |                       | 104      |                        | 104      |                        | 104      |          |
| 144-pin TQFP<br>(20 mm x 20 mm)                         |                 |           |         | 107                   | 107      |                        | 111      |                        | 114      | 114      |
| 184-ball csBGA <sup>7</sup><br>(8 mm x 8 mm, 0.5 mm)    |                 |           |         |                       |          |                        |          |                        | 150      |          |
| 256-ball caBGA<br>(14 mm x 14 mm, 0.8 mm)               |                 |           |         |                       |          |                        | 206      |                        | 206      | 206      |
| 256-ball ftBGA<br>(17 mm x 17 mm, 1.0 mm)               |                 |           |         |                       |          | 206                    | 206      |                        | 206      | 206      |
| 332-ball caBGA<br>(17 mm x 17 mm, 0.8 mm)               |                 |           |         |                       |          |                        |          |                        | 274      | 278      |
| 484-ball ftBGA<br>(23 mm x 23 mm, 1.0 mm)               |                 |           |         |                       |          |                        | 278      |                        | 278      | 334      |

1. Ultra high I/O device.
2. High performance with regulator – VCC = 2.5 V, 3.3 V
3. High performance without regulator – V<sub>CC</sub> = 1.2 V
4. Low power without regulator – V<sub>CC</sub> = 1.2 V
5. WLCSP package only available for ZE devices.
6. 32 QFN package only available for HC and ZE devices.
7. 184 csBGA package only available for HE devices.
8. 48-pin QFN information is 'Advanced'.
9. 48 QFN package only available for HC devices.

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2-640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

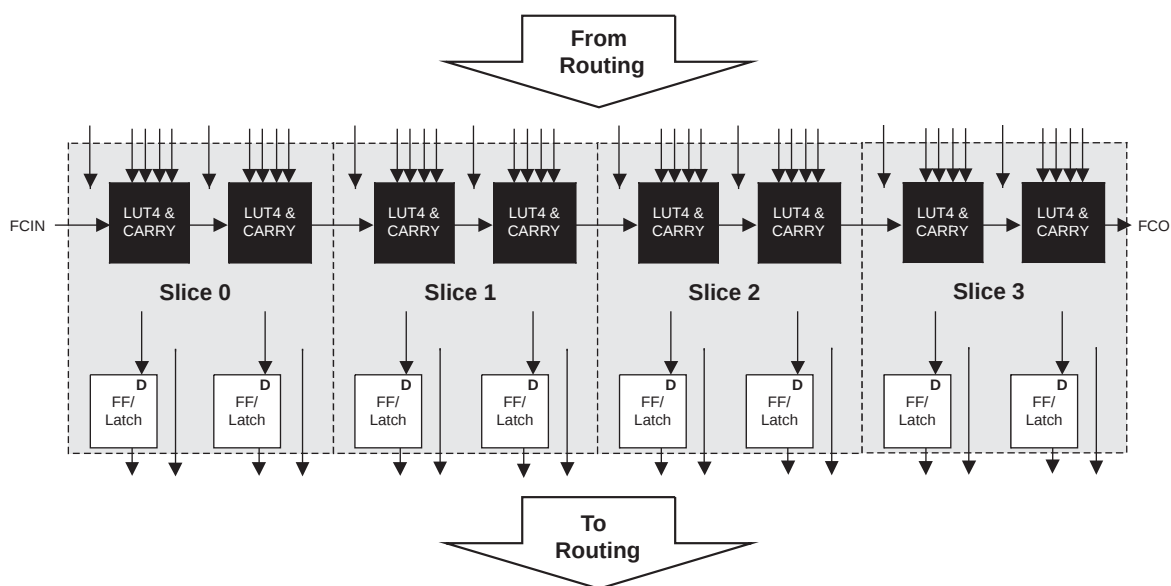
MachXO2 devices provide commonly used hardened functions such as SPI controller, I<sup>2</sup>C controller and timer/counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I<sup>2</sup>C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

## **PFU Blocks**

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

**Figure 2-3. PFU Block Diagram**



## Slices

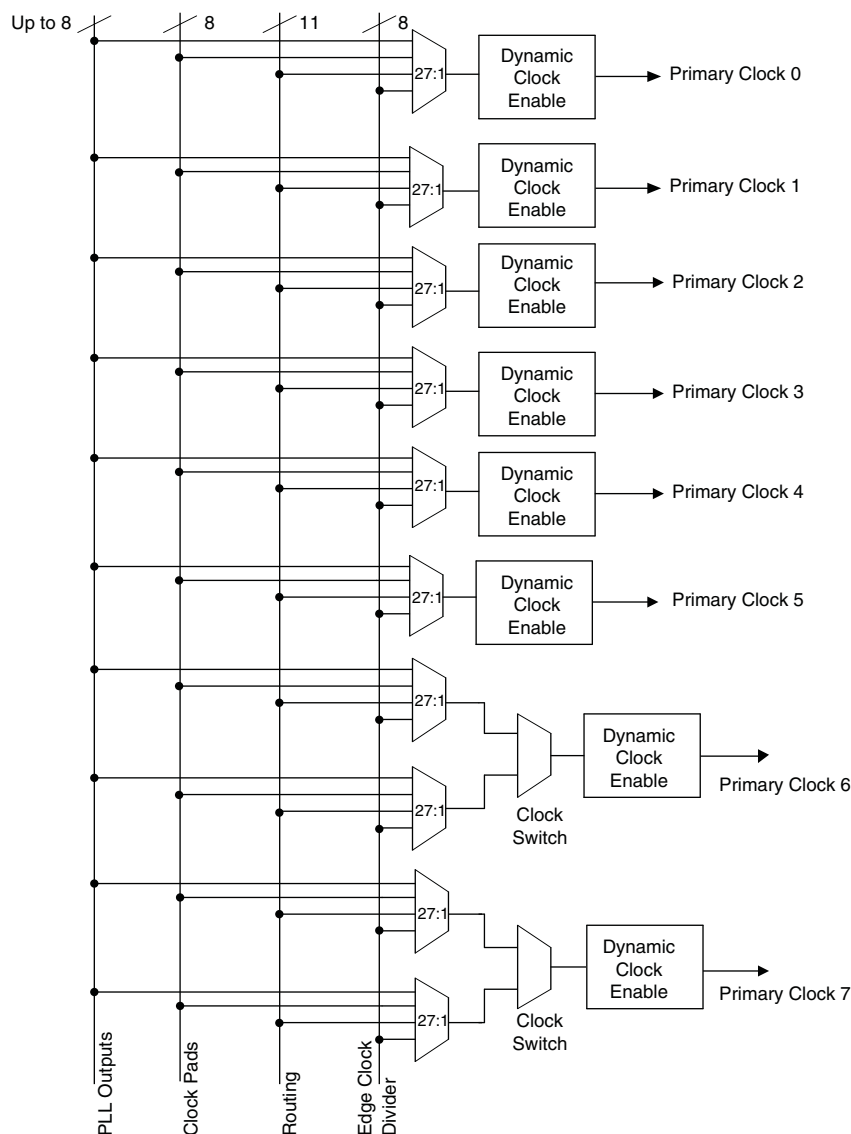
Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

**Table 2-1. Resources and Modes Available per Slice**

| Slice   | PFU Block               |                         |
|---------|-------------------------|-------------------------|
|         | Resources               | Modes                   |
| Slice 0 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 1 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 2 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 3 | 2 LUT4s and 2 Registers | Logic, Ripple, ROM      |

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.

**Figure 2-5. Primary Clocks for MachXO2 Devices**

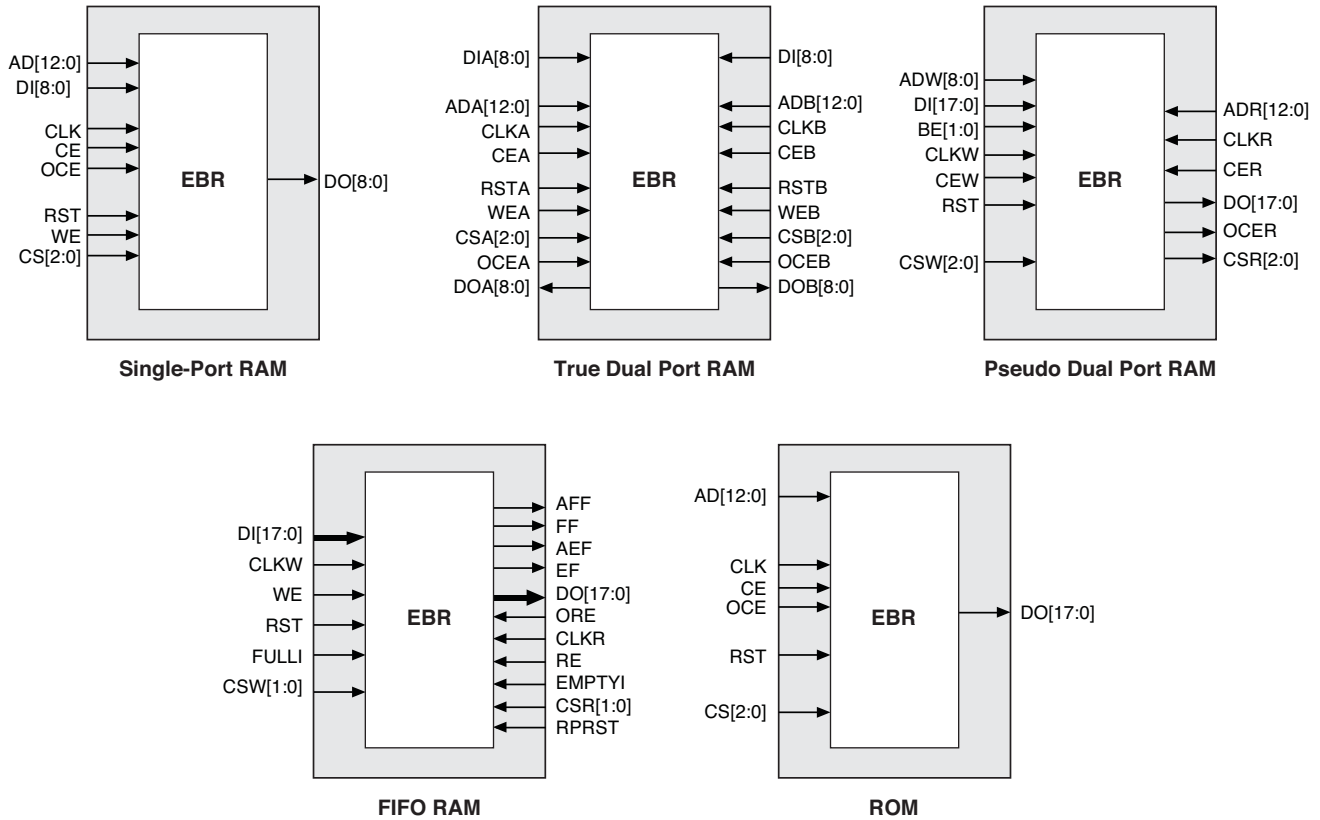


Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO2 External Switching Characteristics table.

**Figure 2-8. sysMEM Memory Primitives**



**Table 2-6. EBR Signal Descriptions**

| Port Name        | Description                 | Active State      |
|------------------|-----------------------------|-------------------|
| CLK              | Clock                       | Rising Clock Edge |
| CE               | Clock Enable                | Active High       |
| OCE <sup>1</sup> | Output Clock Enable         | Active High       |
| RST              | Reset                       | Active High       |
| BE <sup>1</sup>  | Byte Enable                 | Active High       |
| WE               | Write Enable                | Active High       |
| AD               | Address Bus                 | —                 |
| DI               | Data In                     | —                 |
| DO               | Data Out                    | —                 |
| CS               | Chip Select                 | Active High       |
| AFF              | FIFO RAM Almost Full Flag   | —                 |
| FF               | FIFO RAM Full Flag          | —                 |
| AEF              | FIFO RAM Almost Empty Flag  | —                 |
| EF               | FIFO RAM Empty Flag         | —                 |
| RPRST            | FIFO RAM Read Pointer Reset | —                 |

1. Optional signals.

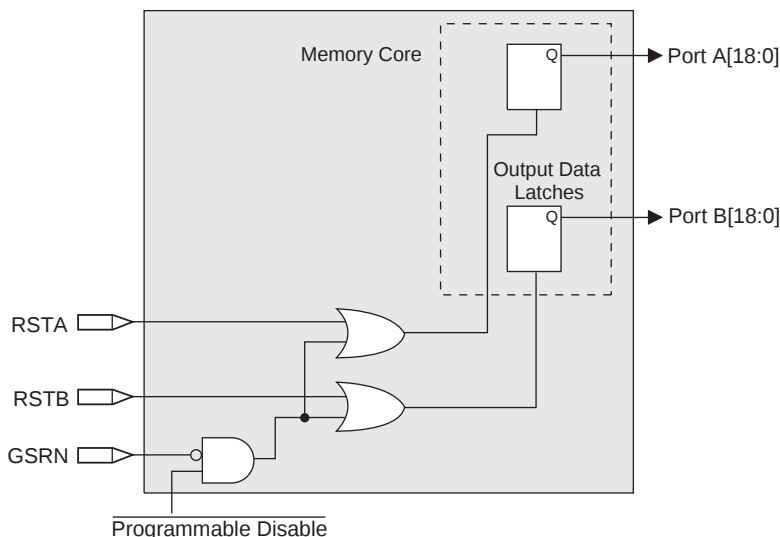
2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.

3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.

4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).

5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

**Figure 2-9. Memory Core Reset**

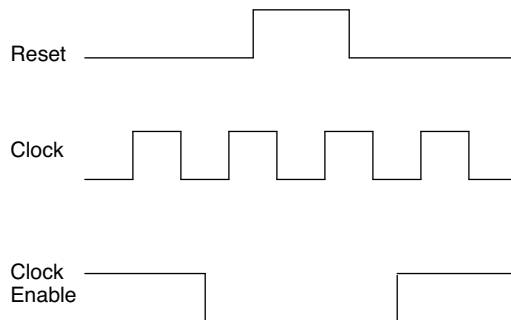


For further information on the sysMEM EBR block, please refer to TN1201, [Memory Usage Guide for MachXO2 Devices](#).

### EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

**Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram**



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of  $1/f_{MAX}$  (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-10. The reset timing rules apply to the RPRreset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPRreset are always asynchronous EBR inputs. For more details refer to TN1201, [Memory Usage Guide for MachXO2 Devices](#).

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

### Static Supply Current – HC/HE Devices<sup>1, 2, 3, 6</sup>

| Symbol     | Parameter                                                   | Device         | Typ. <sup>4</sup> | Units |
|------------|-------------------------------------------------------------|----------------|-------------------|-------|
| $I_{CC}$   | Core Power Supply                                           | LCMXO2-256HC   | 1.15              | mA    |
|            |                                                             | LCMXO2-640HC   | 1.84              | mA    |
|            |                                                             | LCMXO2-640UHC  | 3.48              | mA    |
|            |                                                             | LCMXO2-1200HC  | 3.49              | mA    |
|            |                                                             | LCMXO2-1200UHC | 4.80              | mA    |
|            |                                                             | LCMXO2-2000HC  | 4.80              | mA    |
|            |                                                             | LCMXO2-2000UHC | 8.44              | mA    |
|            |                                                             | LCMXO2-4000HC  | 8.45              | mA    |
|            |                                                             | LCMXO2-7000HC  | 12.87             | mA    |
|            |                                                             | LCMXO2-2000HE  | 1.39              | mA    |
|            |                                                             | LCMXO2-4000HE  | 2.55              | mA    |
|            |                                                             | LCMXO2-7000HE  | 4.06              | mA    |
| $I_{CCIO}$ | Bank Power Supply <sup>5</sup><br>$V_{CCIO} = 2.5\text{ V}$ | All devices    | 0                 | mA    |

- For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).
- Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at  $V_{CCIO}$  or GND, on-chip oscillator is off, on-chip PLL is off.
- Frequency = 0 MHz.
- $T_J = 25\text{ }^{\circ}\text{C}$ , power supplies at nominal voltage.
- Does not include pull-up/pull-down.
- To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

### Programming and Erase Flash Supply Current – HC/HE Devices<sup>1, 2, 3, 4</sup>

| Symbol     | Parameter                      | Device         | Typ. <sup>5</sup> | Units |
|------------|--------------------------------|----------------|-------------------|-------|
| $I_{CC}$   | Core Power Supply              | LCMXO2-256HC   | 14.6              | mA    |
|            |                                | LCMXO2-640HC   | 16.1              | mA    |
|            |                                | LCMXO2-640UHC  | 18.8              | mA    |
|            |                                | LCMXO2-1200HC  | 18.8              | mA    |
|            |                                | LCMXO2-1200UHC | 22.1              | mA    |
|            |                                | LCMXO2-2000HC  | 22.1              | mA    |
|            |                                | LCMXO2-2000UHC | 26.8              | mA    |
|            |                                | LCMXO2-4000HC  | 26.8              | mA    |
|            |                                | LCMXO2-7000HC  | 33.2              | mA    |
|            |                                | LCMXO2-2000HE  | 18.3              | mA    |
|            |                                | LCMXO2-2000UHE | 20.4              | mA    |
|            |                                | LCMXO2-4000HE  | 20.4              | mA    |
|            |                                | LCMXO2-7000HE  | 23.9              | mA    |
| $I_{CCIO}$ | Bank Power Supply <sup>6</sup> | All devices    | 0                 | mA    |

- For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).
- Assumes all inputs are held at  $V_{CCIO}$  or GND and all outputs are tri-stated.
- Typical user pattern.
- JTAG programming is at 25 MHz.
- $T_J = 25\text{ }^{\circ}\text{C}$ , power supplies at nominal voltage.
- Per bank.  $V_{CCIO} = 2.5\text{ V}$ . Does not include pull-up/pull-down.

**Programming and Erase Flash Supply Current – ZE Devices<sup>1, 2, 3, 4</sup>**

| Symbol     | Parameter                      | Device        | Typ. <sup>5</sup> | Units |
|------------|--------------------------------|---------------|-------------------|-------|
| $I_{CC}$   | Core Power Supply              | LCMXO2-256ZE  | 13                | mA    |
|            |                                | LCMXO2-640ZE  | 14                | mA    |
|            |                                | LCMXO2-1200ZE | 15                | mA    |
|            |                                | LCMXO2-2000ZE | 17                | mA    |
|            |                                | LCMXO2-4000ZE | 18                | mA    |
|            |                                | LCMXO2-7000ZE | 20                | mA    |
| $I_{CCIO}$ | Bank Power Supply <sup>6</sup> | All devices   | 0                 | mA    |

1. For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).

2. Assumes all inputs are held at  $V_{CCIO}$  or GND and all outputs are tri-stated.

3. Typical user pattern.

4. JTAG programming is at 25 MHz.

5.  $T_J = 25^\circ\text{C}$ , power supplies at nominal voltage.

6. Per bank.  $V_{CCIO} = 2.5\text{ V}$ . Does not include pull-up/pull-down.

| Input/Output Standard | $V_{IL}$              |                 | $V_{IH}$        |          | $V_{OL}$ Max. (V) | $V_{OH}$ Min. (V) | $I_{OL}$ Max. <sup>4</sup> (mA) | $I_{OH}$ Max. <sup>4</sup> (mA) |
|-----------------------|-----------------------|-----------------|-----------------|----------|-------------------|-------------------|---------------------------------|---------------------------------|
|                       | Min. (V) <sup>3</sup> | Max. (V)        | Min. (V)        | Max. (V) |                   |                   |                                 |                                 |
| LVC MOS10R25          | -0.3                  | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 3.6      | 0.40              | NA Open Drain     | 16, 12, 8, 4                    | NA Open Drain                   |

1. MachXO2 devices allow LVC MOS inputs to be placed in I/O banks where  $V_{CCIO}$  is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO2 devices do not meet the relevant JEDEC specification are documented in the table below.
2. MachXO2 devices allow for LVC MOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1202, [MachXO2 sysIO Usage Guide](#).
3. The dual function I<sup>2</sup>C pins SCL and SDA are limited to a  $V_{IL}$  min of -0.25 V or to -0.3 V with a duration of <10 ns.
4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive  $V_{CCIO}$  or GND pad connections, or between the last  $V_{CCIO}$  or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of  $n * 8$  mA. "n" is the number of I/O pads between the two consecutive bank  $V_{CCIO}$  or GND connections or between the last  $V_{CCIO}$  and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

| Input Standard | $V_{CCIO}$ (V) | $V_{IL}$ Max. (V) |
|----------------|----------------|-------------------|
| LVC MOS 33     | 1.5            | 0.685             |
| LVC MOS 25     | 1.5            | 0.687             |
| LVC MOS 18     | 1.5            | 0.655             |

## sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of MachXO2-640U, MachXO2-1200/U and higher density devices in the MachXO2 PLD family.

### LVDS

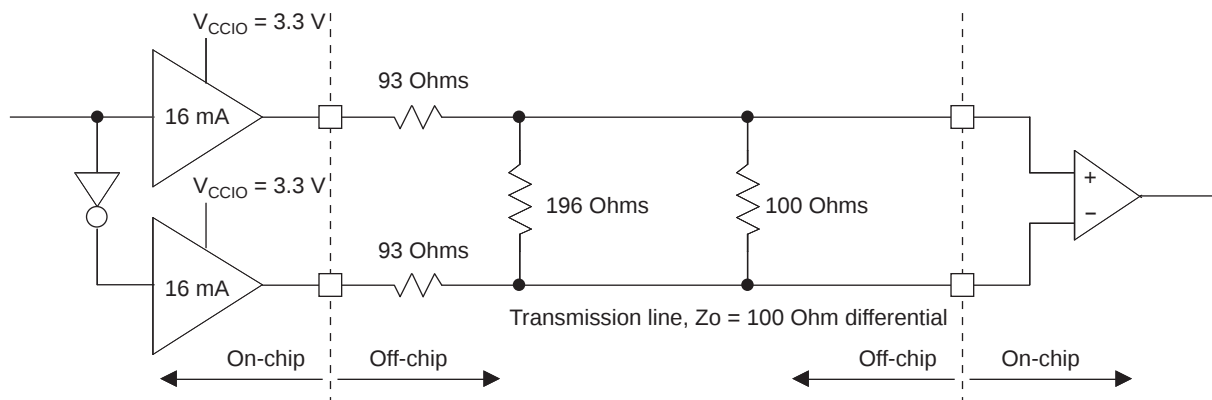
#### Over Recommended Operating Conditions

| Parameter Symbol    | Parameter Description                        | Test Conditions                         | Min.  | Typ.  | Max.  | Units |
|---------------------|----------------------------------------------|-----------------------------------------|-------|-------|-------|-------|
| $V_{INP}$ $V_{INM}$ | Input Voltage                                | $V_{CCIO} = 3.3$ V                      | 0     | —     | 2.605 | V     |
|                     |                                              | $V_{CCIO} = 2.5$ V                      | 0     | —     | 2.05  | V     |
| $V_{THD}$           | Differential Input Threshold                 |                                         | ±100  | —     |       | mV    |
| $V_{CM}$            | Input Common Mode Voltage                    | $V_{CCIO} = 3.3$ V                      | 0.05  | —     | 2.6   | V     |
|                     |                                              | $V_{CCIO} = 2.5$ V                      | 0.05  | —     | 2.0   | V     |
| $I_{IN}$            | Input current                                | Power on                                | —     | —     | ±10   | μA    |
| $V_{OH}$            | Output high voltage for $V_{OP}$ or $V_{OM}$ | $R_T = 100$ Ohm                         | —     | 1.375 | —     | V     |
| $V_{OL}$            | Output low voltage for $V_{OP}$ or $V_{OM}$  | $R_T = 100$ Ohm                         | 0.90  | 1.025 | —     | V     |
| $V_{OD}$            | Output voltage differential                  | $(V_{OP} - V_{OM})$ , $R_T = 100$ Ohm   | 250   | 350   | 450   | mV    |
| $\Delta V_{OD}$     | Change in $V_{OD}$ between high and low      |                                         | —     | —     | 50    | mV    |
| $V_{OS}$            | Output voltage offset                        | $(V_{OP} + V_{OM})/2$ , $R_T = 100$ Ohm | 1.125 | 1.20  | 1.395 | V     |
| $\Delta V_{OS}$     | Change in $V_{OS}$ between H and L           |                                         | —     | —     | 50    | mV    |
| $I_{OSD}$           | Output short circuit current                 | $V_{OD} = 0$ V driver outputs shorted   | —     | —     | 24    | mA    |

### LVPECL

The MachXO2 family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

**Figure 3-3. Differential LVPECL**



**Table 3-3. LVPECL DC Conditions<sup>1</sup>**

#### Over Recommended Operating Conditions

| Symbol     | Description                 | Nominal | Units |
|------------|-----------------------------|---------|-------|
| $Z_{OUT}$  | Output impedance            | 20      | Ohms  |
| $R_S$      | Driver series resistor      | 93      | Ohms  |
| $R_P$      | Driver parallel resistor    | 196     | Ohms  |
| $R_T$      | Receiver termination        | 100     | Ohms  |
| $V_{OH}$   | Output high voltage         | 2.05    | V     |
| $V_{OL}$   | Output low voltage          | 1.25    | V     |
| $V_{OD}$   | Output differential voltage | 0.80    | V     |
| $V_{CM}$   | Output common mode voltage  | 1.65    | V     |
| $Z_{BACK}$ | Back impedance              | 100.5   | Ohms  |
| $I_{DC}$   | DC output current           | 12.11   | mA    |

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

## Maximum sysIO Buffer Performance

| I/O Standard | Max. Speed | Units |
|--------------|------------|-------|
| LVDS25       | 400        | MHz   |
| LVDS25E      | 150        | MHz   |
| RSDS25       | 150        | MHz   |
| RSDS25E      | 150        | MHz   |
| BLVDS25      | 150        | MHz   |
| BLVDS25E     | 150        | MHz   |
| MLVDS25      | 150        | MHz   |
| MLVDS25E     | 150        | MHz   |
| LVPECL33     | 150        | MHz   |
| LVPECL33E    | 150        | MHz   |
| SSTL25_I     | 150        | MHz   |
| SSTL25_II    | 150        | MHz   |
| SSTL25D_I    | 150        | MHz   |
| SSTL25D_II   | 150        | MHz   |
| SSTL18_I     | 150        | MHz   |
| SSTL18_II    | 150        | MHz   |
| SSTL18D_I    | 150        | MHz   |
| SSTL18D_II   | 150        | MHz   |
| HSTL18_I     | 150        | MHz   |
| HSTL18_II    | 150        | MHz   |
| HSTL18D_I    | 150        | MHz   |
| HSTL18D_II   | 150        | MHz   |
| PCI33        | 134        | MHz   |
| LVTTTL33     | 150        | MHz   |
| LVTTTL33D    | 150        | MHz   |
| LVC MOS33    | 150        | MHz   |
| LVC MOS33D   | 150        | MHz   |
| LVC MOS25    | 150        | MHz   |
| LVC MOS25D   | 150        | MHz   |
| LVC MOS25R33 | 150        | MHz   |
| LVC MOS18    | 150        | MHz   |
| LVC MOS18D   | 150        | MHz   |
| LVC MOS18R33 | 150        | MHz   |
| LVC MOS18R25 | 150        | MHz   |
| LVC MOS15    | 150        | MHz   |
| LVC MOS15D   | 150        | MHz   |
| LVC MOS15R33 | 150        | MHz   |
| LVC MOS15R25 | 150        | MHz   |
| LVC MOS12    | 91         | MHz   |
| LVC MOS12D   | 91         | MHz   |

| Parameter                                                                                                                         | Description                                                    | Device                                                                          | -6    |       | -5    |       | -4    |       | Units |
|-----------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------|---------------------------------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|
|                                                                                                                                   |                                                                |                                                                                 | Min.  | Max.  | Min.  | Max.  | Min.  | Max.  |       |
| t <sub>HPLL</sub>                                                                                                                 | Clock to Data Hold – PIO Input Register                        | MachXO2-1200HC-HE                                                               | 0.41  | —     | 0.48  | —     | 0.55  | —     | ns    |
|                                                                                                                                   |                                                                | MachXO2-2000HC-HE                                                               | 0.42  | —     | 0.49  | —     | 0.56  | —     | ns    |
|                                                                                                                                   |                                                                | MachXO2-4000HC-HE                                                               | 0.43  | —     | 0.50  | —     | 0.58  | —     | ns    |
|                                                                                                                                   |                                                                | MachXO2-7000HC-HE                                                               | 0.46  | —     | 0.54  | —     | 0.62  | —     | ns    |
| t <sub>SU_DELPLL</sub>                                                                                                            | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-1200HC-HE                                                               | 2.88  | —     | 3.19  | —     | 3.72  | —     | ns    |
|                                                                                                                                   |                                                                | MachXO2-2000HC-HE                                                               | 2.87  | —     | 3.18  | —     | 3.70  | —     | ns    |
|                                                                                                                                   |                                                                | MachXO2-4000HC-HE                                                               | 2.96  | —     | 3.28  | —     | 3.81  | —     | ns    |
|                                                                                                                                   |                                                                | MachXO2-7000HC-HE                                                               | 3.05  | —     | 3.35  | —     | 3.87  | —     | ns    |
| t <sub>H_DELPLL</sub>                                                                                                             | Clock to Data Hold – PIO Input Register with Input Data Delay  | MachXO2-1200HC-HE                                                               | –0.83 | —     | –0.83 | —     | –0.83 | —     | ns    |
|                                                                                                                                   |                                                                | MachXO2-2000HC-HE                                                               | –0.83 | —     | –0.83 | —     | –0.83 | —     | ns    |
|                                                                                                                                   |                                                                | MachXO2-4000HC-HE                                                               | –0.87 | —     | –0.87 | —     | –0.87 | —     | ns    |
|                                                                                                                                   |                                                                | MachXO2-7000HC-HE                                                               | –0.91 | —     | –0.91 | —     | –0.91 | —     | ns    |
| Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Aligned <sup>9, 12</sup>   |                                                                |                                                                                 |       |       |       |       |       |       |       |
| t <sub>DVA</sub>                                                                                                                  | Input Data Valid After CLK                                     | All MachXO2 devices, all sides                                                  | —     | 0.317 | —     | 0.344 | —     | 0.368 | UI    |
| t <sub>DVE</sub>                                                                                                                  | Input Data Hold After CLK                                      |                                                                                 | 0.742 | —     | 0.702 | —     | 0.668 | —     | UI    |
| f <sub>DATA</sub>                                                                                                                 | DDRX1 Input Data Speed                                         |                                                                                 | —     | 300   | —     | 250   | —     | 208   | Mbps  |
| f <sub>DDRX1</sub>                                                                                                                | DDRX1 SCLK Frequency                                           |                                                                                 | —     | 150   | —     | 125   | —     | 104   | MHz   |
| Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Centered <sup>9, 12</sup> |                                                                |                                                                                 |       |       |       |       |       |       |       |
| t <sub>SU</sub>                                                                                                                   | Input Data Setup Before CLK                                    | All MachXO2 devices, all sides                                                  | 0.566 | —     | 0.560 | —     | 0.538 | —     | ns    |
| t <sub>HO</sub>                                                                                                                   | Input Data Hold After CLK                                      |                                                                                 | 0.778 | —     | 0.879 | —     | 1.090 | —     | ns    |
| f <sub>DATA</sub>                                                                                                                 | DDRX1 Input Data Speed                                         |                                                                                 | —     | 300   | —     | 250   | —     | 208   | Mbps  |
| f <sub>DDRX1</sub>                                                                                                                | DDRX1 SCLK Frequency                                           |                                                                                 | —     | 150   | —     | 125   | —     | 104   | MHz   |
| Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Aligned <sup>9, 12</sup>   |                                                                |                                                                                 |       |       |       |       |       |       |       |
| t <sub>DVA</sub>                                                                                                                  | Input Data Valid After CLK                                     | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only <sup>11</sup> | —     | 0.316 | —     | 0.342 | —     | 0.364 | UI    |
| t <sub>DVE</sub>                                                                                                                  | Input Data Hold After CLK                                      |                                                                                 | 0.710 | —     | 0.675 | —     | 0.679 | —     | UI    |
| f <sub>DATA</sub>                                                                                                                 | DDRX2 Serial Input Data Speed                                  |                                                                                 | —     | 664   | —     | 554   | —     | 462   | Mbps  |
| f <sub>DDRX2</sub>                                                                                                                | DDRX2 ECLK Frequency                                           |                                                                                 | —     | 332   | —     | 277   | —     | 231   | MHz   |
| f <sub>SCLK</sub>                                                                                                                 | SCLK Frequency                                                 |                                                                                 | —     | 166   | —     | 139   | —     | 116   | MHz   |
| Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Centered <sup>9, 12</sup> |                                                                |                                                                                 |       |       |       |       |       |       |       |
| t <sub>SU</sub>                                                                                                                   | Input Data Setup Before CLK                                    | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only <sup>11</sup> | 0.233 | —     | 0.219 | —     | 0.198 | —     | ns    |
| t <sub>HO</sub>                                                                                                                   | Input Data Hold After CLK                                      |                                                                                 | 0.287 | —     | 0.287 | —     | 0.344 | —     | ns    |
| f <sub>DATA</sub>                                                                                                                 | DDRX2 Serial Input Data Speed                                  |                                                                                 | —     | 664   | —     | 554   | —     | 462   | Mbps  |
| f <sub>DDRX2</sub>                                                                                                                | DDRX2 ECLK Frequency                                           |                                                                                 | —     | 332   | —     | 277   | —     | 231   | MHz   |
| f <sub>SCLK</sub>                                                                                                                 | SCLK Frequency                                                 |                                                                                 | —     | 166   | —     | 139   | —     | 116   | MHz   |

| Parameter                                                                                                                        | Description                                               | Device                                                                                    | -6    |       | -5    |       | -4    |       | Units |
|----------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------|-------------------------------------------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|
|                                                                                                                                  |                                                           |                                                                                           | Min.  | Max.  | Min.  | Max.  | Min.  | Max.  |       |
| Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR4_RX.ECLK.Aligned <sup>9, 12</sup>   |                                                           |                                                                                           |       |       |       |       |       |       |       |
| t <sub>DVA</sub>                                                                                                                 | Input Data Valid After ECLK                               | MachXO2-640U,<br>MachXO2-1200/U and<br>larger devices,<br>bottom side only. <sup>11</sup> | —     | 0.290 | —     | 0.320 | —     | 0.345 | UI    |
| t <sub>DVE</sub>                                                                                                                 | Input Data Hold After ECLK                                |                                                                                           | 0.739 | —     | 0.699 | —     | 0.703 | —     | UI    |
| f <sub>DATA</sub>                                                                                                                | DDR4 Serial Input Data Speed                              |                                                                                           | —     | 756   | —     | 630   | —     | 524   | Mbps  |
| f <sub>DDR4</sub>                                                                                                                | DDR4 ECLK Frequency                                       |                                                                                           | —     | 378   | —     | 315   | —     | 262   | MHz   |
| f <sub>SCLK</sub>                                                                                                                | SCLK Frequency                                            |                                                                                           | —     | 95    | —     | 79    | —     | 66    | MHz   |
| Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR4_RX.ECLK.Centered <sup>9, 12</sup> |                                                           |                                                                                           |       |       |       |       |       |       |       |
| t <sub>SU</sub>                                                                                                                  | Input Data Setup Before ECLK                              | MachXO2-640U,<br>MachXO2-1200/U and<br>larger devices,<br>bottom side only. <sup>11</sup> | 0.233 | —     | 0.219 | —     | 0.198 | —     | ns    |
| t <sub>HO</sub>                                                                                                                  | Input Data Hold After ECLK                                |                                                                                           | 0.287 | —     | 0.287 | —     | 0.344 | —     | ns    |
| f <sub>DATA</sub>                                                                                                                | DDR4 Serial Input Data Speed                              |                                                                                           | —     | 756   | —     | 630   | —     | 524   | Mbps  |
| f <sub>DDR4</sub>                                                                                                                | DDR4 ECLK Frequency                                       |                                                                                           | —     | 378   | —     | 315   | —     | 262   | MHz   |
| f <sub>SCLK</sub>                                                                                                                | SCLK Frequency                                            |                                                                                           | —     | 95    | —     | 79    | —     | 66    | MHz   |
| 7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1) <sup>9, 12</sup>                                                                            |                                                           |                                                                                           |       |       |       |       |       |       |       |
| t <sub>DVA</sub>                                                                                                                 | Input Data Valid After ECLK                               | MachXO2-640U,<br>MachXO2-1200/U and<br>larger devices, bottom<br>side only. <sup>11</sup> | —     | 0.290 | —     | 0.320 | —     | 0.345 | UI    |
| t <sub>DVE</sub>                                                                                                                 | Input Data Hold After ECLK                                |                                                                                           | 0.739 | —     | 0.699 | —     | 0.703 | —     | UI    |
| f <sub>DATA</sub>                                                                                                                | DDR71 Serial Input Data Speed                             |                                                                                           | —     | 756   | —     | 630   | —     | 524   | Mbps  |
| f <sub>DDR71</sub>                                                                                                               | DDR71 ECLK Frequency                                      |                                                                                           | —     | 378   | —     | 315   | —     | 262   | MHz   |
| f <sub>CLKIN</sub>                                                                                                               | 7:1 Input Clock Frequency (SCLK) (minimum limited by PLL) |                                                                                           | —     | 108   | —     | 90    | —     | 75    | MHz   |
| Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Aligned <sup>9, 12</sup>   |                                                           |                                                                                           |       |       |       |       |       |       |       |
| t <sub>DIA</sub>                                                                                                                 | Output Data Invalid After CLK Output                      | All MachXO2 devices,<br>all sides.                                                        | —     | 0.520 | —     | 0.550 | —     | 0.580 | ns    |
| t <sub>DIB</sub>                                                                                                                 | Output Data Invalid Before CLK Output                     |                                                                                           | —     | 0.520 | —     | 0.550 | —     | 0.580 | ns    |
| f <sub>DATA</sub>                                                                                                                | DDR1 Output Data Speed                                    |                                                                                           | —     | 300   | —     | 250   | —     | 208   | Mbps  |
| f <sub>DDR1</sub>                                                                                                                | DDR1 SCLK frequency                                       |                                                                                           | —     | 150   | —     | 125   | —     | 104   | MHz   |
| Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Centered <sup>9, 12</sup> |                                                           |                                                                                           |       |       |       |       |       |       |       |
| t <sub>DVB</sub>                                                                                                                 | Output Data Valid Before CLK Output                       | All MachXO2 devices,<br>all sides.                                                        | 1.210 | —     | 1.510 | —     | 1.870 | —     | ns    |
| t <sub>DVA</sub>                                                                                                                 | Output Data Valid After CLK Output                        |                                                                                           | 1.210 | —     | 1.510 | —     | 1.870 | —     | ns    |
| f <sub>DATA</sub>                                                                                                                | DDR1 Output Data Speed                                    |                                                                                           | —     | 300   | —     | 250   | —     | 208   | Mbps  |
| f <sub>DDR1</sub>                                                                                                                | DDR1 SCLK Frequency (minimum limited by PLL)              |                                                                                           | —     | 150   | —     | 125   | —     | 104   | MHz   |
| Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_TX.ECLK.Aligned <sup>9, 12</sup> |                                                           |                                                                                           |       |       |       |       |       |       |       |
| t <sub>DIA</sub>                                                                                                                 | Output Data Invalid After CLK Output                      | MachXO2-640U,<br>MachXO2-1200/U and<br>larger devices, top side<br>only.                  | —     | 0.200 | —     | 0.215 | —     | 0.230 | ns    |
| t <sub>DIB</sub>                                                                                                                 | Output Data Invalid Before CLK Output                     |                                                                                           | —     | 0.200 | —     | 0.215 | —     | 0.230 | ns    |
| f <sub>DATA</sub>                                                                                                                | DDR2 Serial Output Data Speed                             |                                                                                           | —     | 664   | —     | 554   | —     | 462   | Mbps  |
| f <sub>DDR2</sub>                                                                                                                | DDR2 ECLK frequency                                       |                                                                                           | —     | 332   | —     | 277   | —     | 231   | MHz   |
| f <sub>SCLK</sub>                                                                                                                | SCLK Frequency                                            |                                                                                           | —     | 166   | —     | 139   | —     | 116   | MHz   |

| Parameter                                                 | Description                                                    | Device              | -3    |       | -2    |       | -1    |       | Units |
|-----------------------------------------------------------|----------------------------------------------------------------|---------------------|-------|-------|-------|-------|-------|-------|-------|
|                                                           |                                                                |                     | Min.  | Max.  | Min.  | Max.  | Min.  | Max.  |       |
| t <sub>SU_DEL</sub>                                       | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-256ZE       | 2.62  | —     | 2.91  | —     | 3.14  | —     | ns    |
|                                                           |                                                                | MachXO2-640ZE       | 2.56  | —     | 2.85  | —     | 3.08  | —     | ns    |
|                                                           |                                                                | MachXO2-1200ZE      | 2.30  | —     | 2.57  | —     | 2.79  | —     | ns    |
|                                                           |                                                                | MachXO2-2000ZE      | 2.25  | —     | 2.50  | —     | 2.70  | —     | ns    |
|                                                           |                                                                | MachXO2-4000ZE      | 2.39  | —     | 2.60  | —     | 2.76  | —     | ns    |
|                                                           |                                                                | MachXO2-7000ZE      | 2.17  | —     | 2.33  | —     | 2.43  | —     | ns    |
| t <sub>H_DEL</sub>                                        | Clock to Data Hold – PIO Input Register with Input Data Delay  | MachXO2-256ZE       | –0.44 | —     | –0.44 | —     | –0.44 | —     | ns    |
|                                                           |                                                                | MachXO2-640ZE       | –0.43 | —     | –0.43 | —     | –0.43 | —     | ns    |
|                                                           |                                                                | MachXO2-1200ZE      | –0.28 | —     | –0.28 | —     | –0.28 | —     | ns    |
|                                                           |                                                                | MachXO2-2000ZE      | –0.31 | —     | –0.31 | —     | –0.31 | —     | ns    |
|                                                           |                                                                | MachXO2-4000ZE      | –0.34 | —     | –0.34 | —     | –0.34 | —     | ns    |
|                                                           |                                                                | MachXO2-7000ZE      | –0.21 | —     | –0.21 | —     | –0.21 | —     | ns    |
| f <sub>MAX_IO</sub>                                       | Clock Frequency of I/O and PFU Register                        | All MachXO2 devices | —     | 150   | —     | 125   | —     | 104   | MHz   |
| General I/O Pin Parameters (Using Edge Clock without PLL) |                                                                |                     |       |       |       |       |       |       |       |
| t <sub>COE</sub>                                          | Clock to Output – PIO Output Register                          | MachXO2-1200ZE      | —     | 11.10 | —     | 11.51 | —     | 11.91 | ns    |
|                                                           |                                                                | MachXO2-2000ZE      | —     | 11.10 | —     | 11.51 | —     | 11.91 | ns    |
|                                                           |                                                                | MachXO2-4000ZE      | —     | 10.89 | —     | 11.28 | —     | 11.67 | ns    |
|                                                           |                                                                | MachXO2-7000ZE      | —     | 11.10 | —     | 11.51 | —     | 11.91 | ns    |
| t <sub>SUE</sub>                                          | Clock to Data Setup – PIO Input Register                       | MachXO2-1200ZE      | –0.23 | —     | –0.23 | —     | –0.23 | —     | ns    |
|                                                           |                                                                | MachXO2-2000ZE      | –0.23 | —     | –0.23 | —     | –0.23 | —     | ns    |
|                                                           |                                                                | MachXO2-4000ZE      | –0.15 | —     | –0.15 | —     | –0.15 | —     | ns    |
|                                                           |                                                                | MachXO2-7000ZE      | –0.23 | —     | –0.23 | —     | –0.23 | —     | ns    |
| t <sub>HE</sub>                                           | Clock to Data Hold – PIO Input Register                        | MachXO2-1200ZE      | 3.81  | —     | 4.11  | —     | 4.52  | —     | ns    |
|                                                           |                                                                | MachXO2-2000ZE      | 3.81  | —     | 4.11  | —     | 4.52  | —     | ns    |
|                                                           |                                                                | MachXO2-4000ZE      | 3.60  | —     | 3.89  | —     | 4.28  | —     | ns    |
|                                                           |                                                                | MachXO2-7000ZE      | 3.81  | —     | 4.11  | —     | 4.52  | —     | ns    |
| t <sub>SU_DELE</sub>                                      | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-1200ZE      | 2.78  | —     | 3.11  | —     | 3.40  | —     | ns    |
|                                                           |                                                                | MachXO2-2000ZE      | 2.78  | —     | 3.11  | —     | 3.40  | —     | ns    |
|                                                           |                                                                | MachXO2-4000ZE      | 3.11  | —     | 3.48  | —     | 3.79  | —     | ns    |
|                                                           |                                                                | MachXO2-7000ZE      | 2.94  | —     | 3.30  | —     | 3.60  | —     | ns    |
| t <sub>H_DELE</sub>                                       | Clock to Data Hold – PIO Input Register with Input Data Delay  | MachXO2-1200ZE      | –0.29 | —     | –0.29 | —     | –0.29 | —     | ns    |
|                                                           |                                                                | MachXO2-2000ZE      | –0.29 | —     | –0.29 | —     | –0.29 | —     | ns    |
|                                                           |                                                                | MachXO2-4000ZE      | –0.46 | —     | –0.46 | —     | –0.46 | —     | ns    |
|                                                           |                                                                | MachXO2-7000ZE      | –0.37 | —     | –0.37 | —     | –0.37 | —     | ns    |
| General I/O Pin Parameters (Using Primary Clock with PLL) |                                                                |                     |       |       |       |       |       |       |       |
| t <sub>COPLL</sub>                                        | Clock to Output – PIO Output Register                          | MachXO2-1200ZE      | —     | 7.95  | —     | 8.07  | —     | 8.19  | ns    |
|                                                           |                                                                | MachXO2-2000ZE      | —     | 7.97  | —     | 8.10  | —     | 8.22  | ns    |
|                                                           |                                                                | MachXO2-4000ZE      | —     | 7.98  | —     | 8.10  | —     | 8.23  | ns    |
|                                                           |                                                                | MachXO2-7000ZE      | —     | 8.02  | —     | 8.14  | —     | 8.26  | ns    |
| t <sub>SUPLL</sub>                                        | Clock to Data Setup – PIO Input Register                       | MachXO2-1200ZE      | 0.85  | —     | 0.85  | —     | 0.89  | —     | ns    |
|                                                           |                                                                | MachXO2-2000ZE      | 0.84  | —     | 0.84  | —     | 0.86  | —     | ns    |
|                                                           |                                                                | MachXO2-4000ZE      | 0.84  | —     | 0.84  | —     | 0.85  | —     | ns    |
|                                                           |                                                                | MachXO2-7000ZE      | 0.83  | —     | 0.83  | —     | 0.81  | —     | ns    |

## Flash Download Time<sup>1, 2</sup>

| Symbol               | Parameter                | Device       | Typ. | Units |
|----------------------|--------------------------|--------------|------|-------|
| $t_{\text{REFRESH}}$ | POR to Device I/O Active | LCMXO2-256   | 0.6  | ms    |
|                      |                          | LCMXO2-640   | 1.0  | ms    |
|                      |                          | LCMXO2-640U  | 1.9  | ms    |
|                      |                          | LCMXO2-1200  | 1.9  | ms    |
|                      |                          | LCMXO2-1200U | 1.4  | ms    |
|                      |                          | LCMXO2-2000  | 1.4  | ms    |
|                      |                          | LCMXO2-2000U | 2.4  | ms    |
|                      |                          | LCMXO2-4000  | 2.4  | ms    |
|                      |                          | LCMXO2-7000  | 3.8  | ms    |

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.

2. The Flash download time is measured starting from the maximum voltage of POR trip point.

## JTAG Port Timing Specifications

| Symbol               | Parameter                                                          | Min. | Max. | Units |
|----------------------|--------------------------------------------------------------------|------|------|-------|
| $f_{\text{MAX}}$     | TCK clock frequency                                                | —    | 25   | MHz   |
| $t_{\text{BTCPH}}$   | TCK [BSCAN] clock pulse width high                                 | 20   | —    | ns    |
| $t_{\text{BTCPL}}$   | TCK [BSCAN] clock pulse width low                                  | 20   | —    | ns    |
| $t_{\text{BTS}}$     | TCK [BSCAN] setup time                                             | 10   | —    | ns    |
| $t_{\text{BTH}}$     | TCK [BSCAN] hold time                                              | 8    | —    | ns    |
| $t_{\text{BTCO}}$    | TAP controller falling edge of clock to valid output               | —    | 10   | ns    |
| $t_{\text{BTCODIS}}$ | TAP controller falling edge of clock to valid disable              | —    | 10   | ns    |
| $t_{\text{BTCOEN}}$  | TAP controller falling edge of clock to valid enable               | —    | 10   | ns    |
| $t_{\text{BTCRS}}$   | BSCAN test capture register setup time                             | 8    | —    | ns    |
| $t_{\text{BTCRH}}$   | BSCAN test capture register hold time                              | 20   | —    | ns    |
| $t_{\text{BUTCO}}$   | BSCAN test update register, falling edge of clock to valid output  | —    | 25   | ns    |
| $t_{\text{BTUODIS}}$ | BSCAN test update register, falling edge of clock to valid disable | —    | 25   | ns    |
| $t_{\text{BTUPOEN}}$ | BSCAN test update register, falling edge of clock to valid enable  | —    | 25   | ns    |

|                                                        | MachXO2-1200 |           |          |          |                     | MachXO2-1200U |
|--------------------------------------------------------|--------------|-----------|----------|----------|---------------------|---------------|
|                                                        | 100 TQFP     | 132 csBGA | 144 TQFP | 25 WLCSP | 32 QFN <sup>1</sup> | 256 ftBGA     |
| <b>General Purpose I/O per Bank</b>                    |              |           |          |          |                     |               |
| Bank 0                                                 | 18           | 25        | 27       | 11       | 9                   | 50            |
| Bank 1                                                 | 21           | 26        | 26       | 0        | 2                   | 52            |
| Bank 2                                                 | 20           | 28        | 28       | 7        | 9                   | 52            |
| Bank 3                                                 | 20           | 25        | 26       | 0        | 2                   | 16            |
| Bank 4                                                 | 0            | 0         | 0        | 0        | 0                   | 16            |
| Bank 5                                                 | 0            | 0         | 0        | 0        | 0                   | 20            |
| Total General Purpose Single Ended I/O                 | 79           | 104       | 107      | 18       | 22                  | 206           |
| <b>Differential I/O per Bank</b>                       |              |           |          |          |                     |               |
| Bank 0                                                 | 9            | 13        | 14       | 5        | 4                   | 25            |
| Bank 1                                                 | 10           | 13        | 13       | 0        | 1                   | 26            |
| Bank 2                                                 | 10           | 14        | 14       | 2        | 4                   | 26            |
| Bank 3                                                 | 10           | 12        | 13       | 0        | 1                   | 8             |
| Bank 4                                                 | 0            | 0         | 0        | 0        | 0                   | 8             |
| Bank 5                                                 | 0            | 0         | 0        | 0        | 0                   | 10            |
| Total General Purpose Differential I/O                 | 39           | 52        | 54       | 7        | 10                  | 103           |
| <b>Dual Function I/O</b>                               |              |           |          |          |                     |               |
|                                                        | 31           | 33        | 33       | 18       | 22                  | 33            |
| <b>High-speed Differential I/O</b>                     |              |           |          |          |                     |               |
| Bank 0                                                 | 4            | 7         | 7        | 0        | 0                   | 14            |
| <b>Gearboxes</b>                                       |              |           |          |          |                     |               |
| Number of 7:1 or 8:1 Output Gearbox Available (Bank 0) | 4            | 7         | 7        | 0        | 0                   | 14            |
| Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)  | 5            | 7         | 7        | 0        | 2                   | 14            |
| <b>DQS Groups</b>                                      |              |           |          |          |                     |               |
| Bank 1                                                 | 1            | 2         | 2        | 0        | 0                   | 2             |
| <b>VCCIO Pins</b>                                      |              |           |          |          |                     |               |
| Bank 0                                                 | 2            | 3         | 3        | 1        | 2                   | 4             |
| Bank 1                                                 | 2            | 3         | 3        | 0        | 1                   | 4             |
| Bank 2                                                 | 2            | 3         | 3        | 1        | 2                   | 4             |
| Bank 3                                                 | 3            | 3         | 3        | 0        | 1                   | 1             |
| Bank 4                                                 | 0            | 0         | 0        | 0        | 0                   | 2             |
| Bank 5                                                 | 0            | 0         | 0        | 0        | 0                   | 1             |
| VCC                                                    | 2            | 4         | 4        | 2        | 2                   | 8             |
| GND                                                    | 8            | 10        | 12       | 2        | 2                   | 24            |
| NC                                                     | 1            | 1         | 8        | 0        | 0                   | 1             |
| Reserved for Configuration                             | 1            | 1         | 1        | 1        | 1                   | 1             |
| Total Count of Bonded Pins                             | 100          | 132       | 144      | 25       | 32                  | 256           |

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.

|                                                        | MachXO2-7000 |           |           |           |           |           |
|--------------------------------------------------------|--------------|-----------|-----------|-----------|-----------|-----------|
|                                                        | 144 TQFP     | 256 caBGA | 256 ftBGA | 332 caBGA | 400 caBGA | 484 fpBGA |
| <b>General Purpose I/O per Bank</b>                    |              |           |           |           |           |           |
| Bank 0                                                 | 27           | 50        | 50        | 68        | 83        | 82        |
| Bank 1                                                 | 29           | 52        | 52        | 70        | 84        | 84        |
| Bank 2                                                 | 29           | 52        | 52        | 70        | 84        | 84        |
| Bank 3                                                 | 9            | 16        | 16        | 24        | 28        | 28        |
| Bank 4                                                 | 10           | 16        | 16        | 16        | 24        | 24        |
| Bank 5                                                 | 10           | 20        | 20        | 30        | 32        | 32        |
| Total General Purpose Single Ended I/O                 | 114          | 206       | 206       | 278       | 335       | 334       |
| <b>Differential I/O per Bank</b>                       |              |           |           |           |           |           |
| Bank 0                                                 | 14           | 25        | 25        | 34        | 42        | 41        |
| Bank 1                                                 | 14           | 26        | 26        | 35        | 42        | 42        |
| Bank 2                                                 | 14           | 26        | 26        | 35        | 42        | 42        |
| Bank 3                                                 | 4            | 8         | 8         | 12        | 14        | 14        |
| Bank 4                                                 | 5            | 8         | 8         | 8         | 12        | 12        |
| Bank 5                                                 | 5            | 10        | 10        | 15        | 16        | 16        |
| Total General Purpose Differential I/O                 | 56           | 103       | 103       | 139       | 168       | 167       |
| <b>Dual Function I/O</b>                               |              |           |           |           |           |           |
|                                                        | 37           | 37        | 37        | 37        | 37        | 37        |
| <b>High-speed Differential I/O</b>                     |              |           |           |           |           |           |
| Bank 0                                                 | 9            | 20        | 20        | 21        | 21        | 21        |
| <b>Gearboxes</b>                                       |              |           |           |           |           |           |
| Number of 7:1 or 8:1 Output Gearbox Available (Bank 0) | 9            | 20        | 20        | 21        | 21        | 21        |
| Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)  | 14           | 20        | 20        | 21        | 21        | 21        |
| <b>DQS Groups</b>                                      |              |           |           |           |           |           |
| Bank 1                                                 | 2            | 2         | 2         | 2         | 2         | 2         |
| <b>VCCIO Pins</b>                                      |              |           |           |           |           |           |
| Bank 0                                                 | 3            | 4         | 4         | 4         | 5         | 10        |
| Bank 1                                                 | 3            | 4         | 4         | 4         | 5         | 10        |
| Bank 2                                                 | 3            | 4         | 4         | 4         | 5         | 10        |
| Bank 3                                                 | 1            | 1         | 1         | 2         | 2         | 3         |
| Bank 4                                                 | 1            | 2         | 2         | 1         | 2         | 4         |
| Bank 5                                                 | 1            | 1         | 1         | 2         | 2         | 3         |
|                                                        |              |           |           |           |           |           |
| VCC                                                    | 4            | 8         | 8         | 8         | 10        | 12        |
| GND                                                    | 12           | 24        | 24        | 27        | 33        | 48        |
| NC                                                     | 1            | 1         | 1         | 1         | 0         | 49        |
| Reserved for Configuration                             | 1            | 1         | 1         | 1         | 1         | 1         |
| Total Count of Bonded Pins                             | 144          | 256       | 256       | 332       | 400       | 484       |

## Ordering Information

MachXO2 devices have top-side markings, for commercial and industrial grades, as shown below:

|                                                        |                                       |
|--------------------------------------------------------|---------------------------------------|
| <b>LATTICE</b><br>LCMXO2-1200ZE<br>1TG100C<br>Datecode | LCMXO2<br>256ZE<br>1UG64C<br>Datecode |
|--------------------------------------------------------|---------------------------------------|

Notes:

1. Markings are abbreviated for small packages.
2. See [PCN 05A-12](#) for information regarding a change to the top-side mark logo.

| Part Number            | LUTs | Supply Voltage | Grade | Package            | Leads | Temp. |
|------------------------|------|----------------|-------|--------------------|-------|-------|
| LCMXO2-2000ZE-1TG100C  | 2112 | 1.2 V          | –1    | Halogen-Free TQFP  | 100   | COM   |
| LCMXO2-2000ZE-2TG100C  | 2112 | 1.2 V          | –2    | Halogen-Free TQFP  | 100   | COM   |
| LCMXO2-2000ZE-3TG100C  | 2112 | 1.2 V          | –3    | Halogen-Free TQFP  | 100   | COM   |
| LCMXO2-2000ZE-1MG132C  | 2112 | 1.2 V          | –1    | Halogen-Free csBGA | 132   | COM   |
| LCMXO2-2000ZE-2MG132C  | 2112 | 1.2 V          | –2    | Halogen-Free csBGA | 132   | COM   |
| LCMXO2-2000ZE-3MG132C  | 2112 | 1.2 V          | –3    | Halogen-Free csBGA | 132   | COM   |
| LCMXO2-2000ZE-1TG144C  | 2112 | 1.2 V          | –1    | Halogen-Free TQFP  | 144   | COM   |
| LCMXO2-2000ZE-2TG144C  | 2112 | 1.2 V          | –2    | Halogen-Free TQFP  | 144   | COM   |
| LCMXO2-2000ZE-3TG144C  | 2112 | 1.2 V          | –3    | Halogen-Free TQFP  | 144   | COM   |
| LCMXO2-2000ZE-1BG256C  | 2112 | 1.2 V          | –1    | Halogen-Free caBGA | 256   | COM   |
| LCMXO2-2000ZE-2BG256C  | 2112 | 1.2 V          | –2    | Halogen-Free caBGA | 256   | COM   |
| LCMXO2-2000ZE-3BG256C  | 2112 | 1.2 V          | –3    | Halogen-Free caBGA | 256   | COM   |
| LCMXO2-2000ZE-1FTG256C | 2112 | 1.2 V          | –1    | Halogen-Free ftBGA | 256   | COM   |
| LCMXO2-2000ZE-2FTG256C | 2112 | 1.2 V          | –2    | Halogen-Free ftBGA | 256   | COM   |
| LCMXO2-2000ZE-3FTG256C | 2112 | 1.2 V          | –3    | Halogen-Free ftBGA | 256   | COM   |

| Part Number            | LUTs | Supply Voltage | Grade | Package            | Leads | Temp. |
|------------------------|------|----------------|-------|--------------------|-------|-------|
| LCMXO2-4000ZE-1QN84C   | 4320 | 1.2 V          | –1    | Halogen-Free QFN   | 84    | COM   |
| LCMXO2-4000ZE-2QN84C   | 4320 | 1.2 V          | –2    | Halogen-Free QFN   | 84    | COM   |
| LCMXO2-4000ZE-3QN84C   | 4320 | 1.2 V          | –3    | Halogen-Free QFN   | 84    | COM   |
| LCMXO2-4000ZE-1MG132C  | 4320 | 1.2 V          | –1    | Halogen-Free csBGA | 132   | COM   |
| LCMXO2-4000ZE-2MG132C  | 4320 | 1.2 V          | –2    | Halogen-Free csBGA | 132   | COM   |
| LCMXO2-4000ZE-3MG132C  | 4320 | 1.2 V          | –3    | Halogen-Free csBGA | 132   | COM   |
| LCMXO2-4000ZE-1TG144C  | 4320 | 1.2 V          | –1    | Halogen-Free TQFP  | 144   | COM   |
| LCMXO2-4000ZE-2TG144C  | 4320 | 1.2 V          | –2    | Halogen-Free TQFP  | 144   | COM   |
| LCMXO2-4000ZE-3TG144C  | 4320 | 1.2 V          | –3    | Halogen-Free TQFP  | 144   | COM   |
| LCMXO2-4000ZE-1BG256C  | 4320 | 1.2 V          | –1    | Halogen-Free caBGA | 256   | COM   |
| LCMXO2-4000ZE-2BG256C  | 4320 | 1.2 V          | –2    | Halogen-Free caBGA | 256   | COM   |
| LCMXO2-4000ZE-3BG256C  | 4320 | 1.2 V          | –3    | Halogen-Free caBGA | 256   | COM   |
| LCMXO2-4000ZE-1FTG256C | 4320 | 1.2 V          | –1    | Halogen-Free ftBGA | 256   | COM   |
| LCMXO2-4000ZE-2FTG256C | 4320 | 1.2 V          | –2    | Halogen-Free ftBGA | 256   | COM   |
| LCMXO2-4000ZE-3FTG256C | 4320 | 1.2 V          | –3    | Halogen-Free ftBGA | 256   | COM   |
| LCMXO2-4000ZE-1BG332C  | 4320 | 1.2 V          | –1    | Halogen-Free caBGA | 332   | COM   |
| LCMXO2-4000ZE-2BG332C  | 4320 | 1.2 V          | –2    | Halogen-Free caBGA | 332   | COM   |
| LCMXO2-4000ZE-3BG332C  | 4320 | 1.2 V          | –3    | Halogen-Free caBGA | 332   | COM   |
| LCMXO2-4000ZE-1FG484C  | 4320 | 1.2 V          | –1    | Halogen-Free fpBGA | 484   | COM   |
| LCMXO2-4000ZE-2FG484C  | 4320 | 1.2 V          | –2    | Halogen-Free fpBGA | 484   | COM   |
| LCMXO2-4000ZE-3FG484C  | 4320 | 1.2 V          | –3    | Halogen-Free fpBGA | 484   | COM   |

| Part Number           | LUTs | Supply Voltage | Grade | Package            | Leads | Temp. |
|-----------------------|------|----------------|-------|--------------------|-------|-------|
| LCMXO2-1200HC-4SG32I  | 1280 | 2.5 V / 3.3 V  | –4    | Halogen-Free QFN   | 32    | IND   |
| LCMXO2-1200HC-5SG32I  | 1280 | 2.5 V / 3.3 V  | –5    | Halogen-Free QFN   | 32    | IND   |
| LCMXO2-1200HC-6SG32I  | 1280 | 2.5 V / 3.3 V  | –6    | Halogen-Free QFN   | 32    | IND   |
| LCMXO2-1200HC-4TG100I | 1280 | 2.5 V / 3.3 V  | –4    | Halogen-Free TQFP  | 100   | IND   |
| LCMXO2-1200HC-5TG100I | 1280 | 2.5 V / 3.3 V  | –5    | Halogen-Free TQFP  | 100   | IND   |
| LCMXO2-1200HC-6TG100I | 1280 | 2.5 V / 3.3 V  | –6    | Halogen-Free TQFP  | 100   | IND   |
| LCMXO2-1200HC-4MG132I | 1280 | 2.5 V / 3.3 V  | –4    | Halogen-Free csBGA | 132   | IND   |
| LCMXO2-1200HC-5MG132I | 1280 | 2.5 V / 3.3 V  | –5    | Halogen-Free csBGA | 132   | IND   |
| LCMXO2-1200HC-6MG132I | 1280 | 2.5 V / 3.3 V  | –6    | Halogen-Free csBGA | 132   | IND   |
| LCMXO2-1200HC-4TG144I | 1280 | 2.5 V / 3.3 V  | –4    | Halogen-Free TQFP  | 144   | IND   |
| LCMXO2-1200HC-5TG144I | 1280 | 2.5 V / 3.3 V  | –5    | Halogen-Free TQFP  | 144   | IND   |
| LCMXO2-1200HC-6TG144I | 1280 | 2.5 V / 3.3 V  | –6    | Halogen-Free TQFP  | 144   | IND   |

| Part Number             | LUTs | Supply Voltage | Grade | Package            | Leads | Temp. |
|-------------------------|------|----------------|-------|--------------------|-------|-------|
| LCMXO2-1200UHC-4FTG256I | 1280 | 2.5 V / 3.3 V  | –4    | Halogen-Free ftBGA | 256   | IND   |
| LCMXO2-1200UHC-5FTG256I | 1280 | 2.5 V / 3.3 V  | –5    | Halogen-Free ftBGA | 256   | IND   |
| LCMXO2-1200UHC-6FTG256I | 1280 | 2.5 V / 3.3 V  | –6    | Halogen-Free ftBGA | 256   | IND   |

| Part Number            | LUTs | Supply Voltage | Grade | Package            | Leads | Temp. |
|------------------------|------|----------------|-------|--------------------|-------|-------|
| LCMXO2-2000HC-4TG100I  | 2112 | 2.5 V / 3.3 V  | –4    | Halogen-Free TQFP  | 100   | IND   |
| LCMXO2-2000HC-5TG100I  | 2112 | 2.5 V / 3.3 V  | –5    | Halogen-Free TQFP  | 100   | IND   |
| LCMXO2-2000HC-6TG100I  | 2112 | 2.5 V / 3.3 V  | –6    | Halogen-Free TQFP  | 100   | IND   |
| LCMXO2-2000HC-4MG132I  | 2112 | 2.5 V / 3.3 V  | –4    | Halogen-Free csBGA | 132   | IND   |
| LCMXO2-2000HC-5MG132I  | 2112 | 2.5 V / 3.3 V  | –5    | Halogen-Free csBGA | 132   | IND   |
| LCMXO2-2000HC-6MG132I  | 2112 | 2.5 V / 3.3 V  | –6    | Halogen-Free csBGA | 132   | IND   |
| LCMXO2-2000HC-4TG144I  | 2112 | 2.5 V / 3.3 V  | –4    | Halogen-Free TQFP  | 144   | IND   |
| LCMXO2-2000HC-5TG144I  | 2112 | 2.5 V / 3.3 V  | –5    | Halogen-Free TQFP  | 144   | IND   |
| LCMXO2-2000HC-6TG144I  | 2112 | 2.5 V / 3.3 V  | –6    | Halogen-Free TQFP  | 144   | IND   |
| LCMXO2-2000HC-4BG256I  | 2112 | 2.5 V / 3.3 V  | –4    | Halogen-Free caBGA | 256   | IND   |
| LCMXO2-2000HC-5BG256I  | 2112 | 2.5 V / 3.3 V  | –5    | Halogen-Free caBGA | 256   | IND   |
| LCMXO2-2000HC-6BG256I  | 2112 | 2.5 V / 3.3 V  | –6    | Halogen-Free caBGA | 256   | IND   |
| LCMXO2-2000HC-4FTG256I | 2112 | 2.5 V / 3.3 V  | –4    | Halogen-Free ftBGA | 256   | IND   |
| LCMXO2-2000HC-5FTG256I | 2112 | 2.5 V / 3.3 V  | –5    | Halogen-Free ftBGA | 256   | IND   |
| LCMXO2-2000HC-6FTG256I | 2112 | 2.5 V / 3.3 V  | –6    | Halogen-Free ftBGA | 256   | IND   |

| Part Number            | LUTs | Supply Voltage | Grade | Package            | Leads | Temp. |
|------------------------|------|----------------|-------|--------------------|-------|-------|
| LCMXO2-2000UHC-4FG484I | 2112 | 2.5 V / 3.3 V  | –4    | Halogen-Free fpBGA | 484   | IND   |
| LCMXO2-2000UHC-5FG484I | 2112 | 2.5 V / 3.3 V  | –5    | Halogen-Free fpBGA | 484   | IND   |
| LCMXO2-2000UHC-6FG484I | 2112 | 2.5 V / 3.3 V  | –6    | Halogen-Free fpBGA | 484   | IND   |