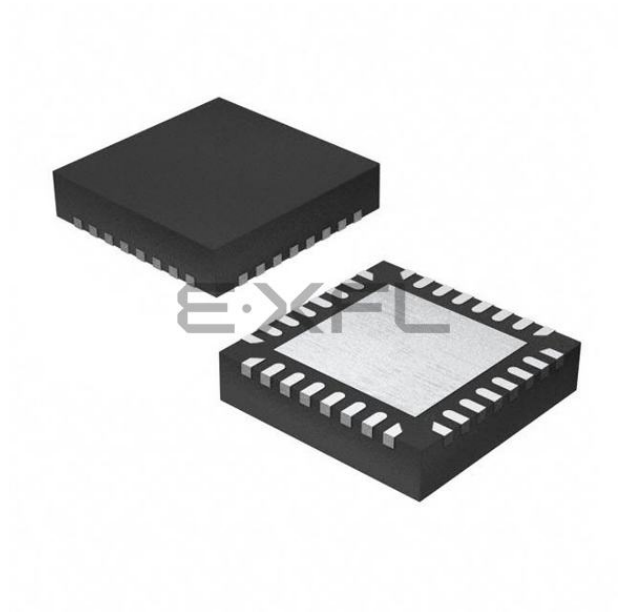
# Lattice Semiconductor Corporation - LCMXO2-256HC-5SG32C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

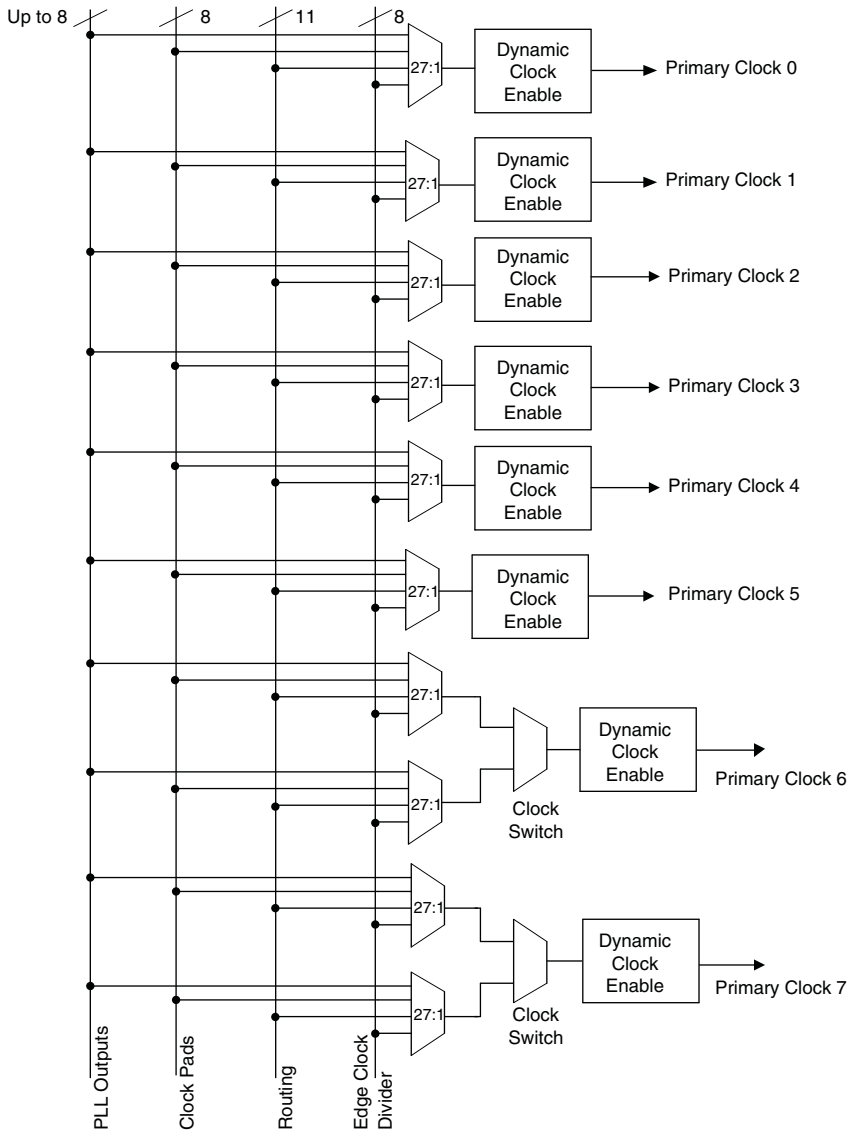
| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 32 |
| Number of Logic Elements/Cells | 256 |
| Total RAM Bits | - |
| Number of I/O | 21 |
| Number of Gates | - |
| Voltage - Supply | 2.375V ~ 3.465V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 32-UFQFN Exposed Pad |
| Supplier Device Package | 32-QFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-256hc-5sg32c |

*Table 1-1. MachXO2™ Family Selection Guide*

| | | XO2-256 | XO2-640 | XO2-640U[1] | XO2-1200 | XO2-1200U[1] | XO2-2000 | XO2-2000U[1] | XO2-4000 | XO2-7000 |
|---|---|---|---|---|---|---|---|---|---|---|
| LUTs | | 256 | 640 | 640 | 1280 | 1280 | 2112 | 2112 | 4320 | 6864 |
| Distributed RAM (kbits) | | 2 | 5 | 5 | 10 | 10 | 16 | 16 | 34 | 54 |
| EBR SRAM (kbits) | | 0 | 18 | 64 | 64 | 74 | 74 | 92 | 92 | 240 |
| Number of EBR SRAM Blocks (9 kbits/block) | | 0 | 2 | 7 | 7 | 8 | 8 | 10 | 10 | 26 |
| UFM (kbits) | | 0 | 24 | 64 | 64 | 80 | 80 | 96 | 96 | 256 |
| Device Options: | HC[2] | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | HE[3] | | | | | | Yes | Yes | Yes | Yes |
| | ZE[4] | Yes | Yes | | Yes | | Yes | | Yes | Yes |
| Number of PLLs | | 0 | 0 | 1 | 1 | 1 | 1 | 2 | 2 | 2 |
| Hardened Functions: | I2C | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | SPI | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Timer/Counter | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **Packages** | | | | | | **IO** | | | | |
| 25-ball WLCSP[5] (2.5 mm x 2.5 mm, 0.4 mm) | | | | | 18 | | | | | |
| 32 QFN[6] (5 mm x 5 mm, 0.5 mm) | | 21 | | | 21 | | | | | |
| 48 QFN[8, 9] (7 mm x 7 mm, 0.5 mm) | | 40 | 40 | | | | | | | |
| 49-ball WLCSP[5] (3.2 mm x 3.2 mm, 0.4 mm) | | | | | | | 38 | | | |
| 64-ball ucBGA (4 mm x 4 mm, 0.4 mm) | | 44 | | | | | | | | |
| 84 QFN[7] (7 mm x 7 mm, 0.5 mm) | | | | | | | | | 68 | |
| 100-pin TQFP (14 mm x 14 mm) | | 55 | 78 | | 79 | | 79 | | | |
| 132-ball csBGA (8 mm x 8 mm, 0.5 mm) | | 55 | 79 | | 104 | | 104 | | 104 | |
| 144-pin TQFP (20 mm x 20 mm) | | | | 107 | 107 | | 111 | | 114 | 114 |
| 184-ball csBGA[7] (8 mm x 8 mm, 0.5 mm) | | | | | | | | | 150 | |
| 256-ball caBGA (14 mm x 14 mm, 0.8 mm) | | | | | | | 206 | | 206 | 206 |
| 256-ball ftBGA (17 mm x 17 mm, 1.0 mm) | | | | | | 206 | 206 | | 206 | 206 |
| 332-ball caBGA (17 mm x 17 mm, 0.8 mm) | | | | | | | | | 274 | 278 |
| 484-ball ftBGA (23 mm x 23 mm, 1.0 mm) | | | | | | | | 278 | 278 | 334 |

1. Ultra high I/O device.
2. High performance with regulator – VCC = 2.5 V, 3.3 V
3. High performance without regulator – $V_{CC}$ = 1.2 V
4. Low power without regulator – $V_{CC}$ = 1.2 V
5. WLCSP package only available for ZE devices.
6. 32 QFN package only available for HC and ZE devices.
7. 184 csBGA package only available for HE devices.
8. 48-pin QFN information is ‘Advanced’.
9. 48 QFN package only available for HC devices.

*Figure 2-5. Primary Clocks for MachXO2 Devices*

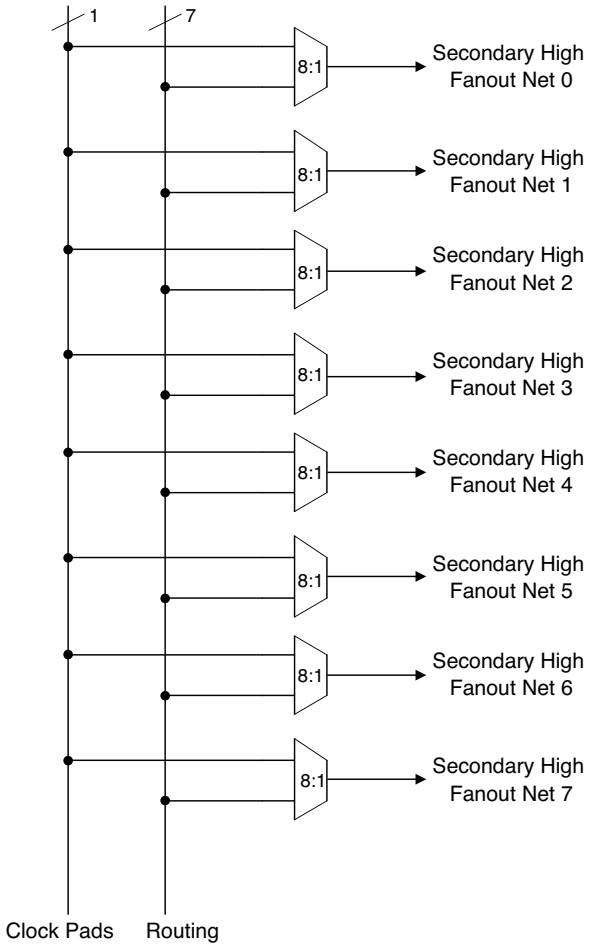



Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO2 External Switching Characteristics table.

*Figure 2-6. Secondary High Fanout Nets for MachXO2 Devices*




## sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The MachXO2-640U, MachXO2-1200/U and larger devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO2 sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO2 clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.

*Table 2-5. sysMEM Block Configurations*

| Memory Mode | Configurations |
|---|---|
| Single Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9 |
| True Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9 |
| Pseudo Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |
| FIFO | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |

**Bus Size Matching**

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

**RAM Initialization and ROM Operation**

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO2 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

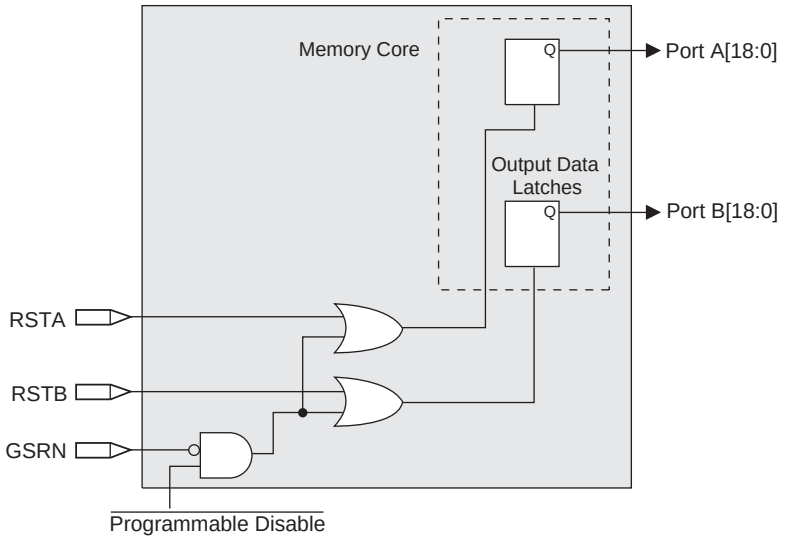
**Memory Cascading**

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

**Single, Dual, Pseudo-Dual Port and FIFO Modes**

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

*Figure 2-9. Memory Core Reset*

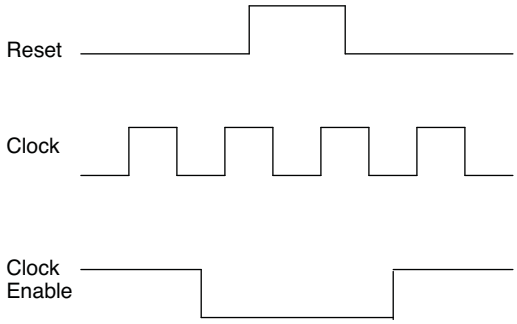



For further information on the sysMEM EBR block, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

**EBR Asynchronous Reset**

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

*Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram*



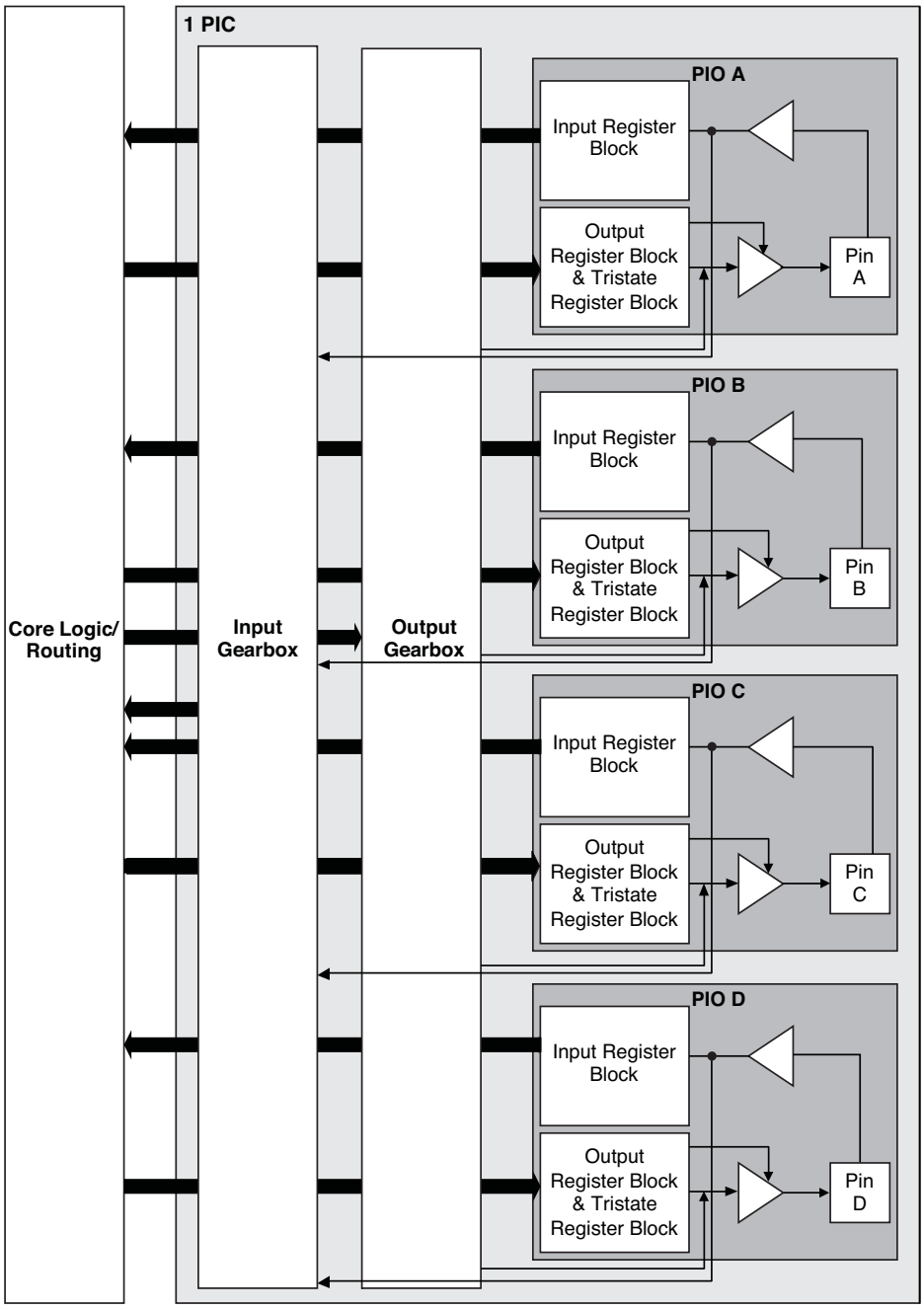

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-10. The reset timing rules apply to the RPReset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For more details refer to TN1201, Memory Usage Guide for MachXO2 Devices.

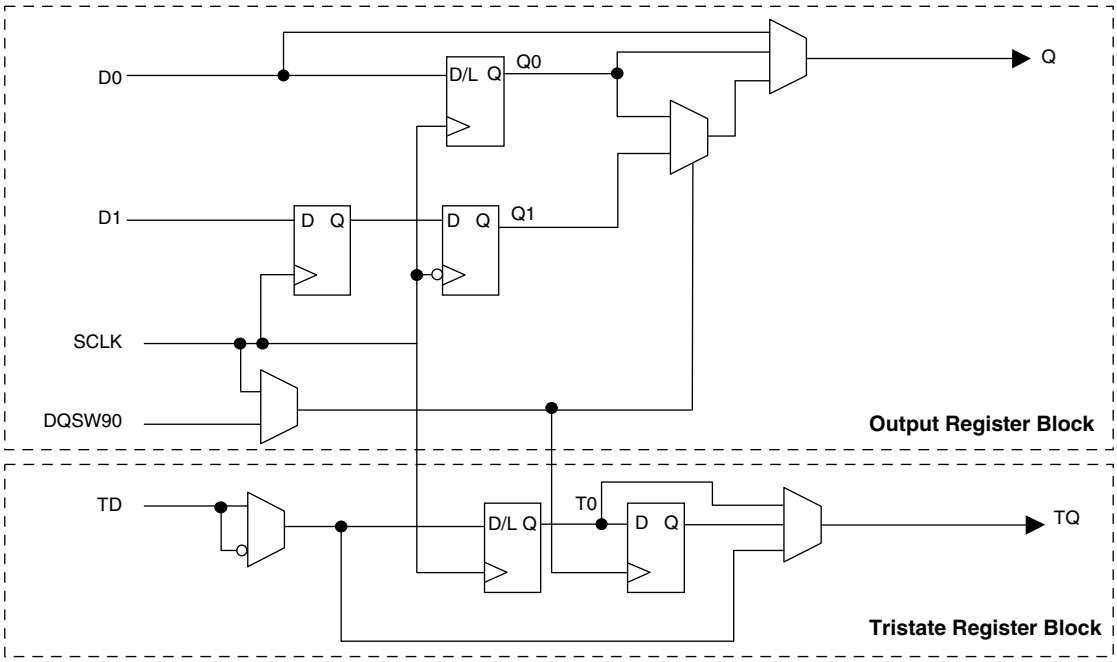
Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

*Figure 2-11. Group of Four Programmable I/O Cells*




Notes:
1. Input gearbox is available only in PIC on the bottom edge of MachXO2-640U, MachXO2-1200/U and larger devices.
2. Output gearbox is available only in PIC on the top edge of MachXO2-640U, MachXO2-1200/U and larger devices.

*Figure 2-15. MachXO2 Output Register Block Diagram (PIO on the Right Edges)*




## Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

The tri-state register blocks on the right edge contain an additional register for DDR memory operation. In DDR memory mode, the register TS input is fed into another register that is clocked using the DQSW90 signal. The output of this register is used as a tri-state control.

# Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

*Table 2-9. Input Gearbox Signal List*

| Name | I/O Type | Description |
|---|---|---|
| D | Input | High-speed data input after programmable delay in PIO A input register block |
| ALIGNWD | Input | Data alignment signal from device core |
| SCLK | Input | Slow-speed system clock |
| ECLK[1:0] | Input | High-speed edge clock |
| RST | Input | Reset |
| Q[7:0] | Output | Low-speed data to device core:<br>Video RX(1:7): Q[6:0]<br>GDDRX4(1:8): Q[7:0]<br>GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7<br>GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3 |

*Table 2-11. I/O Support Device by Device*

| | MachXO2-256, MachXO2-640 | MachXO2-640U, MachXO2-1200 | MachXO2-1200U MachXO2-2000/U, MachXO2-4000, MachXO2-7000 |
|---|---|---|---|
| Number of I/O Banks | 4 | 4 | 6 |
| Type of Input Buffers | Single-ended (all I/O banks)<br>Differential Receivers (all I/O banks) | Single-ended (all I/O banks)<br>Differential Receivers (all I/O banks)<br>Differential input termination (bottom side) | Single-ended (all I/O banks)<br>Differential Receivers (all I/O banks)<br>Differential input termination (bottom side) |
| Types of Output Buffers | Single-ended buffers with complementary outputs (all I/O banks) | Single-ended buffers with complementary outputs (all I/O banks)<br>Differential buffers with true LVDS outputs (50% on top side) | Single-ended buffers with complementary outputs (all I/O banks)<br>Differential buffers with true LVDS outputs (50% on top side) |
| Differential Output Emulation Capability | All I/O banks | All I/O banks | All I/O banks |
| PCI Clamp Support | No | Clamp on bottom side only | Clamp on bottom side only |

*Table 2-12. Supported Input Standards*

| | VCCIO (Typ.) | | | | |
|---|---|---|---|---|---|
| **Input Standard** | **3.3 V** | **2.5 V** | **1.8 V** | **1.5** | **1.2 V** |
| **Single-Ended Interfaces** | | | | | |
| LVTTL | ✓ | ✓[2] | ✓[2] | ✓[2] | |
| LVCMOS33 | ✓ | ✓[2] | ✓[2] | ✓[2] | |
| LVCMOS25 | ✓[2] | ✓ | ✓[2] | ✓[2] | |
| LVCMOS18 | ✓[2] | ✓[2] | ✓ | ✓[2] | |
| LVCMOS15 | ✓[2] | ✓[2] | ✓[2] | ✓ | ✓[2] |
| LVCMOS12 | ✓[2] | ✓[2] | ✓[2] | ✓[2] | ✓ |
| PCI[1] | ✓ | | | | |
| SSTL18 (Class I, Class II) | ✓ | ✓ | ✓ | | |
| SSTL25 (Class I, Class II) | ✓ | ✓ | | | |
| HSTL18 (Class I, Class II) | ✓ | ✓ | ✓ | | |
| **Differential Interfaces** | | | | | |
| LVDS | ✓ | ✓ | | | |
| BLVDS, MVDS, LVPECL, RSDS | ✓ | ✓ | | | |
| MIPI[3] | ✓ | ✓ | | | |
| Differential SSTL18 Class I, II | ✓ | ✓ | ✓ | | |
| Differential SSTL25 Class I, II | ✓ | ✓ | | | |
| Differential HSTL18 Class I, II | ✓ | ✓ | ✓ | | |

1. Bottom banks of MachXO2-640U, MachXO2-1200/U and higher density devices only.
2. Reduced functionality. Refer to TN1202, MachXO2 sysIO Usage Guide for more detail.
3. These interfaces can be emulated with external resistors in all devices.

## Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  — Watchdog timer
  — Clear timer on compare match
  — Fast PWM
  — Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

***Figure 2-23. Timer/Counter Block Diagram***

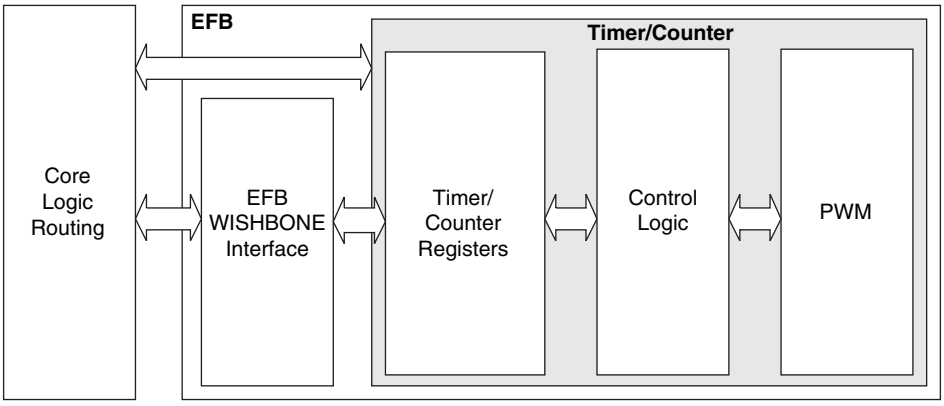



***Table 2-17. Timer/Counter Signal Description***

| Port | I/O | Description |
|---|---|---|
| tc_clki | I | Timer/Counter input clock signal |
| tc_rstn | I | Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled |
| tc_ic | I | Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping. |
| tc_int | O | Without WISHBONE – Can be used as overflow flag<br>With WISHBONE – Controlled by three IRQ registers |
| tc_oc | O | Timer counter output signal |

## sysIO Recommended Operating Conditions

| Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| LVCMOS 3.3 | 3.135 | 3.3 | 3.6 | — | — | — |
| LVCMOS 2.5 | 2.375 | 2.5 | 2.625 | — | — | — |
| LVCMOS 1.8 | 1.71 | 1.8 | 1.89 | — | — | — |
| LVCMOS 1.5 | 1.425 | 1.5 | 1.575 | — | — | — |
| LVCMOS 1.2 | 1.14 | 1.2 | 1.26 | — | — | — |
| LVTTL | 3.135 | 3.3 | 3.6 | — | — | — |
| PCI[3] | 3.135 | 3.3 | 3.6 | — | — | — |
| SSTL25 | 2.375 | 2.5 | 2.625 | 1.15 | 1.25 | 1.35 |
| SSTL18 | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |
| HSTL18 | 1.71 | 1.8 | 1.89 | 0.816 | 0.9 | 1.08 |
| LVCMOS25R33 | 3.135 | 3.3 | 3.6 | 1.1 | 1.25 | 1.4 |
| LVCMOS18R33 | 3.135 | 3.3 | 3.6 | 0.75 | 0.9 | 1.05 |
| LVCMOS18R25 | 2.375 | 2.5 | 2.625 | 0.75 | 0.9 | 1.05 |
| LVCMOS15R33 | 3.135 | 3.3 | 3.6 | 0.6 | 0.75 | 0.9 |
| LVCMOS15R25 | 2.375 | 2.5 | 2.625 | 0.6 | 0.75 | 0.9 |
| LVCMOS12R33[4] | 3.135 | 3.3 | 3.6 | 0.45 | 0.6 | 0.75 |
| LVCMOS12R25[4] | 2.375 | 2.5 | 2.625 | 0.45 | 0.6 | 0.75 |
| LVCMOS10R33[4] | 3.135 | 3.3 | 3.6 | 0.35 | 0.5 | 0.65 |
| LVCMOS10R25[4] | 2.375 | 2.5 | 2.625 | 0.35 | 0.5 | 0.65 |
| LVDS25[1, 2] | 2.375 | 2.5 | 2.625 | — | — | — |
| LVDS33[1, 2] | 3.135 | 3.3 | 3.6 | — | — | — |
| LVPECL[1] | 3.135 | 3.3 | 3.6 | — | — | — |
| BLVDS[1] | 2.375 | 2.5 | 2.625 | — | — | — |
| RSDS[1] | 2.375 | 2.5 | 2.625 | — | — | — |
| SSTL18D | 1.71 | 1.8 | 1.89 | — | — | — |
| SSTL25D | 2.375 | 2.5 | 2.625 | — | — | — |
| HSTL18D | 1.71 | 1.8 | 1.89 | — | — | — |

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
3. Input on the bottom bank of the MachXO2-640U, MachXO2-1200/U and larger devices only.
4. Supported only for inputs and BIDIs for all ZE devices, and –6 speed grade for HE and HC devices.

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ Max. (V) | $V_{OH}$ Min. (V) | $I_{OL}$ Max.[4] (mA) | $I_{OH}$ Max.[4] (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min. (V)[3] | Max. (V) | Min. (V) | Max. (V) | | | | |
| LVCMOS10R25 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.40 | NA Open Drain | 16, 12, 8, 4 | NA Open Drain |

1. MachXO2 devices allow LVCMOS inputs to be placed in I/O banks where $V_{CCIO}$ is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO2 devices do not meet the relevant JEDEC specification are documented in the table below.
2. MachXO2 devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1202, MachXO2 sysIO Usage Guide.
3. The dual function $I^2C$ pins SCL and SDA are limited to a $V_{IL}$ min of –0.25 V or to –0.3 V with a duration of <10 ns.
4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive VCCIO or GND pad connections, or between the last VCCIO or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n * 8 mA. “n” is the number of I/O pads between the two consecutive bank VCCIO or GND connections or between the last VCCIO and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

| Input Standard | $V_{CCIO}$ (V) | $V_{IL}$ Max. (V) |
|---|---|---|
| LVCMOS 33 | 1.5 | 0.685 |
| LVCMOS 25 | 1.5 | 0.687 |
| LVCMOS 18 | 1.5 | 0.655 |

## sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of MachXO2-640U, MachXO2-1200/U and higher density devices in the MachXO2 PLD family.

### LVDS

**Over Recommended Operating Conditions**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | $V_{CCIO}$ = 3.3 V | 0 | — | 2.605 | V |
| | | $V_{CCIO}$ = 2.5 V | 0 | — | 2.05 | V |
| $V_{THD}$ | Differential Input Threshold | | ±100 | — | | mV |
| $V_{CM}$ | Input Common Mode Voltage | $V_{CCIO}$ = 3.3 V | 0.05 | — | 2.6 | V |
| | | $V_{CCIO}$ = 2.5 V | 0.05 | — | 2.0 | V |
| $I_{IN}$ | Input current | Power on | — | — | ±10 | µA |
| $V_{OH}$ | Output high voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ohm | — | 1.375 | — | V |
| $V_{OL}$ | Output low voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ohm | 0.90 | 1.025 | — | V |
| $V_{OD}$ | Output voltage differential | ($V_{OP}$ - $V_{OM}$), $R_T$ = 100 Ohm | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between high and low | | — | — | 50 | mV |
| $V_{OS}$ | Output voltage offset | ($V_{OP}$ + $V_{OM}$)/2, $R_T$ = 100 Ohm | 1.125 | 1.20 | 1.395 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ between H and L | | — | — | 50 | mV |
| $I_{OSD}$ | Output short circuit current | $V_{OD}$ = 0 V driver outputs shorted | — | — | 24 | mA |

# Typical Building Block Function Performance – ZE Devices[1]

## Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

| Function | –3 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit decoder | 13.9 | ns |
| 4:1 MUX | 10.9 | ns |
| 16:1 MUX | 12.0 | ns |

## Register-to-Register Performance

| Function | –3 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16:1 MUX | 191 | MHz |
| 16-bit adder | 134 | MHz |
| 16-bit counter | 148 | MHz |
| 64-bit counter | 77 | MHz |
| **Embedded Memory Functions** | | |
| 1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers) | 90 | MHz |
| **Distributed Memory Functions** | | |
| 16x4 Pseudo-Dual Port RAM (one PFU) | 214 | MHz |

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

# Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

# MachXO2 External Switching Characteristics – ZE Devices[1, 2, 3, 4, 5, 6, 7]

**Over Recommended Operating Conditions**

| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Clocks** | | | | | | | | | |
| **Primary Clocks** | | | | | | | | | |
| $f_{MAX\_PRI}$[8] | Frequency for Primary Clock Tree | All MachXO2 devices | — | 150 | — | 125 | — | 104 | MHz |
| $t_{W\_PRI}$ | Clock Pulse Width for Primary Clock | All MachXO2 devices | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| $t_{SKEW\_PRI}$ | Primary Clock Skew Within a Device | MachXO2-256ZE | — | 1250 | — | 1272 | — | 1296 | ps |
| | | MachXO2-640ZE | — | 1161 | — | 1183 | — | 1206 | ps |
| | | MachXO2-1200ZE | — | 1213 | — | 1267 | — | 1322 | ps |
| | | MachXO2-2000ZE | — | 1204 | — | 1250 | — | 1296 | ps |
| | | MachXO2-4000ZE | — | 1195 | — | 1233 | — | 1269 | ps |
| | | MachXO2-7000ZE | — | 1243 | — | 1268 | — | 1296 | ps |
| **Edge Clock** | | | | | | | | | |
| $f_{MAX\_EDGE}$[8] | Frequency for Edge Clock | MachXO2-1200 and larger devices | — | 210 | — | 175 | — | 146 | MHz |
| **Pin-LUT-Pin Propagation Delay** | | | | | | | | | |
| $t_{PD}$ | Best case propagation delay through one LUT-4 | All MachXO2 devices | — | 9.35 | — | 9.78 | — | 10.21 | ns |
| **General I/O Pin Parameters (Using Primary Clock without PLL)** | | | | | | | | | |
| $t_{CO}$ | Clock to Output – PIO Output Register | MachXO2-256ZE | — | 10.46 | — | 10.86 | — | 11.25 | ns |
| | | MachXO2-640ZE | — | 10.52 | — | 10.92 | — | 11.32 | ns |
| | | MachXO2-1200ZE | — | 11.24 | — | 11.68 | — | 12.12 | ns |
| | | MachXO2-2000ZE | — | 11.27 | — | 11.71 | — | 12.16 | ns |
| | | MachXO2-4000ZE | — | 11.28 | — | 11.78 | — | 12.28 | ns |
| | | MachXO2-7000ZE | — | 11.22 | — | 11.76 | — | 12.30 | ns |
| $t_{SU}$ | Clock to Data Setup – PIO Input Register | MachXO2-256ZE | –0.21 | — | –0.21 | — | –0.21 | — | ns |
| | | MachXO2-640ZE | –0.22 | — | –0.22 | — | –0.22 | — | ns |
| | | MachXO2-1200ZE | –0.25 | — | –0.25 | — | –0.25 | — | ns |
| | | MachXO2-2000ZE | –0.27 | — | –0.27 | — | –0.27 | — | ns |
| | | MachXO2-4000ZE | –0.31 | — | –0.31 | — | –0.31 | — | ns |
| | | MachXO2-7000ZE | –0.33 | — | –0.33 | — | –0.33 | — | ns |
| $t_{H}$ | Clock to Data Hold – PIO Input Register | MachXO2-256ZE | 3.96 | — | 4.25 | — | 4.65 | — | ns |
| | | MachXO2-640ZE | 4.01 | — | 4.31 | — | 4.71 | — | ns |
| | | MachXO2-1200ZE | 3.95 | — | 4.29 | — | 4.73 | — | ns |
| | | MachXO2-2000ZE | 3.94 | — | 4.29 | — | 4.74 | — | ns |
| | | MachXO2-4000ZE | 3.96 | — | 4.36 | — | 4.87 | — | ns |
| | | MachXO2-7000ZE | 3.93 | — | 4.37 | — | 4.91 | — | ns |

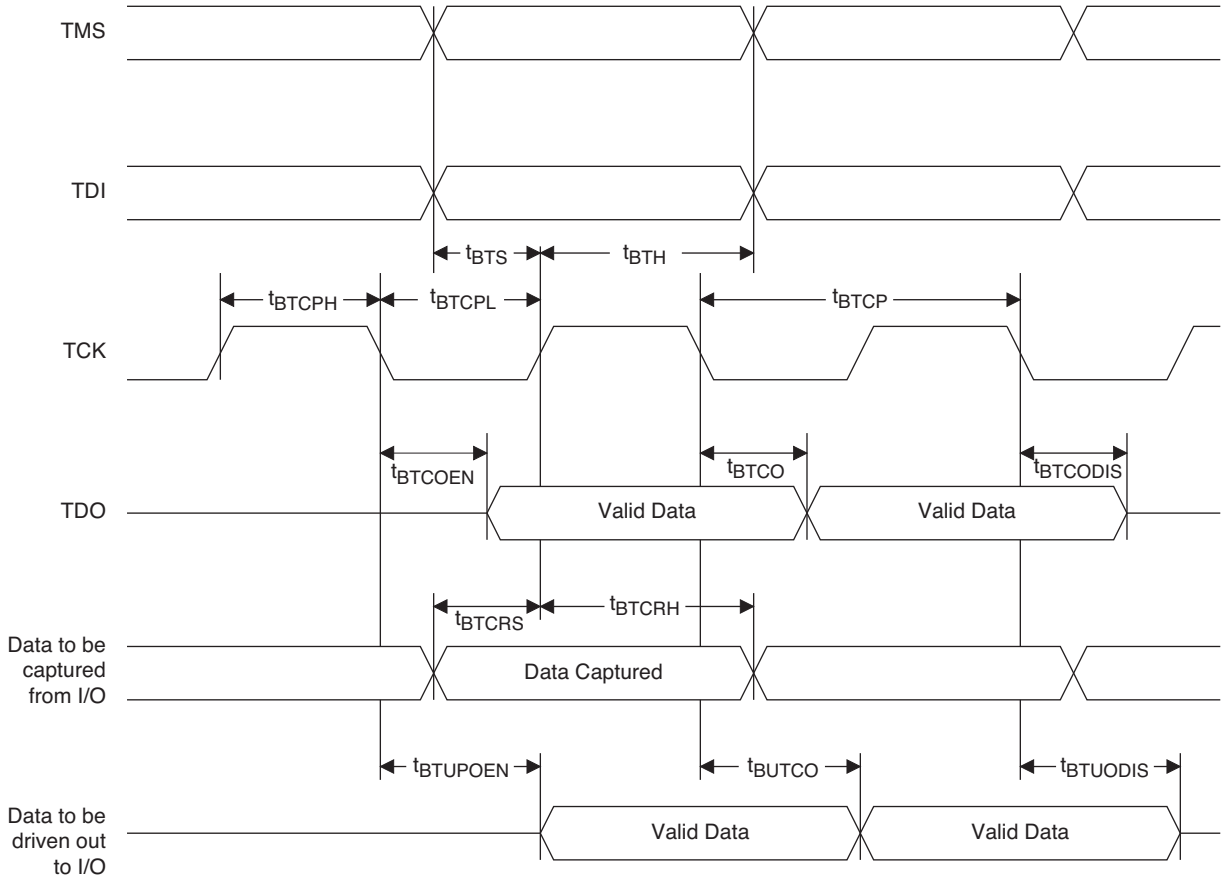
## sysCLOCK PLL Timing (Continued)

**Over Recommended Operating Conditions**

| Parameter | Descriptions | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $t_{ROTATE\_WD}$ | PHASESTEP Pulse Width | | 4 | — | VCO Cycles |

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after $t_{LOCK}$ for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide for more details.
5. At minimum $f_{PFD.}$ As the $f_{PFD}$ increases the time will decrease to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

*Figure 3-12. JTAG Port Timing Waveforms*



| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000ZE-1TG100C | 2112 | 1.2 V | –1 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000ZE-2TG100C | 2112 | 1.2 V | –2 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000ZE-3TG100C | 2112 | 1.2 V | –3 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000ZE-1MG132C | 2112 | 1.2 V | –1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000ZE-2MG132C | 2112 | 1.2 V | –2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000ZE-3MG132C | 2112 | 1.2 V | –3 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000ZE-1TG144C | 2112 | 1.2 V | –1 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000ZE-2TG144C | 2112 | 1.2 V | –2 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000ZE-3TG144C | 2112 | 1.2 V | –3 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000ZE-1BG256C | 2112 | 1.2 V | –1 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000ZE-2BG256C | 2112 | 1.2 V | –2 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000ZE-3BG256C | 2112 | 1.2 V | –3 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000ZE-1FTG256C | 2112 | 1.2 V | –1 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000ZE-2FTG256C | 2112 | 1.2 V | –2 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000ZE-3FTG256C | 2112 | 1.2 V | –3 | Halogen-Free ftBGA | 256 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000ZE-1QN84C | 4320 | 1.2 V | –1 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000ZE-2QN84C | 4320 | 1.2 V | –2 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000ZE-3QN84C | 4320 | 1.2 V | –3 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000ZE-1MG132C | 4320 | 1.2 V | –1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000ZE-2MG132C | 4320 | 1.2 V | –2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000ZE-3MG132C | 4320 | 1.2 V | –3 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000ZE-1TG144C | 4320 | 1.2 V | –1 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000ZE-2TG144C | 4320 | 1.2 V | –2 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000ZE-3TG144C | 4320 | 1.2 V | –3 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000ZE-1BG256C | 4320 | 1.2 V | –1 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000ZE-2BG256C | 4320 | 1.2 V | –2 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000ZE-3BG256C | 4320 | 1.2 V | –3 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000ZE-1FTG256C | 4320 | 1.2 V | –1 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000ZE-2FTG256C | 4320 | 1.2 V | –2 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000ZE-3FTG256C | 4320 | 1.2 V | –3 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000ZE-1BG332C | 4320 | 1.2 V | –1 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000ZE-2BG332C | 4320 | 1.2 V | –2 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000ZE-3BG332C | 4320 | 1.2 V | –3 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000ZE-1FG484C | 4320 | 1.2 V | –1 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000ZE-2FG484C | 4320 | 1.2 V | –2 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000ZE-3FG484C | 4320 | 1.2 V | –3 | Halogen-Free fpBGA | 484 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-1200ZE-1TG100IR1[1] | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-2TG100IR1[1] | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-3TG100IR1[1] | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-1MG132IR1[1] | 1280 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-2MG132IR1[1] | 1280 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-3MG132IR1[1] | 1280 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-1TG144IR1[1] | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200ZE-2TG144IR1[1] | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200ZE-3TG144IR1[1] | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 144 | IND |

1. Specifications for the “LCMXO2-1200ZE-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000HE-4MG132I | 4320 | 1.2 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HE-5MG132I | 4320 | 1.2 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HE-6MG132I | 4320 | 1.2 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HE-4TG144I | 4320 | 1.2 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HE-5TG144I | 4320 | 1.2 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HE-6TG144I | 4320 | 1.2 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HE-4MG184I | 4320 | 1.2 V | –4 | Halogen-Free csBGA | 184 | IND |
| LCMXO2-4000HE-5MG184I | 4320 | 1.2 V | –5 | Halogen-Free csBGA | 184 | IND |
| LCMXO2-4000HE-6MG184I | 4320 | 1.2 V | –6 | Halogen-Free csBGA | 184 | IND |
| LCMXO2-4000HE-4BG256I | 4320 | 1.2 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HE-5BG256I | 4320 | 1.2 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HE-6BG256I | 4320 | 1.2 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HE-4FTG256I | 4320 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HE-5FTG256I | 4320 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HE-6FTG256I | 4320 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HE-4BG332I | 4320 | 1.2 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HE-5BG332I | 4320 | 1.2 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HE-6BG332I | 4320 | 1.2 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HE-4FG484I | 4320 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HE-5FG484I | 4320 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HE-6FG484I | 4320 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000HE-4TG144I | 6864 | 1.2 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HE-5TG144I | 6864 | 1.2 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HE-6TG144I | 6864 | 1.2 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HE-4BG256I | 6864 | 1.2 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HE-5BG256I | 6864 | 1.2 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HE-6BG256I | 6864 | 1.2 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HE-4FTG256I | 6864 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HE-5FTG256I | 6864 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HE-6FTG256I | 6864 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HE-4BG332I | 6864 | 1.2 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HE-5BG332I | 6864 | 1.2 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HE-6BG332I | 6864 | 1.2 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HE-4FG484I | 6864 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HE-5FG484I | 6864 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HE-6FG484I | 6864 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | IND |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| May 2014 | 2.5 | Architecture | Updated TransFR (Transparent Field Reconfiguration) section.<br>Updated TransFR description for PLL use during background Flash programming. |
| February 2014 | 02.4 | Introduction | Included the 49 WLCSP package in the MachXO2 Family Selection Guide table. |
| | | Architecture | Added information to Standby Mode and Power Saving Options section. |
| | | Pinout Information | Added the XO2-2000 49 WLCSP in the Pinout Information Summary table. |
| | | Ordering Information | Added UW49 package in MachXO2 Part Number Description. |
| | | | Added and LCMXO2-2000ZE-1UWG49CTR in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging section. |
| | | | Added and LCMXO2-2000ZE-1UWG49ITR in Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. |
| December 2013 | 02.3 | Architecture | Updated information on CLKOS output divider in sysCLOCK Phase Locked Loops (PLLs) section. |
| | | DC and Switching Characteristics | Updated Static Supply Current – ZE Devices table. |
| | | | Updated footnote 4 in sysIO Single-Ended DC Electrical Characteristics table; Updated $V_{IL}$ Max. (V) data for LVCMOS 25 and LVCMOS 28. |
| | | | Updated $V_{OS}$ test condition in sysIO Differential Electrical Characteristics - LVDS table. |
| September 2013 | 02.2 | Architecture | Removed $I^2C$ Clock-Stretching feature per PCN #10A-13. |
| | | | Removed information on PDPR memory in RAM Mode section. |
| | | | Updated Supported Input Standards table. |
| | | DC and Switching Characteristics | Updated Power-On-Reset Voltage Levels table. |
| June 2013 | 02.1 | Architecture | Architecture Overview – Added information on the state of the register on power up and after configuration. |
| | | | sysCLOCK Phase Locked Loops (PLLs) section – Added missing cross reference to sysCLOCK PLL Timing table. |
| | | DC and Switching Characteristics | Added slew rate information to footnote 2 of the MachXO2 External Switching Characteristics – HC/HE Devices and the MachXO2 External Switching Characteristics – ZE Devices tables. |
| | | | Power-On-Reset Voltage Levels table – Added symbols. |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| May 2011 | 01.3 | Multiple | Replaced “SED” with “SRAM CRC Error Detection” throughout the document. |
| | | DC and Switching Characteristics | Added footnote 1 to Program Erase Specifications table. |
| | | Pinout Information | Updated Pin Information Summary tables. |
| | | | Signal name SO/SISPISO changed to SO/SPISO in the Signal Descriptions table. |
| April 2011 | 01.2 | — | Data sheet status changed from Advance to Preliminary. |
| | | Introduction | Updated MachXO2 Family Selection Guide table. |
| | | Architecture | Updated Supported Input Standards table. |
| | | | Updated sysMEM Memory Primitives diagram. |
| | | | Added differential SSTL and HSTL IO standards. |
| | | DC and Switching Characteristics | Updates following parameters: POR voltage levels, DC electrical characteristics, static supply current for ZE/HE/HC devices, static power consumption contribution of different components – ZE devices, programming and erase Flash supply current. |
| | | | Added VREF specifications to sysIO recommended operating conditions. |
| | | | Updating timing information based on characterization. |
| | | | Added differential SSTL and HSTL IO standards. |
| | | Ordering Information | Added Ordering Part Numbers for R1 devices, and devices in WLCSP packages. |
| | | | Added R1 device specifications. |
| January 2011 | 01.1 | All | Included ultra-high I/O devices. |
| | | DC and Switching Characteristics | Recommended Operating Conditions table – Added footnote 3. |
| | | | DC Electrical Characteristics table – Updated data for $I_{IL}$, $I_{IH}$. $V_{HYST}$ typical values updated. |
| | | | Generic DDRX2 Outputs with Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for $T_{DIA}$ and $T_{DIB}$. |
| | | | Generic DDRX4 Outputs with Clock and Data Aligned at Pin (GDDRX4_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for $T_{DIA}$ and $T_{DIB}$. |
| | | | Power-On-Reset Voltage Levels table - clarified note 3. |
| | | | Clarified VCCIO related recommended operating conditions specifications. |
| | | | Added power supply ramp rate requirements. |
| | | | Added Power Supply Ramp Rates table. |
| | | | Updated Programming/Erase Specifications table. |
| | | | Removed references to $V_{CCP}$. |
| | | Pinout Information | Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables. |
| | | | Removed references to $V_{CCP}$. |
| November 2010 | 01.0 | — | Initial release. |