# Lattice Semiconductor Corporation - LCMXO2-256HC-5TG100C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

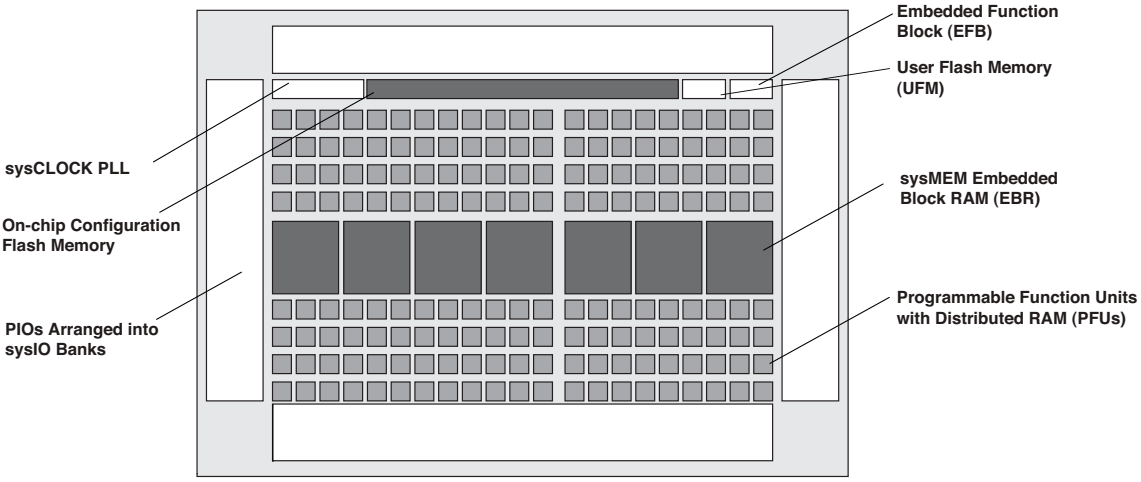
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 32 |
| Number of Logic Elements/Cells | 256 |
| Total RAM Bits | - |
| Number of I/O | 55 |
| Number of Gates | - |
| Voltage - Supply | 2.375V ~ 3.465V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-256hc-5tg100c |

## Architecture Overview

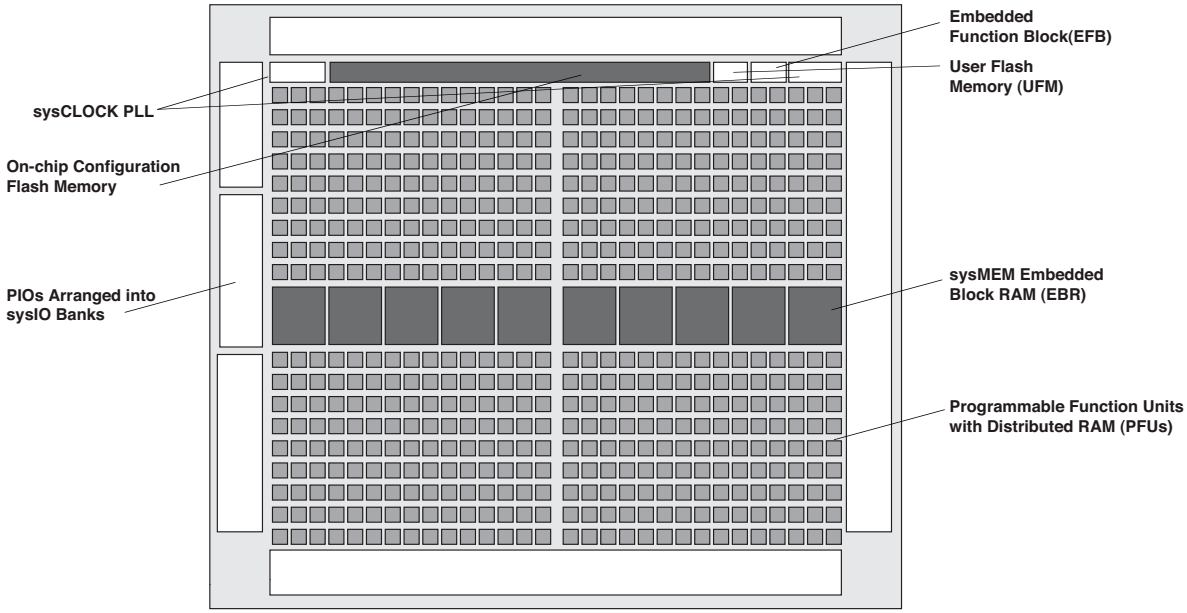
The MachXO2 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.

***Figure 2-1. Top View of the MachXO2-1200 Device***



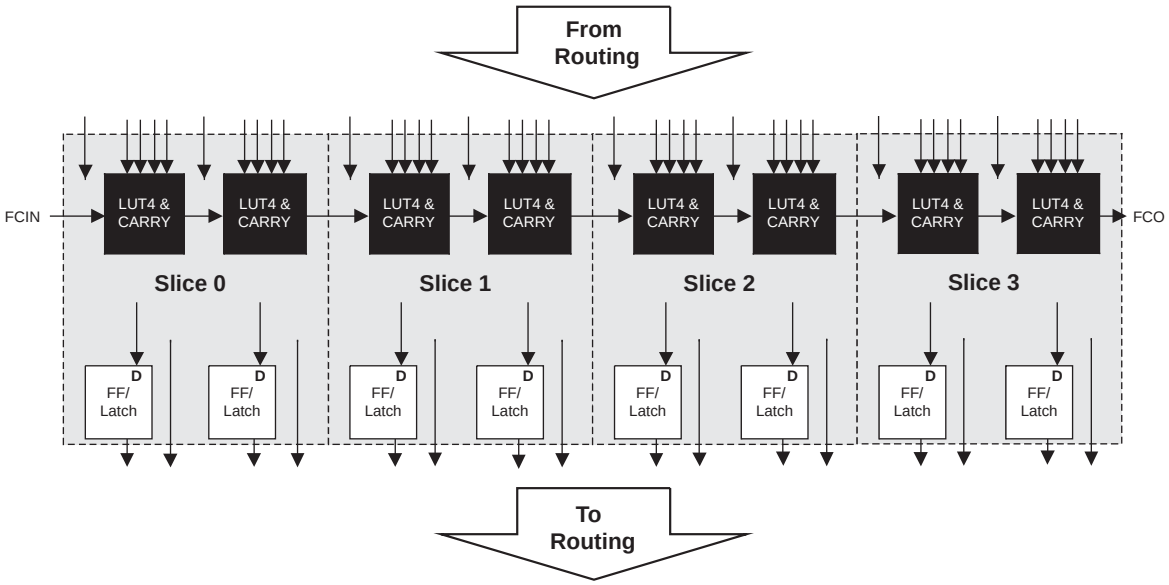

Note: MachXO2-256, and MachXO2-640/U are similar to MachXO2-1200. MachXO2-256 has a lower LUT count and no PLL or EBR blocks. MachXO2-640 has no PLL, a lower LUT count and two EBR blocks. MachXO2-640U has a lower LUT count, one PLL and seven EBR blocks.

***Figure 2-2. Top View of the MachXO2-4000 Device***




Note: MachXO2-1200U, MachXO2-2000/U and MachXO2-7000 are similar to MachXO2-4000. MachXO2-1200U and MachXO2-2000 have a lower LUT count, one PLL, and eight EBR blocks. MachXO2-2000U has a lower LUT count, two PLLs, and 10 EBR blocks. MachXO2-7000 has a higher LUT count, two PLLs, and 26 EBR blocks.

*Figure 2-3. PFU Block Diagram*




## Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

*Table 2-1. Resources and Modes Available per Slice*

| Slice | PFU Block | |
|---|---|---|
| | Resources | Modes |
| Slice 0 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 1 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 2 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 3 | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.

### ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

## Routing

There are many resources provided in the MachXO2 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

## Clock/Control Distribution Network

Each MachXO2 device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO2 architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO2-640U, MachXO2-1200/U and higher density devices have two edge clocks each on the top and bottom edges. Lower density devices have no edge clocks. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO2 devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO2 External Switching Characteristics table.

The primary clock signals for the MachXO2-256 and MachXO2-640 are generated from eight 17:1 muxes The available clock sources include eight I/O sources and 9 routing inputs. Primary clock signals for the MachXO2-640U, MachXO2-1200/U and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.

*Table 2-5. sysMEM Block Configurations*

| Memory Mode | Configurations |
|---|---|
| Single Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9 |
| True Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9 |
| Pseudo Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |
| FIFO | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |

**Bus Size Matching**

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

**RAM Initialization and ROM Operation**

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO2 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

**Memory Cascading**

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

**Single, Dual, Pseudo-Dual Port and FIFO Modes**

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

*Figure 2-8. sysMEM Memory Primitives*

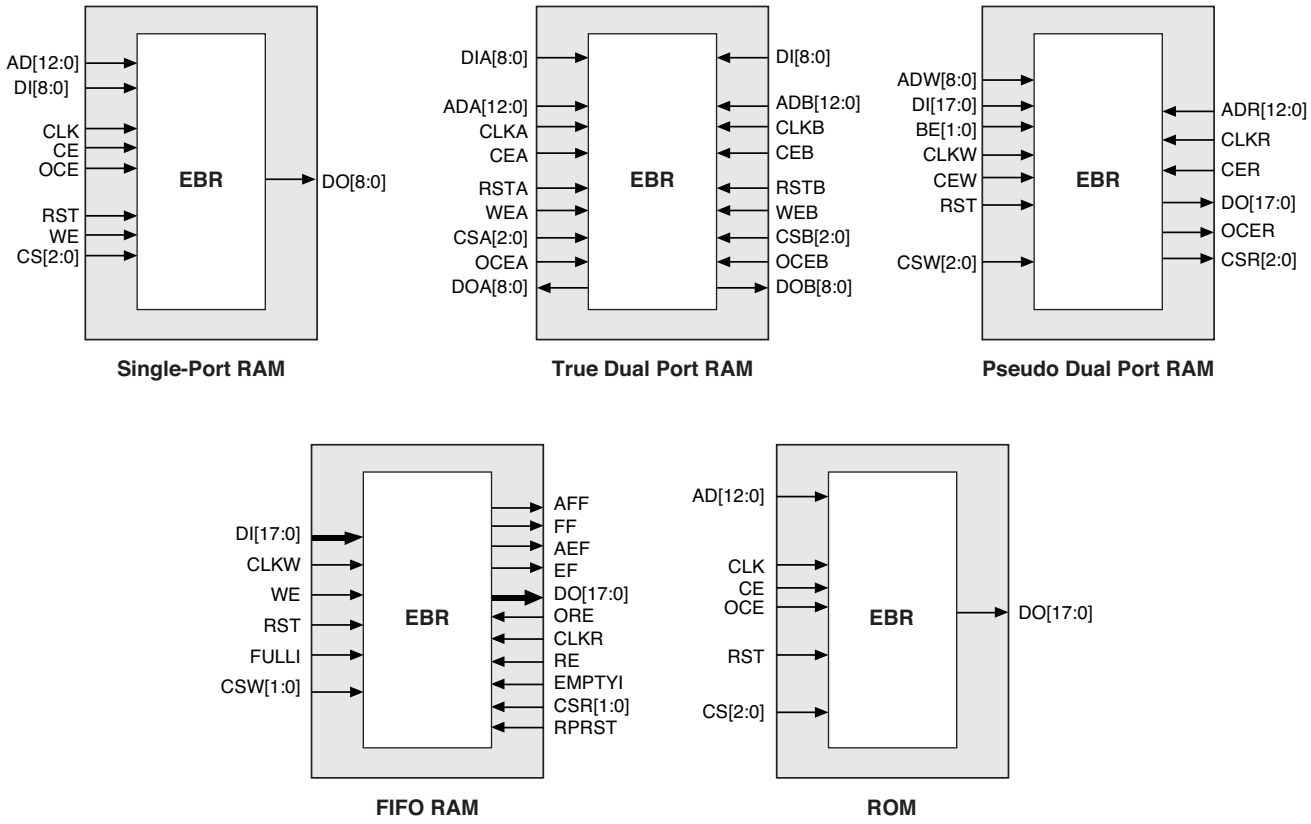
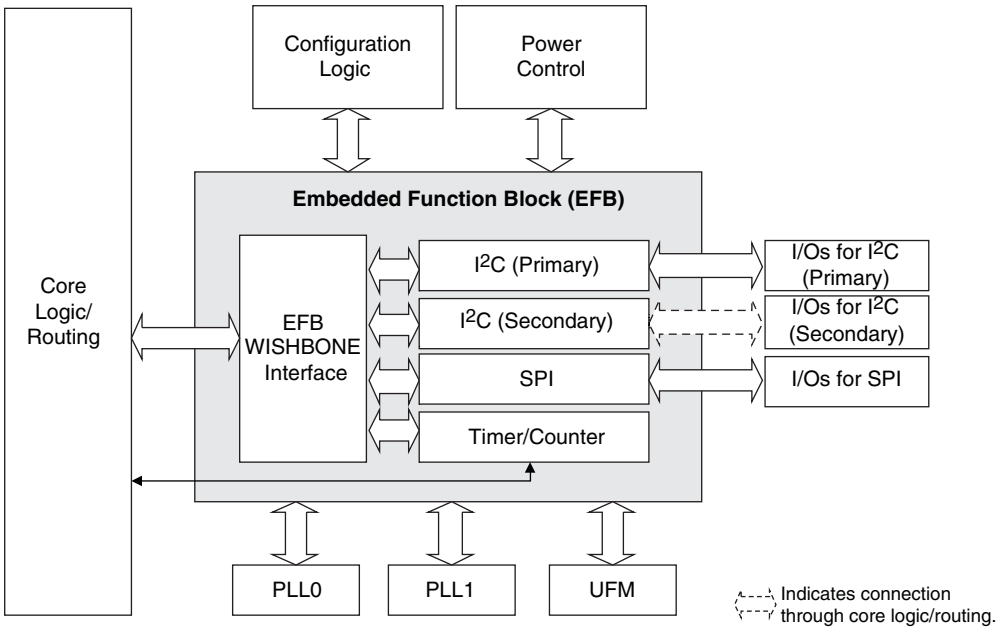



*Table 2-6. EBR Signal Descriptions*

| Port Name | Description | Active State |
|---|---|---|
| CLK | Clock | Rising Clock Edge |
| CE | Clock Enable | Active High |
| OCE[1] | Output Clock Enable | Active High |
| RST | Reset | Active High |
| BE[1] | Byte Enable | Active High |
| WE | Write Enable | Active High |
| AD | Address Bus | — |
| DI | Data In | — |
| DO | Data Out | — |
| CS | Chip Select | Active High |
| AFF | FIFO RAM Almost Full Flag | — |
| FF | FIFO RAM Full Flag | — |
| AEF | FIFO RAM Almost Empty Flag | — |
| EF | FIFO RAM Empty Flag | — |
| RPRST | FIFO RAM Read Pointer Reset | — |

1. Optional signals.
2. For dual port EBR primitives a trailing ‘A’ or ‘B’ in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing ‘R’ or ‘W’ in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

*Figure 2-20. Embedded Function Block Interface*




## Hardened I²C IP Core

Every MachXO2 device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I²C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface

*Table 2-18. MachXO2 Power Saving Features Description*

| Device Subsystem | Feature Description |
|---|---|
| Bandgap | The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices. |
| Power-On-Reset (POR) | The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe $V_{CC}$ drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable. |
| On-Chip Oscillator | The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode. |
| PLL | Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off. |
| I/O Bank Controller | Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection. |
| Dynamic Clock Enable for Primary Clock Nets | Each primary clock net can be dynamically disabled to save power. |
| Power Guard | Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources. |

For more details on the standby mode refer to TN1198, Power Estimation and Management for MachXO2 Devices.

## Power On Reset

MachXO2 devices have power-on reset circuitry to monitor $V_{CCINT}$ and $V_{CCIO}$ voltage levels during power-up and operation. At power-up, the POR circuitry monitors $V_{CCINT}$ and $V_{CCIO0}$ (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the $V_{PORUP}$ level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices), $V_{CCINT}$ is the same as the $V_{CC}$ supply voltage. For devices with voltage regulators (HC devices), $V_{CCINT}$ is regulated from the $V_{CC}$ supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time ($t_{REFRESH}$) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external $V_{CC}$ voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor $V_{CCINT}$ levels. If $V_{CCINT}$ drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the $V_{CCINT}$ and $V_{CCIO}$ voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the $V_{CC}$ supply dropping below $V_{CC}$ (min) they should not shut down the bandgap or POR circuit.

# MachXO2 Family Data Sheet DC and Switching Characteristics

March 2017 Data Sheet DS1035

## Absolute Maximum Ratings[1, 2, 3]

| | MachXO2 ZE/HE (1.2 V) | MachXO2 HC (2.5 V / 3.3 V) |
|---|---|---|
| Supply Voltage $V_{CC}$ | –0.5 V to 1.32 V | –0.5 V to 3.75 V |
| Output Supply Voltage $V_{CCIO}$ | –0.5 V to 3.75 V | –0.5 V to 3.75 V |
| I/O Tri-state Voltage Applied[4, 5] | –0.5 V to 3.75 V | –0.5 V to 3.75 V |
| Dedicated Input Voltage Applied[4] | –0.5 V to 3.75 V | –0.5 V to 3.75 V |
| Storage Temperature (Ambient) | –55 °C to 125 °C | –55 °C to 125 °C |
| Junction Temperature ($T_J$) | –40 °C to 125 °C | –40 °C to 125 °C |

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to ($V_{IHMAX}$ + 2) volts is permitted for a duration of <20 ns.
5. The dual function $I^2C$ pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.

## Recommended Operating Conditions[1]

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{CC}$[1] | Core Supply Voltage for 1.2 V Devices | 1.14 | 1.26 | V |
| | Core Supply Voltage for 2.5 V / 3.3 V Devices | 2.375 | 3.6 | V |
| $V_{CCIO}$[1, 2, 3] | I/O Driver Supply Voltage | 1.14 | 3.6 | V |
| $t_{JCOM}$ | Junction Temperature Commercial Operation | 0 | 85 | °C |
| $t_{JIND}$ | Junction Temperature Industrial Operation | –40 | 100 | °C |

1. Like power supplies must be tied together. For example, if $V_{CCIO}$ and $V_{CC}$ are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. $V_{CCIO}$ pins of unused I/O banks should be connected to the $V_{CC}$ power supply on boards.

## Power Supply Ramp Rates[1]

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{RAMP}$ | Power supply ramp rates for all power supplies. | 0.01 | — | 100 | V/ms |

1. Assumes monotonic ramp rates.

## BLVDS

The MachXO2 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

***Figure 3-2. BLVDS Multi-point Output Example***

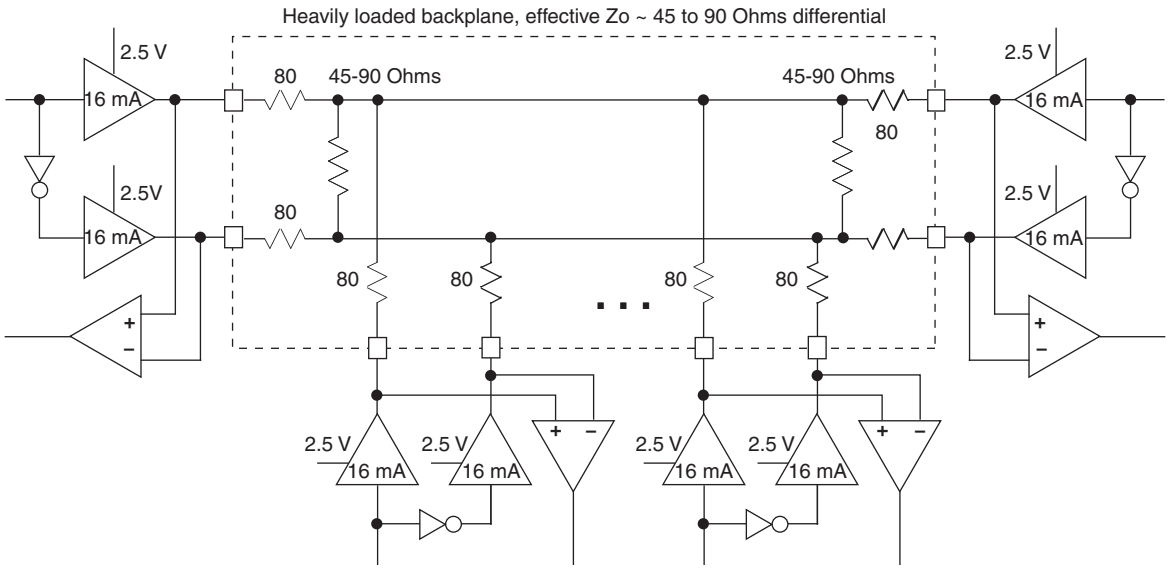



***Table 3-2. BLVDS DC Conditions[1]***

**Over Recommended Operating Conditions**

| Symbol | Description | Nominal | | Units |
|---|---|---|---|---|
| | | Zo = 45 | Zo = 90 | |
| $Z_{OUT}$ | Output impedance | 20 | 20 | Ohms |
| $R_S$ | Driver series resistance | 80 | 80 | Ohms |
| $R_{TLEFT}$ | Left end termination | 45 | 90 | Ohms |
| $R_{TRIGHT}$ | Right end termination | 45 | 90 | Ohms |
| $V_{OH}$ | Output high voltage | 1.376 | 1.480 | V |
| $V_{OL}$ | Output low voltage | 1.124 | 1.020 | V |
| $V_{OD}$ | Output differential voltage | 0.253 | 0.459 | V |
| $V_{CM}$ | Output common mode voltage | 1.250 | 1.250 | V |
| $I_{DC}$ | DC output current | 11.236 | 10.204 | mA |

1. For input buffer, see LVDS table.

## RSDS

The MachXO2 family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

***Figure 3-4. RSDS (Reduced Swing Differential Standard)***

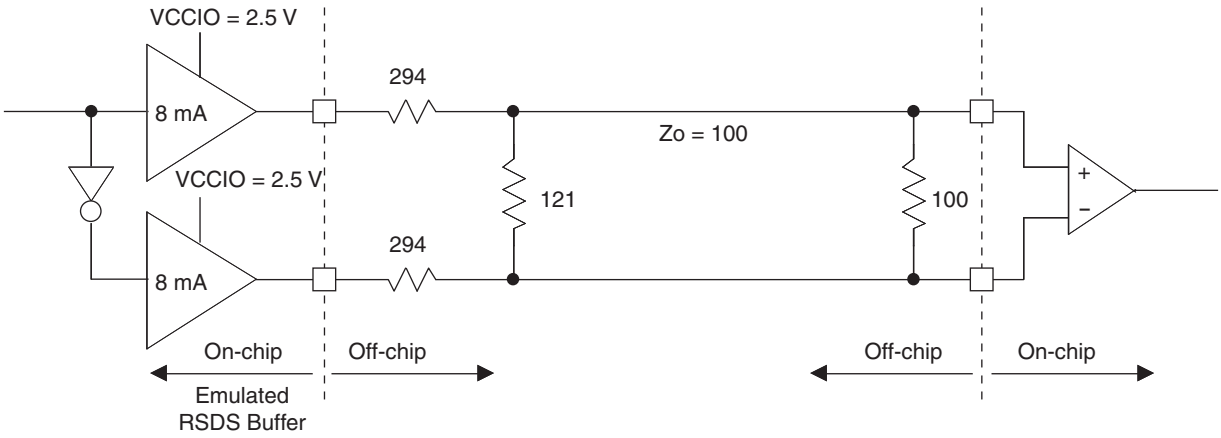



***Table 3-4. RSDS DC Conditions***

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ohms |
| $R_S$ | Driver series resistor | 294 | Ohms |
| $R_P$ | Driver parallel resistor | 121 | Ohms |
| $R_T$ | Receiver termination | 100 | Ohms |
| $V_{OH}$ | Output high voltage | 1.35 | V |
| $V_{OL}$ | Output low voltage | 1.15 | V |
| $V_{OD}$ | Output differential voltage | 0.20 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 101.5 | Ohms |
| $I_{DC}$ | DC output current | 3.66 | mA |

# Typical Building Block Function Performance – ZE Devices[1]

## Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

| Function | –3 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit decoder | 13.9 | ns |
| 4:1 MUX | 10.9 | ns |
| 16:1 MUX | 12.0 | ns |

## Register-to-Register Performance

| Function | –3 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16:1 MUX | 191 | MHz |
| 16-bit adder | 134 | MHz |
| 16-bit counter | 148 | MHz |
| 64-bit counter | 77 | MHz |
| **Embedded Memory Functions** | | |
| 1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers) | 90 | MHz |
| **Distributed Memory Functions** | | |
| 16x4 Pseudo-Dual Port RAM (one PFU) | 214 | MHz |

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

# Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

| Parameter | Description | Device | –6 | | –5 | | –4 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{HPLL}$ | Clock to Data Hold – PIO Input Register | MachXO2-1200HC-HE | 0.41 | — | 0.48 | — | 0.55 | — | ns |
| | | MachXO2-2000HC-HE | 0.42 | — | 0.49 | — | 0.56 | — | ns |
| | | MachXO2-4000HC-HE | 0.43 | — | 0.50 | — | 0.58 | — | ns |
| | | MachXO2-7000HC-HE | 0.46 | — | 0.54 | — | 0.62 | — | ns |
| $t_{SU\_DELPLL}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-1200HC-HE | 2.88 | — | 3.19 | — | 3.72 | — | ns |
| | | MachXO2-2000HC-HE | 2.87 | — | 3.18 | — | 3.70 | — | ns |
| | | MachXO2-4000HC-HE | 2.96 | — | 3.28 | — | 3.81 | — | ns |
| | | MachXO2-7000HC-HE | 3.05 | — | 3.35 | — | 3.87 | — | ns |
| $t_{H\_DELPLL}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-1200HC-HE | –0.83 | — | –0.83 | — | –0.83 | — | ns |
| | | MachXO2-2000HC-HE | –0.83 | — | –0.83 | — | –0.83 | — | ns |
| | | MachXO2-4000HC-HE | –0.87 | — | –0.87 | — | –0.87 | — | ns |
| | | MachXO2-7000HC-HE | –0.91 | — | –0.91 | — | –0.91 | — | ns |
| **Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 12]** | | | | | | | | | |
| $t_{DVA}$ | Input Data Valid After CLK | All MachXO2 devices, all sides | — | 0.317 | — | 0.344 | — | 0.368 | UI |
| $t_{DVE}$ | Input Data Hold After CLK | | 0.742 | — | 0.702 | — | 0.668 | — | UI |
| $f_{DATA}$ | DDRX1 Input Data Speed | | — | 300 | — | 250 | — | 208 | Mbps |
| $f_{DDRX1}$ | DDRX1 SCLK Frequency | | — | 150 | — | 125 | — | 104 | MHz |
| **Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 12]** | | | | | | | | | |
| $t_{SU}$ | Input Data Setup Before CLK | All MachXO2 devices, all sides | 0.566 | — | 0.560 | — | 0.538 | — | ns |
| $t_{HO}$ | Input Data Hold After CLK | | 0.778 | — | 0.879 | — | 1.090 | — | ns |
| $f_{DATA}$ | DDRX1 Input Data Speed | | — | 300 | — | 250 | — | 208 | Mbps |
| $f_{DDRX1}$ | DDRX1 SCLK Frequency | | — | 150 | — | 125 | — | 104 | MHz |
| **Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 12]** | | | | | | | | | |
| $t_{DVA}$ | Input Data Valid After CLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11] | — | 0.316 | — | 0.342 | — | 0.364 | UI |
| $t_{DVE}$ | Input Data Hold After CLK | | 0.710 | — | 0.675 | — | 0.679 | — | UI |
| $f_{DATA}$ | DDRX2 Serial Input Data Speed | | — | 664 | — | 554 | — | 462 | Mbps |
| $f_{DDRX2}$ | DDRX2 ECLK Frequency | | — | 332 | — | 277 | — | 231 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 166 | — | 139 | — | 116 | MHz |
| **Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 12]** | | | | | | | | | |
| $t_{SU}$ | Input Data Setup Before CLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11] | 0.233 | — | 0.219 | — | 0.198 | — | ns |
| $t_{HO}$ | Input Data Hold After CLK | | 0.287 | — | 0.287 | — | 0.344 | — | ns |
| $f_{DATA}$ | DDRX2 Serial Input Data Speed | | — | 664 | — | 554 | — | 462 | Mbps |
| $f_{DDRX2}$ | DDRX2 ECLK Frequency | | — | 332 | — | 277 | — | 231 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 166 | — | 139 | — | 116 | MHz |

| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{SU\_DEL}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-256ZE | 2.62 | — | 2.91 | — | 3.14 | — | ns |
| | | MachXO2-640ZE | 2.56 | — | 2.85 | — | 3.08 | — | ns |
| | | MachXO2-1200ZE | 2.30 | — | 2.57 | — | 2.79 | — | ns |
| | | MachXO2-2000ZE | 2.25 | — | 2.50 | — | 2.70 | — | ns |
| | | MachXO2-4000ZE | 2.39 | — | 2.60 | — | 2.76 | — | ns |
| | | MachXO2-7000ZE | 2.17 | — | 2.33 | — | 2.43 | — | ns |
| $t_{H\_DEL}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-256ZE | –0.44 | — | –0.44 | — | –0.44 | — | ns |
| | | MachXO2-640ZE | –0.43 | — | –0.43 | — | –0.43 | — | ns |
| | | MachXO2-1200ZE | –0.28 | — | –0.28 | — | –0.28 | — | ns |
| | | MachXO2-2000ZE | –0.31 | — | –0.31 | — | –0.31 | — | ns |
| | | MachXO2-4000ZE | –0.34 | — | –0.34 | — | –0.34 | — | ns |
| | | MachXO2-7000ZE | –0.21 | — | –0.21 | — | –0.21 | — | ns |
| $f_{MAX\_IO}$ | Clock Frequency of I/O and PFU Register | All MachXO2 devices | — | 150 | — | 125 | — | 104 | MHz |
| **General I/O Pin Parameters (Using Edge Clock without PLL)** | | | | | | | | | |
| $t_{COE}$ | Clock to Output – PIO Output Register | MachXO2-1200ZE | — | 11.10 | — | 11.51 | — | 11.91 | ns |
| | | MachXO2-2000ZE | — | 11.10 | — | 11.51 | — | 11.91 | ns |
| | | MachXO2-4000ZE | — | 10.89 | — | 11.28 | — | 11.67 | ns |
| | | MachXO2-7000ZE | — | 11.10 | — | 11.51 | — | 11.91 | ns |
| $t_{SUE}$ | Clock to Data Setup – PIO Input Register | MachXO2-1200ZE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-2000ZE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-4000ZE | –0.15 | — | –0.15 | — | –0.15 | — | ns |
| | | MachXO2-7000ZE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| $t_{HE}$ | Clock to Data Hold – PIO Input Register | MachXO2-1200ZE | 3.81 | — | 4.11 | — | 4.52 | — | ns |
| | | MachXO2-2000ZE | 3.81 | — | 4.11 | — | 4.52 | — | ns |
| | | MachXO2-4000ZE | 3.60 | — | 3.89 | — | 4.28 | — | ns |
| | | MachXO2-7000ZE | 3.81 | — | 4.11 | — | 4.52 | — | ns |
| $t_{SU\_DELE}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-1200ZE | 2.78 | — | 3.11 | — | 3.40 | — | ns |
| | | MachXO2-2000ZE | 2.78 | — | 3.11 | — | 3.40 | — | ns |
| | | MachXO2-4000ZE | 3.11 | — | 3.48 | — | 3.79 | — | ns |
| | | MachXO2-7000ZE | 2.94 | — | 3.30 | — | 3.60 | — | ns |
| $t_{H\_DELE}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-1200ZE | –0.29 | — | -0.29 | — | –0.29 | — | ns |
| | | MachXO2-2000ZE | –0.29 | — | -0.29 | — | –0.29 | — | ns |
| | | MachXO2-4000ZE | –0.46 | — | -0.46 | — | –0.46 | — | ns |
| | | MachXO2-7000ZE | –0.37 | — | -0.37 | — | –0.37 | — | ns |
| **General I/O Pin Parameters (Using Primary Clock with PLL)** | | | | | | | | | |
| $t_{COPLL}$ | Clock to Output – PIO Output Register | MachXO2-1200ZE | — | 7.95 | — | 8.07 | — | 8.19 | ns |
| | | MachXO2-2000ZE | — | 7.97 | — | 8.10 | — | 8.22 | ns |
| | | MachXO2-4000ZE | — | 7.98 | — | 8.10 | — | 8.23 | ns |
| | | MachXO2-7000ZE | — | 8.02 | — | 8.14 | — | 8.26 | ns |
| $t_{SUPLL}$ | Clock to Data Setup – PIO Input Register | MachXO2-1200ZE | 0.85 | — | 0.85 | — | 0.89 | — | ns |
| | | MachXO2-2000ZE | 0.84 | — | 0.84 | — | 0.86 | — | ns |
| | | MachXO2-4000ZE | 0.84 | — | 0.84 | — | 0.85 | — | ns |
| | | MachXO2-7000ZE | 0.83 | — | 0.83 | — | 0.81 | — | ns |

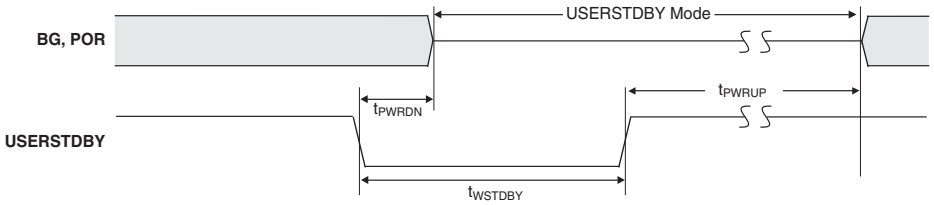
## MachXO2 Oscillator Output Frequency

| Symbol | Parameter | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|
| $f_{MAX}$ | Oscillator Output Frequency (Commercial Grade Devices, 0 to 85°C) | 125.685 | 133 | 140.315 | MHz |
| | Oscillator Output Frequency (Industrial Grade Devices, –40 °C to 100 °C) | 124.355 | 133 | 141.645 | MHz |
| $t_{DT}$ | Output Clock Duty Cycle | 43 | 50 | 57 | % |
| $t_{OPJIT}$[1] | Output Clock Period Jitter | 0.01 | 0.012 | 0.02 | UIPP |
| $t_{STABLEOSC}$ | STDBY Low to Oscillator Stable | 0.01 | 0.05 | 0.1 | µs |

1. Output Clock Period Jitter specified at 133 MHz. The values for lower frequencies will be smaller UIPP. The typical value for 133 MHz is 95 ps and for 2.08 MHz the typical value is 1.54 ns.

## MachXO2 Standby Mode Timing – HC/HE Devices

| Symbol | Parameter | Device | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PWRDN}$ | USERSTDBY High to Stop | All | — | — | 9 | ns |
| $t_{PWRUP}$ | USERSTDBY Low to Power Up | LCMXO2-256 | | — | | µs |
| | | LCMXO2-640 | | — | | µs |
| | | LCMXO2-640U | | — | | µs |
| | | LCMXO2-1200 | 20 | — | 50 | µs |
| | | LCMXO2-1200U | | — | | µs |
| | | LCMXO2-2000 | | — | | µs |
| | | LCMXO2-2000U | | — | | µs |
| | | LCMXO2-4000 | | — | | µs |
| | | LCMXO2-7000 | | — | | µs |
| $t_{WSTDBY}$ | USERSTDBY Pulse Width | All | 18 | — | — | ns |




## MachXO2 Standby Mode Timing – ZE Devices

| Symbol | Parameter | Device | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PWRDN}$ | USERSTDBY High to Stop | All | — | — | 13 | ns |
| $t_{PWRUP}$ | USERSTDBY Low to Power Up | LCMXO2-256 | | — | | µs |
| | | LCMXO2-640 | | — | | µs |
| | | LCMXO2-1200 | 20 | — | 50 | µs |
| | | LCMXO2-2000 | | — | | µs |
| | | LCMXO2-4000 | | — | | µs |
| | | LCMXO2-7000 | | — | | µs |
| $t_{WSTDBY}$ | USERSTDBY Pulse Width | All | 19 | — | — | ns |
| $t_{BNDGAPSTBL}$ | USERSTDBY High to Bandgap Stable | All | — | — | 15 | ns |

| | MachXO2-4000 | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 84 QFN | 132 csBGA | 144 TQFP | 184 csBGA | 256 caBGA | 256 ftBGA | 332 caBGA | 484 fpBGA |
| **General Purpose I/O per Bank** | | | | | | | | |
| Bank 0 | 27 | 25 | 27 | 37 | 50 | 50 | 68 | 70 |
| Bank 1 | 10 | 26 | 29 | 37 | 52 | 52 | 68 | 68 |
| Bank 2 | 22 | 28 | 29 | 39 | 52 | 52 | 70 | 72 |
| Bank 3 | 0 | 7 | 9 | 10 | 16 | 16 | 24 | 24 |
| Bank 4 | 9 | 8 | 10 | 12 | 16 | 16 | 16 | 16 |
| Bank 5 | 0 | 10 | 10 | 15 | 20 | 20 | 28 | 28 |
| Total General Purpose Single Ended I/O | 68 | 104 | 114 | 150 | 206 | 206 | 274 | 278 |
| | | | | | | | | |
| **Differential I/O per Bank** | | | | | | | | |
| Bank 0 | 13 | 13 | 14 | 18 | 25 | 25 | 34 | 35 |
| Bank 1 | 4 | 13 | 14 | 18 | 26 | 26 | 34 | 34 |
| Bank 2 | 11 | 14 | 14 | 19 | 26 | 26 | 35 | 36 |
| Bank 3 | 0 | 3 | 4 | 4 | 8 | 8 | 12 | 12 |
| Bank 4 | 4 | 4 | 5 | 6 | 8 | 8 | 8 | 8 |
| Bank 5 | 0 | 5 | 5 | 7 | 10 | 10 | 14 | 14 |
| Total General Purpose Differential I/O | 32 | 52 | 56 | 72 | 103 | 103 | 137 | 139 |
| | | | | | | | | |
| **Dual Function I/O** | 28 | 37 | 37 | 37 | 37 | 37 | 37 | 37 |
| **High-speed Differential I/O** | | | | | | | | |
| Bank 0 | 8 | 8 | 9 | 8 | 18 | 18 | 18 | 18 |
| **Gearboxes** | | | | | | | | |
| Number of 7:1 or 8:1 Output Gearbox Available (Bank 0) | 8 | 8 | 9 | 9 | 18 | 18 | 18 | 18 |
| Number of 7:1 or 8:1 Input Gearbox Available (Bank 2) | 11 | 14 | 14 | 12 | 18 | 18 | 18 | 18 |
| **DQS Groups** | | | | | | | | |
| Bank 1 | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | | | | | | | | |
| **VCCIO Pins** | | | | | | | | |
| Bank 0 | 3 | 3 | 3 | 3 | 4 | 4 | 4 | 10 |
| Bank 1 | 1 | 3 | 3 | 3 | 4 | 4 | 4 | 10 |
| Bank 2 | 2 | 3 | 3 | 3 | 4 | 4 | 4 | 10 |
| Bank 3 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 3 |
| Bank 4 | 1 | 1 | 1 | 1 | 2 | 2 | 1 | 4 |
| Bank 5 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 3 |
| | | | | | | | | |
| VCC | 4 | 4 | 4 | 4 | 8 | 8 | 8 | 12 |
| GND | 4 | 10 | 12 | 16 | 24 | 24 | 27 | 48 |
| NC | 1 | 1 | 1 | 1 | 1 | 1 | 5 | 105 |
| Reserved for configuration | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Total Count of Bonded Pins | 84 | 132 | 144 | 184 | 256 | 256 | 332 | 484 |

# MachXO2 Family Data Sheet Ordering Information



## MachXO2 Part Number Description

LCMXO2 – XXXX X X X – X XXXXXX X XX XX

**Device Family**
MachXO2 PLD

**Logic Capacity**
256 = 256 LUTs
640 = 640 LUTs
1200 = 1280 LUTs
2000 = 2112 LUTs
4000 = 4320 LUTs
7000 = 6864 LUTs

**I/O Count**
Blank = Standard Device
U = Ultra High I/O Device

**Power/Performance**
Z = Low Power
H = High Performance

**Supply Voltage**
C = 2.5 V / 3.3 V
E = 1.2 V

**Speed**
1 = Slowest
2
3 = Fastest
} Low Power

4 = Slowest
5
6 = Fastest
} High Performance

**Device Status**
Blank = Production Device
ES = Engineering Sample
R1 = Production Release 1 Device
1K = WLCSP Package, 1,000 parts per reel

**Shipping Method**
Blank = Trays
TR = Tape and Reel

**Grade**
C = Commercial
I = Industrial

**Package**
UWG25 = 25-Ball Halogen-Free WLCSP (0.4 mm Pitch)
SG32 = 32-Pin Halogen-Free QFN (0.5 mm Pitch)
SG48 = 48-Pin Halogen-Free QFN (0.5 mm Pitch)
UWG49 = 49-ball Halogen-Free WLCSP (0.4 mm Pitch)
UMG64 = 64-Ball Halogen-Free ucBGA (0.4 mm Pitch)
QN84 = 84-Pin Halogen-Free QFN (0.5 mm Pitch)
TG100 = 100-Pin Halogen-Free TQFP
TG144 = 144-Pin Halogen-Free TQFP
MG132 = 132-Ball Halogen-Free csBGA (0.5 mm Pitch)
MG184 = 184-Ball Halogen-Free csBGA (0.5 mm Pitch)
BG256 = 256-Ball Halogen-Free caBGA (0.8 mm Pitch)
FTG256 = 256-Ball Halogen-Free ftBGA (1.0 mm Pitch)
BG332 = 332-Ball Halogen-Free caBGA (0.8 mm Pitch)
FG484 = 484-Ball Halogen-Free fpBGA (1.0 mm Pitch)

* 48-pin QFN information is 'Advanced'.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000UHC-4FG484C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-2000UHC-5FG484C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-2000UHC-6FG484C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000HC-4QN84C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000HC-5QN84C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000HC-6QN84C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000HC-4MG132C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HC-5MG132C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HC-6MG132C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HC-4TG144C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HC-5TG144C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HC-6TG144C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HC-4BG256C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HC-5BG256C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HC-6BG256C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HC-4FTG256C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HC-5FTG256C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HC-6FTG256C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HC-4BG332C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HC-5BG332C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HC-6BG332C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HC-4FG484C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HC-5FG484C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HC-6FG484C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000HE-6BG332C | 4320 | 1.2 V | –6 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HE-4FG484C | 4320 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HE-5FG484C | 4320 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HE-6FG484C | 4320 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000HE-4TG144C | 6864 | 1.2 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000HE-5TG144C | 6864 | 1.2 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000HE-6TG144C | 6864 | 1.2 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000HE-4BG256C | 6864 | 1.2 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000HE-5BG256C | 6864 | 1.2 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000HE-6BG256C | 6864 | 1.2 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000HE-4FTG256C | 6864 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000HE-5FTG256C | 6864 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000HE-6FTG256C | 6864 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000HE-4BG332C | 6864 | 1.2 V | –4 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000HE-5BG332C | 6864 | 1.2 V | –5 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000HE-6BG332C | 6864 | 1.2 V | –6 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000HE-4FG484C | 6864 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000HE-5FG484C | 6864 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000HE-6FG484C | 6864 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000ZE-1UWG49ITR[1] | 2112 | 1.2 V | –1 | Halogen-Free WLCSP | 49 | IND |
| LCMXO2-2000ZE-1UWG49ITR50[3] | 2112 | 1.2 V | –1 | Halogen-Free WLCSP | 49 | IND |
| LCMXO2-2000ZE-1UWG49ITR1K[2] | 2112 | 1.2 V | –1 | Halogen-Free WLCSP | 49 | IND |
| LCMXO2-2000ZE-1TG100I | 2112 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-2000ZE-2TG100I | 2112 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-2000ZE-3TG100I | 2112 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-2000ZE-1MG132I | 2112 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-2000ZE-2MG132I | 2112 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-2000ZE-3MG132I | 2112 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-2000ZE-1TG144I | 2112 | 1.2 V | –1 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000ZE-2TG144I | 2112 | 1.2 V | –2 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000ZE-3TG144I | 2112 | 1.2 V | –3 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000ZE-1BG256I | 2112 | 1.2 V | –1 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-2000ZE-2BG256I | 2112 | 1.2 V | –2 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-2000ZE-3BG256I | 2112 | 1.2 V | –3 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-2000ZE-1FTG256I | 2112 | 1.2 V | –1 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-2000ZE-2FTG256I | 2112 | 1.2 V | –2 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-2000ZE-3FTG256I | 2112 | 1.2 V | –3 | Halogen-Free ftBGA | 256 | IND |

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

| Date | Version | Section | Change Summary |
|---|---|---|---|
| December 2014 | 2.9 | Introduction | Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide.<br>— Removed XO2-4000U data.<br>— Removed 400-ball ftBGA.<br>— Removed 25-ball WLCSP value for XO2-2000U. |
| | | DC and Switching Characteristics | Updated the Recommended Operating Conditions section. Adjusted Max. values for $V_{CC}$ and $V_{CCIO}$. |
| | | | Updated the sysIO Recommended Operating Conditions section. Adjusted Max. values for LVCMOS 3.3, LVTTL, PCI, LVDS33 and LVPECL. |
| | | Pinout Information | Updated the Pinout Information Summary section. Removed MachXO2-4000U. |
| | | Ordering Information | Updated the MachXO2 Part Number Description section. Removed BG400 package. |
| | | | Updated the High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers. |
| | | | Updated the High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers. |
| November 2014 | 2.8 | Introduction | Updated the Features section.<br>— Revised I/Os under Flexible Logic Architecture.<br>— Revised standby power under Ultra Low Power Devices.<br>— Revise input frequency range under Flexible On-Chip Clocking. |
| | | | Updated Table 1-1, MachXO2 Family Selection Guide.<br>— Added XO2-4000U data.<br>— Removed HE and ZE device options for XO2-4000.<br>— Added 400-ball ftBGA. |
| | | Pinout Information | Updated the Pinout Information Summary section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400. |
| | | Ordering Information | Updated the MachXO2 Part Number Description section. Added BG400 package. |
| | | | Updated the Ordering Information section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400 part numbers. |
| October 2014 | 2.7 | Ordering Information | Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Fixed typo in LCMXO2-2000ZE-1UWG49ITR part number package. |
| | | Architecture | Updated the Supported Standards section. Added MIPI information to Table 2-12. Supported Input Standards and Table 2-13. Supported Output Standards. |
| | | DC and Switching Characteristics | Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition. |
| | | | Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition. |
| | | | Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values. |
| July 2014 | 2.6 | DC and Switching Characteristics | Updated sysIO Single-Ended DC Electrical Characteristics[1, 2] section. Updated footnote 4. |
| | | | Updated Register-to-Register Performance section. Updated footnote. |
| | | Ordering Information | Updated UW49 package to UWG49 in MachXO2 Part Number Description. |
| | | | Updated LCMXO2-2000ZE-1UWG49CTR package in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging. |