

Welcome to E-XFL.COM

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	32
Number of Logic Elements/Cells	256
Total RAM Bits	-
Number of I/O	55
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-256hc-6mg132i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag "hard" control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysl/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2-640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO2 devices provide commonly used hardened functions such as SPI controller, I²C controller and timer/ counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I²C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

PFU Blocks

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.



Figure 2-4. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

- WCK is CLK
 WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

 Table 2-2. Slice Signal Descriptions

Function	Туре	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multi-purpose input
Input	Control signal	CE	Clock enable
Input	Control signal	LSR	Local set/reset
Input	Control signal	CLK	System clock
Input	Inter-PFU signal	FCIN	Fast carry in ¹
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Fast carry out ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.



Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-14 shows the output register block on the left, top and bottom edges.

Figure 2-14. MachXO2 Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)



Right Edge

The output register block on the right edge is a superset of the output register on left, top and bottom edges of the device. In addition to supporting SDR and Generic DDR modes, the output register blocks for PIOs on the right edge include additional logic to support DDR-memory interfaces. Operation of this block is similar to that of the output register block on other edges.

In DDR memory mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the DQSW90 signal is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-15 shows the output register block on the right edge.



Figure 2-17. Output Gearbox



More information on the output gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.



For more details on these embedded functions, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

User Flash Memory (UFM)

MachXO2-640/U and higher density devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I²C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

Standby Mode and Power Saving Options

MachXO2 devices are available in three options for maximum flexibility: ZE, HC and HE devices. The ZE devices have ultra low static and dynamic power consumption. These devices use a 1.2 V core voltage that further reduces power consumption. The HC and HE devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the HE devices operate at 1.2 V V_{CC}.

MachXO2 devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO2 devices support an ultra low power Stand-by mode. While most of these features are available in all three device types, these features are mainly intended for use with MachXO2 ZE devices to manage power consumption.

In the stand-by mode the MachXO2 devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I²C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned "off" or go into a low power consumption state to save power when the device enters this state. Note that the MachXO2 devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.



Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe V_{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1198, Power Estimation and Management for MachXO2 Devices.

Power On Reset

MachXO2 devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the V_{PORUP} level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices), V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators (HC devices), V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time (t_{REFRESH}) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tristate. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min) they should not shut down the bandgap or POR circuit.



Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I²C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

- 1. Internal Flash Download
- 2. JTAG
- 3. Standard Serial Peripheral Interface (Master SPI mode) interface to boot PROM memory
- 4. System microprocessor to drive a serial slave SPI port (SSPI mode)
- 5. Standard I²C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, MachXO2 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.



When implementing background programming of the on-chip Flash, care must be taken for the operation of the PLL. For devices that have two PLLs (XO2-2000U, -4000 and -7000), the system must put the RPLL (Right-side PLL) in reset state during the background Flash programming. More detailed description can be found in TN1204, MachXO2 Programming and Configuration Usage Guide.

Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO2 devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile Flash memory spaces. The device can be in one of two modes:

- 1. Unlocked Readback of the SRAM configuration and non-volatile Flash memory spaces is allowed.
- 2. Permanently Locked The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Dual Boot

MachXO2 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the on-chip Flash. The golden image MUST reside in an external SPI Flash. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1206, MachXO2 Soft Error Detection Usage Guide.

TraceID

Each MachXO2 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I²C, or JTAG interfaces.

Density Shifting

The MachXO2 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO2 migration files.



			-6 -5 -		-4				
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
		MachXO2-1200HC-HE	0.41		0.48		0.55	—	ns
1	Clock to Data Hold – PIO Input	MachXO2-2000HC-HE	0.42		0.49		0.56	—	ns
THPLL	Register	MachXO2-4000HC-HE	0.43		0.50		0.58	—	ns
		MachXO2-7000HC-HE		—	ns				
		MachXO2-1200HC-HE	2.88		3.19		3.72	—	ns
	Clock to Data Setup – PIO	MachXO2-2000HC-HE	2.87		3.18		3.70	—	ns
Delay	MachXO2-4000HC-HE	2.96		3.28		3.81	—	ns	
	,	MachXO2-7000HC-HE	3.05		3.35		3.87	—	ns
		MachXO2-1200HC-HE	-0.83		-0.83		-0.83	—	ns
	Clock to Data Hold – PIO Input	MachXO2-2000HC-HE	-0.83		-0.83		-0.83	—	ns
^I H_DELPLL	Register with Input Data Delay	MachXO2-4000HC-HE	-0.87		-0.87		-0.87	—	ns
		MachXO2-7000HC-HE	-0.91	—	-0.91	—	-0.91	—	ns
Generic DDF	RX1 Inputs with Clock and Data	Aligned at Pin Using PC	LK Pin	for Cloc	k Input -	GDDR	(1_RX.S	CLK.Ali	gned ^{9, 12}
t _{DVA}	Input Data Valid After CLK			0.317	—	0.344	—	0.368	UI
t _{DVE}	Input Data Hold After CLK	All MachXO2 devices,	0.742	—	0.702	—	0.668	—	UI
f _{DATA}	DDRX1 Input Data Speed	all sides	_	300	—	250	—	208	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency			150	—	125	—	104	MHz
Generic DDF	X1 Inputs with Clock and Data C	Centered at Pin Using PC	LK Pin f	or Clock	Input –	GDDRX	1_RX.SC	LK.Cen	tered ^{9, 12}
t _{SU}	Input Data Setup Before CLK		0.566		0.560		0.538	—	ns
t _{HO}	Input Data Hold After CLK	All MachXO2 devices,	0.778		0.879		1.090	—	ns
f _{DATA}	DDRX1 Input Data Speed	all sides		300		250		208	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency			150		125		104	MHz
Generic DDF	RX2 Inputs with Clock and Data	Aligned at Pin Using PC	LK Pin f	for Clock	k Input –	GDDR	(2_RX.E	CLK.Ali	gned ^{9, 12}
t _{DVA}	Input Data Valid After CLK		—	0.316		0.342		0.364	UI
t _{DVE}	Input Data Hold After CLK	MachXO2-640U,	0.710		0.675		0.679	—	UI
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	664	_	554	_	462	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency	bottom side only ¹¹		332		277		231	MHz
f _{SCLK}	SCLK Frequency			166		139	—	116	MHz
Generic DDF	X2 Inputs with Clock and Data C	Centered at Pin Using PC	LK Pin f	or Clock	Input –	GDDRX	2_RX.EC	LK.Cen	tered ^{9, 12}
t _{SU}	Input Data Setup Before CLK		0.233		0.219		0.198	—	ns
t _{HO}	Input Data Hold After CLK	MachXO2-640U	0.287	—	0.287	—	0.344	—	ns
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	664	_	554	_	462	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency	bottom side only ¹¹	—	332	—	277	—	231	MHz
f _{SCLK}	SCLK Frequency	1	—	166		139		116	MHz



MachXO2 External Switching Characteristics – ZE Devices^{1, 2, 3, 4, 5, 6, 7}

			-	-3	-	-2	-	1	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Clocks			1						
Primary Cloo	cks								
f _{MAX_PRI} ⁸	Frequency for Primary Clock Tree	All MachXO2 devices	_	150	_	125	_	104	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	1.00	_	1.20	_	1.40	_	ns
		MachXO2-256ZE	_	1250	—	1272		1296	ps
		MachXO2-640ZE		1161		1183		1206	ps
	Primary Clock Skew Within a	MachXO2-1200ZE	_	1213		1267		1322	ps
^t SKEW_PRI	Device	MachXO2-2000ZE		1204		1250		1296	ps
		MachXO2-4000ZE		1195		1233		1269	ps
		MachXO2-7000ZE		1243		1268		1296	ps
Edge Clock									
f _{MAX_EDGE} ⁸	Frequency for Edge Clock	MachXO2-1200 and larger devices	_	210	_	175	_	146	MHz
Pin-LUT-Pin	Propagation Delay		1	1	1	1	1	1	
t _{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	_	9.35	_	9.78	_	10.21	ns
General I/O	Pin Parameters (Using Primary	Clock without PLL)	I	I	I	I	I		
		MachXO2-256ZE		10.46	—	10.86	—	11.25	ns
		MachXO2-640ZE	_	10.52	—	10.92		11.32	ns
	Clock to Output – PIO Output	MachXO2-1200ZE	_	11.24		11.68		12.12	ns
^t CO	Register	MachXO2-2000ZE	_	11.27		11.71		12.16	ns
		MachXO2-4000ZE	_	11.28		11.78		12.28	ns
		MachXO2-7000ZE		11.22		11.76		12.30	ns
		MachXO2-256ZE	-0.21		-0.21		-0.21		ns
		MachXO2-640ZE	-0.22		-0.22		-0.22	—	ns
	Clock to Data Setup – PIO	MachXO2-1200ZE	-0.25	—	-0.25		-0.25	_	ns
t _{SU}	Input Register	MachXO2-2000ZE	-0.27		-0.27		-0.27	_	ns
		MachXO2-4000ZE	-0.31		-0.31		-0.31	_	ns
		MachXO2-7000ZE	-0.33		-0.33		-0.33	_	ns
		MachXO2-256ZE	3.96	—	4.25	—	4.65	—	ns
		MachXO2-640ZE	4.01		4.31		4.71	_	ns
+	Clock to Data Hold – PIO Input	MachXO2-1200ZE	3.95		4.29	_	4.73	—	ns
Ч	Register	MachXO2-2000ZE	3.94		4.29		4.74	_	ns
		MachXO2-4000ZE	3.96		4.36		4.87	_	ns
		MachXO2-7000ZE	3.93	_	4.37	_	4.91		ns

Over Recommended Operating Conditions



Figure 3-9. GDDR71 Video Timing Waveforms



Figure 3-10. Receiver GDDR71_RX. Waveforms



Figure 3-11. Transmitter GDDR71_TX. Waveforms







		M	achXO2-120	MachXO2-1200U		
	100 TQFP	132 csBGA	144 TQFP	25 WLCSP	32 QFN ¹	256 ftBGA
General Purpose I/O per Bank						
Bank 0	18	25	27	11	9	50
Bank 1	21	26	26	0	2	52
Bank 2	20	28	28	7	9	52
Bank 3	20	25	26	0	2	16
Bank 4	0	0	0	0	0	16
Bank 5	0	0	0	0	0	20
Total General Purpose Single Ended I/O	79	104	107	18	22	206
Differential I/O per Bank						
Bank 0	9	13	14	5	4	25
Bank 1	10	13	13	0	1	26
Bank 2	10	14	14	2	4	26
Bank 3	10	12	13	0	1	8
Bank 4	0	0	0	0	0	8
Bank 5	0	0	0	0	0	10
Total General Purpose Differential I/O	39	52	54	7	10	103
Dual Function I/O	31	33	33	18	22	33
High-speed Differential I/O						1
Bank 0	4	7	7	0	0	14
Gearboxes						1
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	4	7	7	0	0	14
Number of 7:1 or 8:1 Input Gearbox Avail- able (Bank 2)	5	7	7	0	2	14
DQS Groups						
Bank 1	1	2	2	0	0	2
VCCIO Pins	1	1				1
Bank 0	2	3	3	1	2	4
Bank 1	2	3	3	0	1	4
Bank 2	2	3	3	1	2	4
Bank 3	3	3	3	0	1	1
Bank 4	0	0	0	0	0	2
Bank 5	0	0	0	0	0	1
	I			гг		Γ
VCC	2	4	4	2	2	8
GND	8	10	12	2	2	24
NC	1	1	8	0	0	1
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	100	132	144	25	32	256

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1TG100C	2112	1.2 V	-1	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-2TG100C	2112	1.2 V	-2	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-3TG100C	2112	1.2 V	-3	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-1MG132C	2112	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-2MG132C	2112	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-3MG132C	2112	1.2 V	-3	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-1TG144C	2112	1.2 V	-1	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-2TG144C	2112	1.2 V	-2	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-3TG144C	2112	1.2 V	-3	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-1BG256C	2112	1.2 V	-1	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-2BG256C	2112	1.2 V	-2	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-3BG256C	2112	1.2 V	-3	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-1FTG256C	2112	1.2 V	-1	Halogen-Free ftBGA	256	COM
LCMXO2-2000ZE-2FTG256C	2112	1.2 V	-2	Halogen-Free ftBGA	256	COM
LCMXO2-2000ZE-3FTG256C	2112	1.2 V	-3	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000ZE-1QN84C	4320	1.2 V	-1	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-2QN84C	4320	1.2 V	-2	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-3QN84C	4320	1.2 V	-3	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-1MG132C	4320	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-2MG132C	4320	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-3MG132C	4320	1.2 V	-3	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-1TG144C	4320	1.2 V	-1	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-2TG144C	4320	1.2 V	-2	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-3TG144C	4320	1.2 V	-3	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-1BG256C	4320	1.2 V	-1	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-2BG256C	4320	1.2 V	-2	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-3BG256C	4320	1.2 V	-3	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-1FTG256C	4320	1.2 V	-1	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-2FTG256C	4320	1.2 V	-2	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-3FTG256C	4320	1.2 V	-3	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-1BG332C	4320	1.2 V	-1	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-2BG332C	4320	1.2 V	-2	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-3BG332C	4320	1.2 V	-3	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-1FG484C	4320	1.2 V	-1	Halogen-Free fpBGA	484	COM
LCMXO2-4000ZE-2FG484C	4320	1.2 V	-2	Halogen-Free fpBGA	484	COM
LCMXO2-4000ZE-3FG484C	4320	1.2 V	-3	Halogen-Free fpBGA	484	COM



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144C	6864	1.2 V	-1	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-2TG144C	6864	1.2 V	-2	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-3TG144C	6864	1.2 V	-3	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-1BG256C	6864	1.2 V	-1	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-2BG256C	6864	1.2 V	-2	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-3BG256C	6864	1.2 V	-3	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-1FTG256C	6864	1.2 V	-1	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-2FTG256C	6864	1.2 V	-2	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-3FTG256C	6864	1.2 V	-3	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-1BG332C	6864	1.2 V	-1	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-2BG332C	6864	1.2 V	-2	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-3BG332C	6864	1.2 V	-3	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-1FG484C	6864	1.2 V	-1	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-2FG484C	6864	1.2 V	-2	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-3FG484C	6864	1.2 V	-3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100CR11	1280	1.2 V	-1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100CR11	1280	1.2 V	-2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100CR11	1280	1.2 V	-3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132CR1 ¹	1280	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132CR11	1280	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132CR1 ¹	1280	1.2 V	-3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144CR1 ¹	1280	1.2 V	-1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144CR1 ¹	1280	1.2 V	-2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144CR1 ¹	1280	1.2 V	-3	Halogen-Free TQFP	144	COM

1. Specifications for the "LCMXO2-1200ZE-speed package CR1" are the same as the "LCMXO2-1200ZE-speed package C" devices respectively, except as specified in the R1 Device Specifications section of this data sheet.



High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32C	256	2.5 V / 3.3 V	-4	Halogen-Free QFN	32	COM
LCMXO2-256HC-5SG32C	256	2.5 V / 3.3 V	-5	Halogen-Free QFN	32	COM
LCMXO2-256HC-6SG32C	256	2.5 V / 3.3 V	-6	Halogen-Free QFN	32	COM
LCMXO2-256HC-4SG48C	256	2.5 V / 3.3 V	-4	Halogen-Free QFN	48	COM
LCMXO2-256HC-5SG48C	256	2.5 V / 3.3 V	-5	Halogen-Free QFN	48	COM
LCMXO2-256HC-6SG48C	256	2.5 V / 3.3 V	-6	Halogen-Free QFN	48	COM
LCMXO2-256HC-4UMG64C	256	2.5 V / 3.3 V	-4	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-5UMG64C	256	2.5 V / 3.3 V	-5	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-6UMG64C	256	2.5 V / 3.3 V	-6	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-4TG100C	256	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-256HC-5TG100C	256	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-256HC-6TG100C	256	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-256HC-4MG132C	256	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-256HC-5MG132C	256	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-256HC-6MG132C	256	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48C	640	2.5 V / 3.3 V	-4	Halogen-Free QFN	48	COM
LCMXO2-640HC-5SG48C	640	2.5 V / 3.3 V	-5	Halogen-Free QFN	48	COM
LCMXO2-640HC-6SG48C	640	2.5 V / 3.3 V	-6	Halogen-Free QFN	48	COM
LCMXO2-640HC-4TG100C	640	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-640HC-5TG100C	640	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-640HC-6TG100C	640	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-640HC-4MG132C	640	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-640HC-5MG132C	640	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-640HC-6MG132C	640	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144C	640	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-5TG144C	640	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-6TG144C	640	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	COM



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32I	1280	2.5 V / 3.3 V	-4	Halogen-Free QFN	32	IND
LCMXO2-1200HC-5SG32I	1280	2.5 V / 3.3 V	-5	Halogen-Free QFN	32	IND
LCMXO2-1200HC-6SG32I	1280	2.5 V / 3.3 V	-6	Halogen-Free QFN	32	IND
LCMXO2-1200HC-4TG100I	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100I	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100I	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132I	1280	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132I	1280	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132I	1280	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144I	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144I	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144I	1280	2.5 V/ 3.3 V	-6	Halogen-Free TQFP	144	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256I	1280	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-5FTG256I	1280	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-6FTG256I	1280	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100I	2112	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-5TG100I	2112	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-6TG100I	2112	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-4MG132I	2112	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-5MG132I	2112	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-6MG132I	2112	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-4TG144I	2112	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-5TG144I	2112	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-6TG144I	2112	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-4BG256I	2112	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-5BG256I	2112	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-6BG256I	2112	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-4FTG256I	2112	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-5FTG256I	2112	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-6FTG256I	2112	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484I	2112	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-5FG484I	2112	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-6FG484I	2112	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	IND



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84I	4320	2.5 V / 3.3 V	-4	Halogen-Free QFN	84	IND
LCMXO2-4000HC-5QN84I	4320	2.5 V / 3.3 V	-5	Halogen-Free QFN	84	IND
LCMXO2-4000HC-6QN84I	4320	2.5 V / 3.3 V	-6	Halogen-Free QFN	84	IND
LCMXO2-4000HC-4TG144I	4320	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-5TG144I	4320	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-6TG144I	4320	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-4MG132I	4320	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-5MG132I	4320	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-6MG132I	4320	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-4BG256I	4320	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-5BG256I	4320	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-6BG256I	4320	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-4FTG256I	4320	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-5FTG256I	4320	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-6FTG256I	4320	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-4BG332I	4320	2.5 V / 3.3 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-5BG332I	4320	2.5 V / 3.3 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-6BG332I	4320	2.5 V / 3.3 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-4FG484I	4320	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-5FG484I	4320	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-6FG484I	4320	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144I	6864	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-5TG144I	6864	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-6TG144I	6864	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-4BG256I	6864	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-5BG256I	6864	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-6BG256I	6864	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-4FTG256I	6864	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-5FTG256I	6864	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-6FTG256I	6864	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-4BG332I	6864	2.5 V / 3.3 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-5BG332I	6864	2.5 V / 3.3 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-6BG332I	6864	2.5 V / 3.3 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-4FG400I	6864	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-5FG400I	6864	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-6FG400I	6864	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-4FG484I	6864	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-5FG484I	6864	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-6FG484I	6864	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	IND



High Performance Industrial Grade Devices Without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100I	2112	1.2 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-5TG100I	2112	1.2 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-6TG100I	2112	1.2 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-4MG132I	2112	1.2 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-5MG132I	2112	1.2 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-6MG132I	2112	1.2 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-4TG144I	2112	1.2 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-5TG144I	2112	1.2 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-6TG144I	2112	1.2 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-4BG256I	2112	1.2 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-5BG256I	2112	1.2 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-6BG256I	2112	1.2 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-4FTG256I	2112	1.2 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-5FTG256I	2112	1.2 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-6FTG256I	2112	1.2 V	-6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484I	2112	1.2 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-5FG484I	2112	1.2 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-6FG484I	2112	1.2 V	-6	Halogen-Free fpBGA	484	IND



MachXO2 Family Data Sheet Revision History

March 2017

Data Sheet DS1035

Date	Version	Section	Change Summary
March 2017	3.3	DC and Switching Characteristics	Updated the Absolute Maximum Ratings section. Added standards.
			Updated the sysIO Recommended Operating Conditions section. Added standards.
			Updated the sysIO Single-Ended DC Electrical Characteristics sec- tion. Added standards.
			Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA} . The parameter descriptions were also modified.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA} . The parameter descriptions were also modified.
			Updated the sysCONFIG Port Timing Specifications section. Corrected the t_{INITL} units from ns to μ s.
		Pinout Information	Updated the Signal Descriptions section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals.
			Updated the Pinout Information Summary section. Added footnote to MachXO2-1200 32 QFN.
		Ordering Information	Updated the MachXO2 Part Number Description section. Corrected the MG184, BG256, FTG256 package information. Added "(0.8 mm Pitch)" to BG332.
			Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. — Updated LCMXO2-1200ZE-1UWG25ITR50 footnote. — Corrected footnote numbering typo. — Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2- 2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s.

^{© 2016} Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Date	Version	Section	Change Summary
December 2014	2.9	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Removed XO2-4000U data. — Removed 400-ball ftBGA. — Removed 25-ball WLCSP value for XO2-2000U.
		DC and Switching Characteristics	Updated the Recommended Operating Conditions section. Adjusted Max. values for V_{CC} and V_{CCIO}
			Updated the sysIO Recommended Operating Conditions section. Adjusted Max. values for LVCMOS 3.3, LVTTL, PCI, LVDS33 and LVPECL.
		Pinout Information	Updated the Pinout Information Summary section. Removed MachXO2-4000U.
		Ordering Information	Updated the MachXO2 Part Number Description section. Removed BG400 package.
			Updated the High-Performance Commercial Grade Devices with Volt- age Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
			Updated the High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
November 2014	lovember 2014 2.8	Introduction	Updated the Features section. — Revised I/Os under Flexible Logic Architecture. — Revised standby power under Ultra Low Power Devices. — Revise input frequency range under Flexible On-Chip Clocking.
			Updated Table 1-1, MachXO2 Family Selection Guide. — Added XO2-4000U data. — Removed HE and ZE device options for XO2-4000. — Added 400-ball ftBGA.
		Pinout Information	Updated the Pinout Information Summary section. Added MachXO2- 4000U caBGA400 and MachXO2-7000 caBGA400.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added BG400 package.
			Updated the Ordering Information section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400 part numbers.
October 2014	2.7	Ordering Information	Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Fixed typo in LCMXO2-2000ZE- 1UWG49ITR part number package.
		Architecture	Updated the Supported Standards section. Added MIPI information to Table 2-12. Supported Input Standards and Table 2-13. Supported Output Standards.
		DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition.
			Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition.
			Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.
July 2014	2.6	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics ^{1, 2} section. Updated footnote 4.
			Updated Register-to-Register Performance section. Updated foot- note.
		Ordering Information	Updated UW49 package to UWG49 in MachXO2 Part Number Description.
			Updated LCMXO2-2000ZE-1UWG49CTR package in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging.