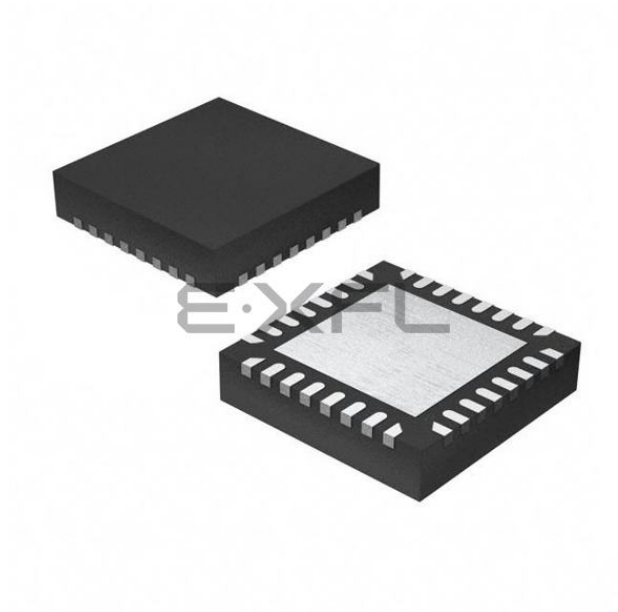
# Lattice Semiconductor Corporation - LCMXO2-256HC-6SG32C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

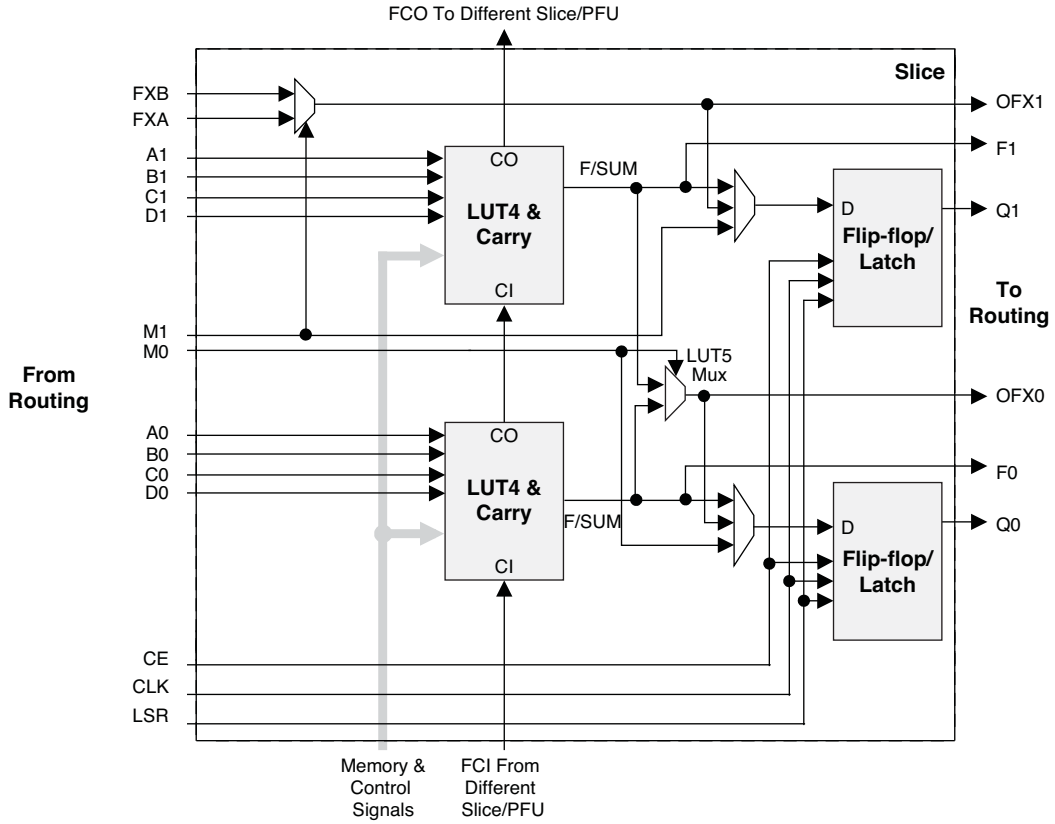
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 32 |
| Number of Logic Elements/Cells | 256 |
| Total RAM Bits | - |
| Number of I/O | 21 |
| Number of Gates | - |
| Voltage - Supply | 2.375V ~ 3.465V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 32-UFQFN Exposed Pad |
| Supplier Device Package | 32-QFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-256hc-6sg32c |

*Figure 2-4. Slice Diagram*




For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

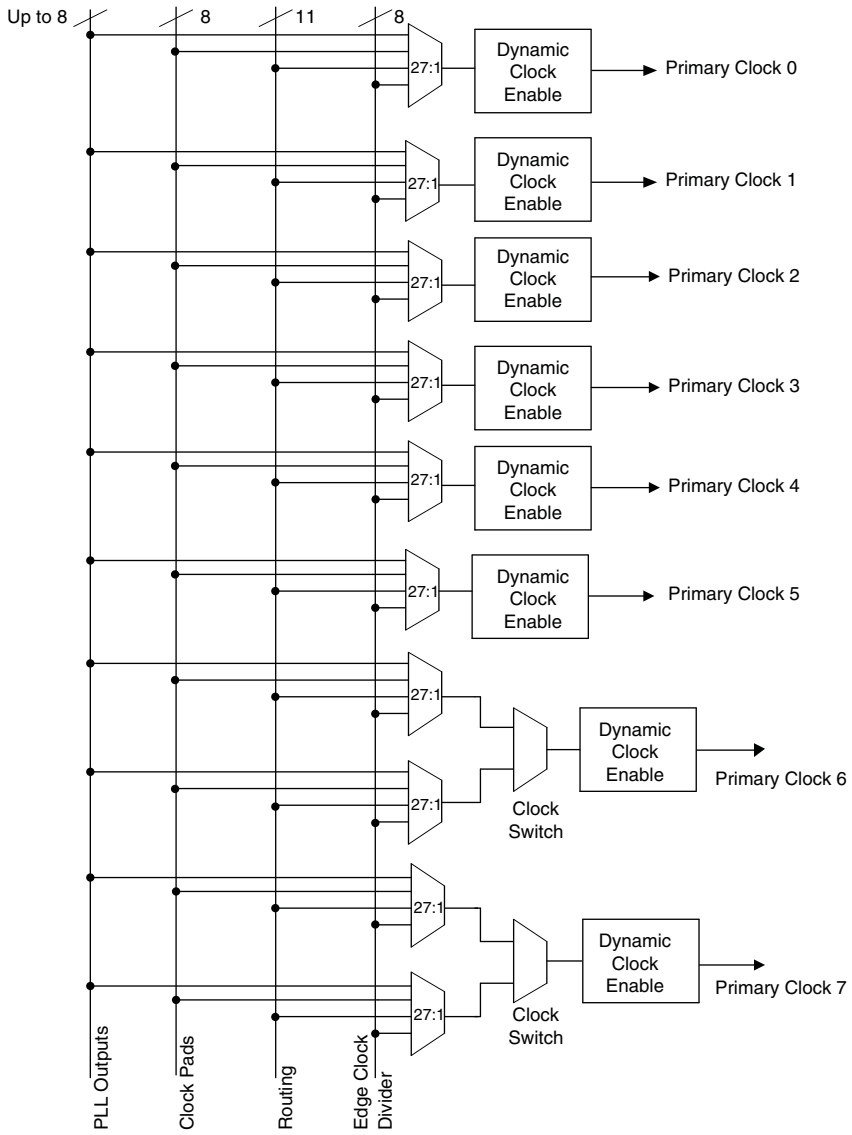
- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

*Table 2-2. Slice Signal Descriptions*

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0/M1 | Multi-purpose input |
| Input | Control signal | CE | Clock enable |
| Input | Control signal | LSR | Local set/reset |
| Input | Control signal | CLK | System clock |
| Input | Inter-PFU signal | FCIN | Fast carry in[1] |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register outputs |
| Output | Data signals | OFX0 | Output of a LUT5 MUX |
| Output | Data signals | OFX1 | Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice |
| Output | Inter-PFU signal | FCO | Fast carry out[1] |

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

*Figure 2-5. Primary Clocks for MachXO2 Devices*




Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO2 External Switching Characteristics table.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.

3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

**FIFO Configuration**

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

***Table 2-7. Programmable FIFO Flag Ranges***

| Flag Name | Programming Range |
|---|---|
| Full (FF) | 1 to max (up to $2^N$-1) |
| Almost Full (AF) | 1 to Full-1 |
| Almost Empty (AE) | 1 to Full-1 |
| Empty (EF) | 0 |

N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

**Memory Core Reset**

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

More information on the input gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.

## Output Gearbox

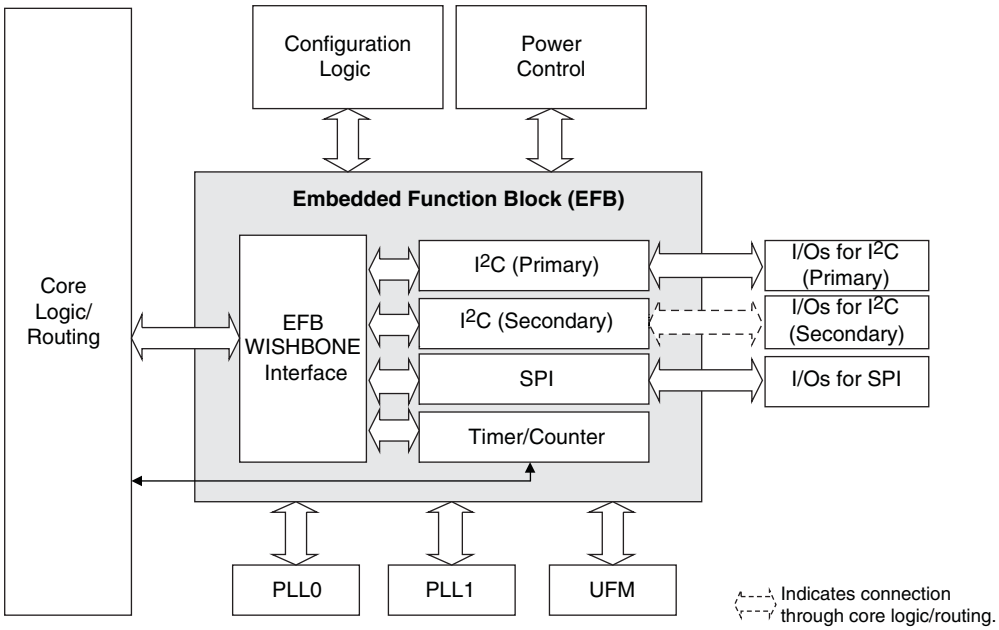
Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

***Table 2-10. Output Gearbox Signal List***

| Name | I/O Type | Description |
|---|---|---|
| Q | Output | High-speed data output |
| D[7:0] | Input | Low-speed data from device core |
| Video TX(7:1): D[6:0] | | |
| GDDRX4(8:1): D[7:0] | | |
| GDDRX2(4:1)(IOL-A): D[3:0] | | |
| GDDRX2(4:1)(IOL-C): D[7:4] | | |
| SCLK | Input | Slow-speed system clock |
| ECLK [1:0] | Input | High-speed edge clock |
| RST | Input | Reset |

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-17 shows the output gearbox block diagram.

*Figure 2-20. Embedded Function Block Interface*




## Hardened I²C IP Core

Every MachXO2 device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I²C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface

## Power-On-Reset Voltage Levels[1, 2, 3, 4, 5]

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{PORUP}$ | Power-On-Reset ramp up trip point (band gap based circuit monitoring $V_{CCINT}$ and $V_{CCIO0}$) | 0.9 | — | 1.06 | V |
| $V_{PORUPEXT}$ | Power-On-Reset ramp up trip point (band gap based circuit monitoring external $V_{CC}$ power supply) | 1.5 | — | 2.1 | V |
| $V_{PORDNBG}$ | Power-On-Reset ramp down trip point (band gap based circuit monitoring $V_{CCINT}$) | 0.75 | — | 0.93 | V |
| $V_{PORDNBGEXT}$ | Power-On-Reset ramp down trip point (band gap based circuit monitoring $V_{CC}$) | 0.98 | — | 1.33 | V |
| $V_{PORDNSRAM}$ | Power-On-Reset ramp down trip point (SRAM based circuit monitoring $V_{CCINT}$) | — | 0.6 | — | V |
| $V_{PORDNSRAMEXT}$ | Power-On-Reset ramp down trip point (SRAM based circuit monitoring $V_{CC}$) | — | 0.96 | — | V |

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators $V_{CCINT}$ is the same as the $V_{CC}$ supply voltage. For devices with voltage regulators, $V_{CCINT}$ is regulated from the $V_{CC}$ supply voltage.
3. Note that $V_{PORUP}$ (min.) and $V_{PORDNBG}$ (max.) are in different process corners. For any given process corner $V_{PORDNBG}$ (max.) is always 12.0 mV below $V_{PORUP}$ (min.).
4. $V_{PORUPEXT}$ is for HC devices only. In these devices a separate POR circuit monitors the external $V_{CC}$ power supply.
5. $V_{CCIO0}$ does not have a Power-On-Reset ramp down trip point. $V_{CCIO0}$ must remain within the Recommended Operating Conditions to ensure proper operation.

## Programming/Erase Specifications

| Symbol | Parameter | Min. | Max.[1] | Units |
|---|---|---|---|---|
| $N_{PROGCYC}$ | Flash Programming cycles per $t_{RETENTION}$ | — | 10,000 | Cycles |
| | Flash functional programming cycles | — | 100,000 | |
| $t_{RETENTION}$ | Data retention at 100 °C junction temperature | 10 | — | Years |
| | Data retention at 85 °C junction temperature | 20 | — | |

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

## Hot Socketing Specifications[1, 2, 3]

| Symbol | Parameter | Condition | Max. | Units |
|---|---|---|---|---|
| $I_{DK}$ | Input or I/O leakage Current | $0 < V_{IN} < V_{IH}$ (MAX) | +/–1000 | µA |

1. Insensitive to sequence of $V_{CC}$ and $V_{CCIO}$. However, assumes monotonic rise/fall rates for $V_{CC}$ and $V_{CCIO}$.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).
3. $I_{DK}$ is additive to $I_{PU}$, $I_{PD}$ or $I_{BH}$.

## ESD Performance

Please refer to the MachXO2 Product Family Qualification Summary for complete qualification data, including ESD performance.

## Static Supply Current – ZE Devices[1, 2, 3, 6]

| Symbol | Parameter | Device | Typ.[4] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LCMXO2-256ZE | 18 | µA |
| | | LCMXO2-640ZE | 28 | µA |
| | | LCMXO2-1200ZE | 56 | µA |
| | | LCMXO2-2000ZE | 80 | µA |
| | | LCMXO2-4000ZE | 124 | µA |
| | | LCMXO2-7000ZE | 189 | µA |
| $I_{CCIO}$ | Bank Power Supply[5] $V_{CCIO}$ = 2.5 V | All devices | 1 | µA |

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at $V_{CCIO}$ or GND, on-chip oscillator is off, on-chip PLL is off. To estimate the impact of turning each of these items on, please refer to the following table or for more detail with your specific design use the Power Calculator tool.
3. Frequency = 0 MHz.
4. $T_J$ = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

## Static Power Consumption Contribution of Different Components – ZE Devices

The table below can be used for approximating static power consumption. For a more accurate power analysis for your design please use the Power Calculator tool.

| Symbol | Parameter | Typ. | Units |
|---|---|---|---|
| $I_{DCBG}$ | Bandgap DC power contribution | 101 | µA |
| $I_{DCPOR}$ | POR DC power contribution | 38 | µA |
| $I_{DCIOBANKCONTROLLER}$ | DC power contribution per I/O bank controller | 143 | µA |

## RSDS

The MachXO2 family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

***Figure 3-4. RSDS (Reduced Swing Differential Standard)***

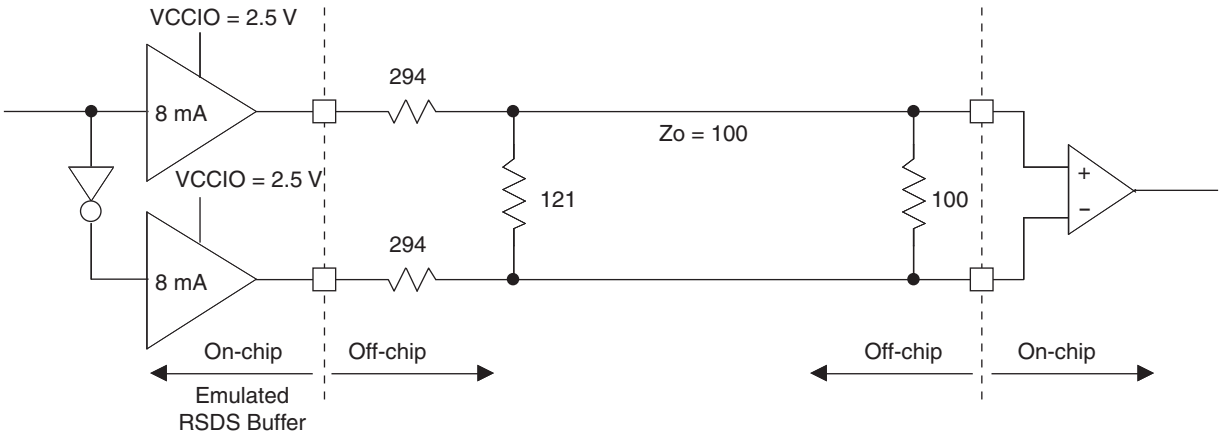



***Table 3-4. RSDS DC Conditions***

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ohms |
| $R_S$ | Driver series resistor | 294 | Ohms |
| $R_P$ | Driver parallel resistor | 121 | Ohms |
| $R_T$ | Receiver termination | 100 | Ohms |
| $V_{OH}$ | Output high voltage | 1.35 | V |
| $V_{OL}$ | Output low voltage | 1.15 | V |
| $V_{OD}$ | Output differential voltage | 0.20 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 101.5 | Ohms |
| $I_{DC}$ | DC output current | 3.66 | mA |

# Typical Building Block Function Performance – HC/HE Devices[1]

## Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

| Function | -6 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit decoder | 8.9 | ns |
| 4:1 MUX | 7.5 | ns |
| 16:1 MUX | 8.3 | ns |

## Register-to-Register Performance

| Function | -6 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16:1 MUX | 412 | MHz |
| 16-bit adder | 297 | MHz |
| 16-bit counter | 324 | MHz |
| 64-bit counter | 161 | MHz |
| **Embedded Memory Functions** | | |
| 1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers) | 183 | MHz |
| **Distributed Memory Functions** | | |
| 16x4 Pseudo-Dual Port RAM (one PFU) | 500 | MHz |

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

# Typical Building Block Function Performance – ZE Devices[1]

## Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

| Function | –3 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit decoder | 13.9 | ns |
| 4:1 MUX | 10.9 | ns |
| 16:1 MUX | 12.0 | ns |

## Register-to-Register Performance

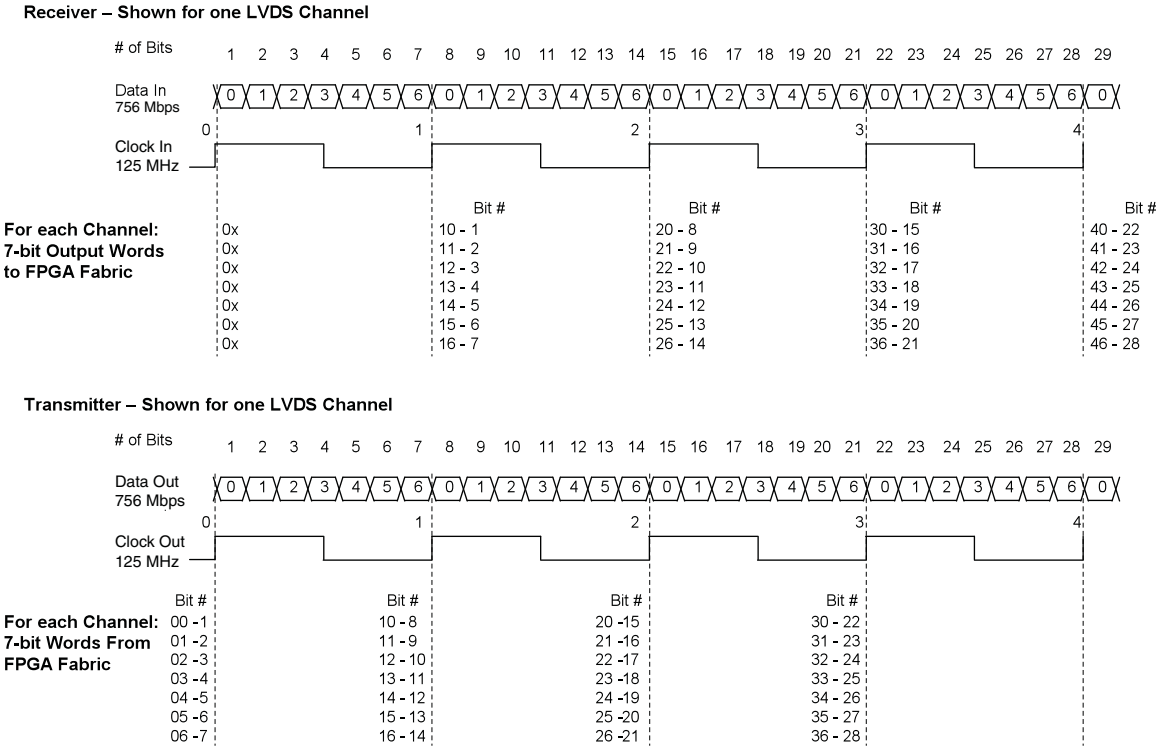
| Function | –3 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16:1 MUX | 191 | MHz |
| 16-bit adder | 134 | MHz |
| 16-bit counter | 148 | MHz |
| 64-bit counter | 77 | MHz |
| **Embedded Memory Functions** | | |
| 1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers) | 90 | MHz |
| **Distributed Memory Functions** | | |
| 16x4 Pseudo-Dual Port RAM (one PFU) | 214 | MHz |

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

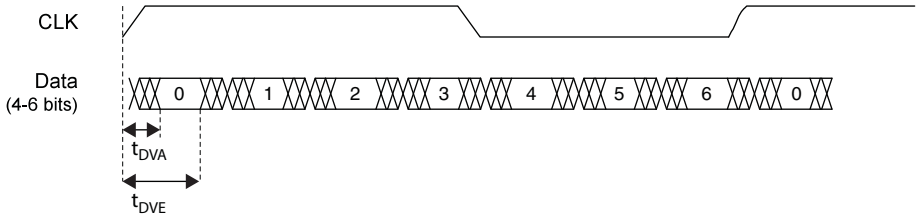
# Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

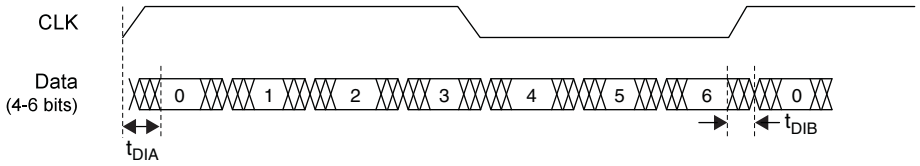
### Figure 3-9. GDDR71 Video Timing Waveforms




### Figure 3-10. Receiver GDDR71_RX. Waveforms




### Figure 3-11. Transmitter GDDR71_TX. Waveforms

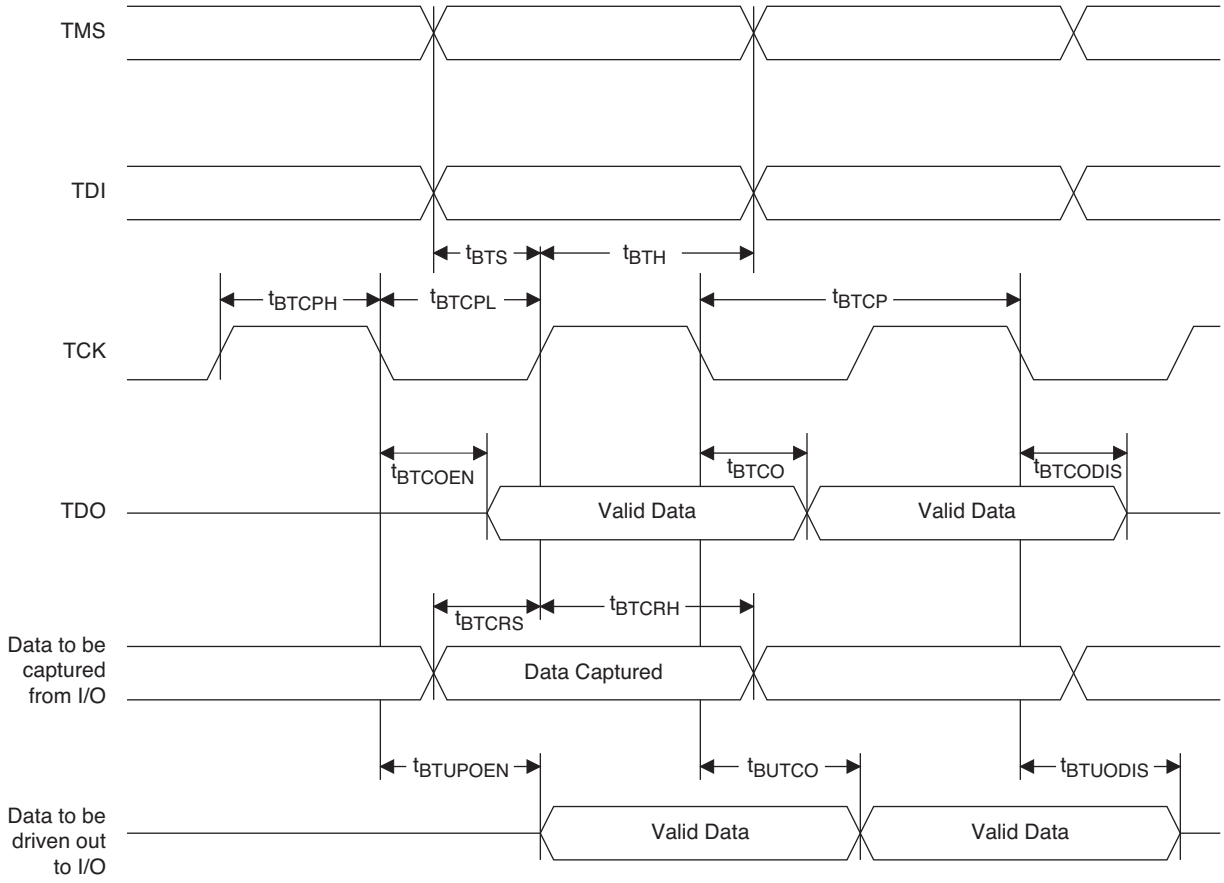


## sysCLOCK PLL Timing

**Over Recommended Operating Conditions**

| Parameter | Descriptions | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $f_{IN}$ | Input Clock Frequency (CLKI, CLKFB) | | 7 | 400 | MHz |
| $f_{OUT}$ | Output Clock Frequency (CLKOP, CLKOS, CLKOS2) | | 1.5625 | 400 | MHz |
| $f_{OUT2}$ | Output Frequency (CLKOS3 cascaded from CLKOS2) | | 0.0122 | 400 | MHz |
| $f_{VCO}$ | PLL VCO Frequency | | 200 | 800 | MHz |
| $f_{PFD}$ | Phase Detector Input Frequency | | 7 | 400 | MHz |
| **AC Characteristics** | | | | | |
| $t_{DT}$ | Output Clock Duty Cycle | Without duty trim selected[3] | 45 | 55 | % |
| $t_{DT\_TRIM}$[7] | Edge Duty Trim Accuracy | | –75 | 75 | % |
| $t_{PH}$[4] | Output Phase Accuracy | | –6 | 6 | % |
| $t_{OPJIT}$[1, 8] | Output Clock Period Jitter | $f_{OUT}$ > 100 MHz | — | 150 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.007 | UIPP |
| | Output Clock Cycle-to-cycle Jitter | $f_{OUT}$ > 100 MHz | — | 180 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.009 | UIPP |
| | Output Clock Phase Jitter | $f_{PFD}$ > 100 MHz | — | 160 | ps p-p |
| | | $f_{PFD}$ < 100 MHz | — | 0.011 | UIPP |
| | Output Clock Period Jitter (Fractional-N) | $f_{OUT}$ > 100 MHz | — | 230 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.12 | UIPP |
| | Output Clock Cycle-to-cycle Jitter (Fractional-N) | $f_{OUT}$ > 100 MHz | — | 230 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.12 | UIPP |
| $t_{SPO}$ | Static Phase Offset | Divider ratio = integer | –120 | 120 | ps |
| $t_W$ | Output Clock Pulse Width | At 90% or 10%[3] | 0.9 | — | ns |
| $t_{LOCK}$[2, 5] | PLL Lock-in Time | | — | 15 | ms |
| $t_{UNLOCK}$ | PLL Unlock Time | | — | 50 | ns |
| $t_{IPJIT}$[6] | Input Clock Period Jitter | $f_{PFD} \geq 20$ MHz | — | 1,000 | ps p-p |
| | | $f_{PFD}$ < 20 MHz | — | 0.02 | UIPP |
| $t_{HI}$ | Input Clock High Time | 90% to 90% | 0.5 | — | ns |
| $t_{LO}$ | Input Clock Low Time | 10% to 10% | 0.5 | — | ns |
| $t_{STABLE}$[5] | STANDBY High to PLL Stable | | — | 15 | ms |
| $t_{RST}$ | RST/RESETM Pulse Width | | 1 | — | ns |
| $t_{RSTREC}$ | RST Recovery Time | | 1 | — | ns |
| $t_{RST\_DIV}$ | RESETC/D Pulse Width | | 10 | — | ns |
| $t_{RSTREC\_DIV}$ | RESETC/D Recovery Time | | 1 | — | ns |
| $t_{ROTATE-SETUP}$ | PHASESTEP Setup Time | | 10 | — | ns |

*Figure 3-12. JTAG Port Timing Waveforms*



| | MachXO2-4000 | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 84 QFN | 132 csBGA | 144 TQFP | 184 csBGA | 256 caBGA | 256 ftBGA | 332 caBGA | 484 fpBGA |
| **General Purpose I/O per Bank** | | | | | | | | |
| Bank 0 | 27 | 25 | 27 | 37 | 50 | 50 | 68 | 70 |
| Bank 1 | 10 | 26 | 29 | 37 | 52 | 52 | 68 | 68 |
| Bank 2 | 22 | 28 | 29 | 39 | 52 | 52 | 70 | 72 |
| Bank 3 | 0 | 7 | 9 | 10 | 16 | 16 | 24 | 24 |
| Bank 4 | 9 | 8 | 10 | 12 | 16 | 16 | 16 | 16 |
| Bank 5 | 0 | 10 | 10 | 15 | 20 | 20 | 28 | 28 |
| Total General Purpose Single Ended I/O | 68 | 104 | 114 | 150 | 206 | 206 | 274 | 278 |
| | | | | | | | | |
| **Differential I/O per Bank** | | | | | | | | |
| Bank 0 | 13 | 13 | 14 | 18 | 25 | 25 | 34 | 35 |
| Bank 1 | 4 | 13 | 14 | 18 | 26 | 26 | 34 | 34 |
| Bank 2 | 11 | 14 | 14 | 19 | 26 | 26 | 35 | 36 |
| Bank 3 | 0 | 3 | 4 | 4 | 8 | 8 | 12 | 12 |
| Bank 4 | 4 | 4 | 5 | 6 | 8 | 8 | 8 | 8 |
| Bank 5 | 0 | 5 | 5 | 7 | 10 | 10 | 14 | 14 |
| Total General Purpose Differential I/O | 32 | 52 | 56 | 72 | 103 | 103 | 137 | 139 |
| | | | | | | | | |
| **Dual Function I/O** | 28 | 37 | 37 | 37 | 37 | 37 | 37 | 37 |
| **High-speed Differential I/O** | | | | | | | | |
| Bank 0 | 8 | 8 | 9 | 8 | 18 | 18 | 18 | 18 |
| **Gearboxes** | | | | | | | | |
| Number of 7:1 or 8:1 Output Gearbox Available (Bank 0) | 8 | 8 | 9 | 9 | 18 | 18 | 18 | 18 |
| Number of 7:1 or 8:1 Input Gearbox Available (Bank 2) | 11 | 14 | 14 | 12 | 18 | 18 | 18 | 18 |
| **DQS Groups** | | | | | | | | |
| Bank 1 | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | | | | | | | | |
| **VCCIO Pins** | | | | | | | | |
| Bank 0 | 3 | 3 | 3 | 3 | 4 | 4 | 4 | 10 |
| Bank 1 | 1 | 3 | 3 | 3 | 4 | 4 | 4 | 10 |
| Bank 2 | 2 | 3 | 3 | 3 | 4 | 4 | 4 | 10 |
| Bank 3 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 3 |
| Bank 4 | 1 | 1 | 1 | 1 | 2 | 2 | 1 | 4 |
| Bank 5 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 3 |
| | | | | | | | | |
| VCC | 4 | 4 | 4 | 4 | 8 | 8 | 8 | 12 |
| GND | 4 | 10 | 12 | 16 | 24 | 24 | 27 | 48 |
| NC | 1 | 1 | 1 | 1 | 1 | 1 | 5 | 105 |
| Reserved for configuration | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Total Count of Bonded Pins | 84 | 132 | 144 | 184 | 256 | 256 | 332 | 484 |

## For Further Information

For further information regarding logic signal connections for various packages please refer to the MachXO2 Device Pinout Files.

## Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Users must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

### For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1198, Power Estimation and Management for MachXO2 Devices
- The Power Calculator tool is included with the Lattice design tools, or as a standalone download from www.latticesemi.com/software

## Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-256ZE-1SG32C | 256 | 1.2 V | –1 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256ZE-2SG32C | 256 | 1.2 V | –2 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256ZE-3SG32C | 256 | 1.2 V | –3 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256ZE-1UMG64C | 256 | 1.2 V | –1 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256ZE-2UMG64C | 256 | 1.2 V | –2 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256ZE-3UMG64C | 256 | 1.2 V | –3 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256ZE-1TG100C | 256 | 1.2 V | –1 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256ZE-2TG100C | 256 | 1.2 V | –2 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256ZE-3TG100C | 256 | 1.2 V | –3 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256ZE-1MG132C | 256 | 1.2 V | –1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-256ZE-2MG132C | 256 | 1.2 V | –2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-256ZE-3MG132C | 256 | 1.2 V | –3 | Halogen-Free csBGA | 132 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640ZE-1TG100C | 640 | 1.2 V | –1 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640ZE-2TG100C | 640 | 1.2 V | –2 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640ZE-3TG100C | 640 | 1.2 V | –3 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640ZE-1MG132C | 640 | 1.2 V | –1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-640ZE-2MG132C | 640 | 1.2 V | –2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-640ZE-3MG132C | 640 | 1.2 V | –3 | Halogen-Free csBGA | 132 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-1200ZE-1SG32C | 1280 | 1.2 V | –1 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200ZE-2SG32C | 1280 | 1.2 V | –2 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200ZE-3SG32C | 1280 | 1.2 V | –3 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200ZE-1TG100C | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200ZE-2TG100C | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200ZE-3TG100C | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200ZE-1MG132C | 1280 | 1.2 V | –1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-2MG132C | 1280 | 1.2 V | –2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-3MG132C | 1280 | 1.2 V | –3 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-1TG144C | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200ZE-2TG144C | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200ZE-3TG144C | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 144 | COM |

## High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-256HC-4SG32C | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256HC-5SG32C | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256HC-6SG32C | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256HC-4SG48C | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 48 | COM |
| LCMXO2-256HC-5SG48C | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 48 | COM |
| LCMXO2-256HC-6SG48C | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 48 | COM |
| LCMXO2-256HC-4UMG64C | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256HC-5UMG64C | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256HC-6UMG64C | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256HC-4TG100C | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256HC-5TG100C | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256HC-6TG100C | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256HC-4MG132C | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-256HC-5MG132C | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-256HC-6MG132C | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640HC-4SG48C | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 48 | COM |
| LCMXO2-640HC-5SG48C | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 48 | COM |
| LCMXO2-640HC-6SG48C | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 48 | COM |
| LCMXO2-640HC-4TG100C | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640HC-5TG100C | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640HC-6TG100C | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640HC-4MG132C | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-640HC-5MG132C | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-640HC-6MG132C | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640UHC-4TG144C | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-640UHC-5TG144C | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-640UHC-6TG144C | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |

# MachXO2 Family Data Sheet Revision History

**March 2017** **Data Sheet DS1035**

| Date | Version | Section | Change Summary |
|---|---|---|---|
| March 2017 | 3.3 | DC and Switching Characteristics | Updated the Absolute Maximum Ratings section.<br>Added standards. |
| | | | Updated the sysIO Recommended Operating Conditions section.<br>Added standards. |
| | | | Updated the sysIO Single-Ended DC Electrical Characteristics section. Added standards. |
| | | | Updated the MachXO2 External Switching Characteristics – HC/HE Devices section.<br>Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the $D_{VB}$ and the $D_{VA}$ parameters were changed to $D_{IB}$ and $D_{IA}$. The parameter descriptions were also modified. |
| | | | Updated the MachXO2 External Switching Characteristics – ZE Devices section.<br>Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the $D_{VB}$ and the $D_{VA}$ parameters were changed to $D_{IB}$ and $D_{IA}$. The parameter descriptions were also modified. |
| | | | Updated the sysCONFIG Port Timing Specifications section.<br>Corrected the $t_{INITL}$ units from ns to µs. |
| | | Pinout Information | Updated the Signal Descriptions section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals. |
| | | | Updated the Pinout Information Summary section. Added footnote to MachXO2-1200 32 QFN. |
| | | Ordering Information | Updated the MachXO2 Part Number Description section. Corrected the MG184, BG256, FTG256 package information. Added “(0.8 mm Pitch)” to BG332. |
| | | | Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section.<br>— Updated LCMXO2-1200ZE-1UWG25ITR50 footnote.<br>— Corrected footnote numbering typo.<br>— Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2-2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s. |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| December 2014 | 2.9 | Introduction | Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide.<br>— Removed XO2-4000U data.<br>— Removed 400-ball ftBGA.<br>— Removed 25-ball WLCSP value for XO2-2000U. |
| | | DC and Switching Characteristics | Updated the Recommended Operating Conditions section. Adjusted Max. values for $V_{CC}$ and $V_{CCIO}$. |
| | | | Updated the sysIO Recommended Operating Conditions section. Adjusted Max. values for LVCMOS 3.3, LVTTL, PCI, LVDS33 and LVPECL. |
| | | Pinout Information | Updated the Pinout Information Summary section. Removed MachXO2-4000U. |
| | | Ordering Information | Updated the MachXO2 Part Number Description section. Removed BG400 package. |
| | | | Updated the High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers. |
| | | | Updated the High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers. |
| November 2014 | 2.8 | Introduction | Updated the Features section.<br>— Revised I/Os under Flexible Logic Architecture.<br>— Revised standby power under Ultra Low Power Devices.<br>— Revise input frequency range under Flexible On-Chip Clocking. |
| | | | Updated Table 1-1, MachXO2 Family Selection Guide.<br>— Added XO2-4000U data.<br>— Removed HE and ZE device options for XO2-4000.<br>— Added 400-ball ftBGA. |
| | | Pinout Information | Updated the Pinout Information Summary section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400. |
| | | Ordering Information | Updated the MachXO2 Part Number Description section. Added BG400 package. |
| | | | Updated the Ordering Information section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400 part numbers. |
| October 2014 | 2.7 | Ordering Information | Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Fixed typo in LCMXO2-2000ZE-1UWG49ITR part number package. |
| | | Architecture | Updated the Supported Standards section. Added MIPI information to Table 2-12. Supported Input Standards and Table 2-13. Supported Output Standards. |
| | | DC and Switching Characteristics | Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition. |
| | | | Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition. |
| | | | Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values. |
| July 2014 | 2.6 | DC and Switching Characteristics | Updated sysIO Single-Ended DC Electrical Characteristics[1, 2] section. Updated footnote 4. |
| | | | Updated Register-to-Register Performance section. Updated footnote. |
| | | Ordering Information | Updated UW49 package to UWG49 in MachXO2 Part Number Description. |
| | | | Updated LCMXO2-2000ZE-1UWG49CTR package in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging. |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| February 2012 | 01.7 | All | Updated document with new corporate logo. |
| | 01.6 | — | Data sheet status changed from preliminary to final. |
| | | Introduction | MachXO2 Family Selection Guide table – Removed references to 49-ball WLCSP. |
| | | DC and Switching Characteristics | Updated Flash Download Time table. |
| | | | Modified Storage Temperature in the Absolute Maximum Ratings section. |
| | | | Updated $I_{DK}$ max in Hot Socket Specifications table. |
| | | | Modified Static Supply Current tables for ZE and HC/HE devices. |
| | | | Updated Power Supply Ramp Rates table. |
| | | | Updated Programming and Erase Supply Current tables. |
| | | | Updated data in the External Switching Characteristics table. |
| | | | Corrected Absolute Maximum Ratings for Dedicated Input Voltage Applied for LCMXO2 HC. |
| | | | DC Electrical Characteristics table – Minor corrections to conditions for $I_{IL}$, $I_{IH}$. |
| | | Pinout Information | Removed references to 49-ball WLCSP. |
| | | | Signal Descriptions table – Updated description for GND, VCC, and VCCIOx. |
| | | | Updated Pin Information Summary table – Number of VCCIOs, GNDs, VCCs, and Total Count of Bonded Pins for MachXO2-256, 640, and 640U and Dual Function I/O for MachXO2-4000 332caBGA. |
| | | Ordering Information | Removed references to 49-ball WLCSP |
| August 2011 | 01.5 | DC and Switching Characteristics | Updated ESD information. |
| | | Ordering Information | Updated footnote for ordering WLCSP devices. |
| | 01.4 | Architecture | Updated information in Clock/Control Distribution Network and sysCLOCK Phase Locked Loops (PLLs). |
| | | DC and Switching Characteristics | Updated $I_{IL}$ and $I_{IH}$ conditions in the DC Electrical Characteristics table. |
| | | Pinout Information | Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables. |
| | | | Updated Pin Information Summary table: Dual Function I/O, DQS Groups Bank 1, Total General Purpose Single-Ended I/O, Differential I/O Per Bank, Total Count of Bonded Pins, Gearboxes.<br><br>Added column of data for MachXO2-2000 49 WLCSP. |
| | | Ordering Information | Updated R1 Device Specifications text section with information on migration from MachXO2-1200-R1 to Standard (non-R1) devices. |
| | | | Corrected Supply Voltage typo for part numbers: LCMX02-2000UHE-4FG484I, LCMX02-2000UHE-5FG484I, LCMX02-2000UHE-6FG484I. |
| | | | Added footnote for WLCSP package parts. |
| | | Supplemental Information | Removed reference to Stand-alone Power Calculator for MachXO2 Devices. Added reference to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices. |