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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

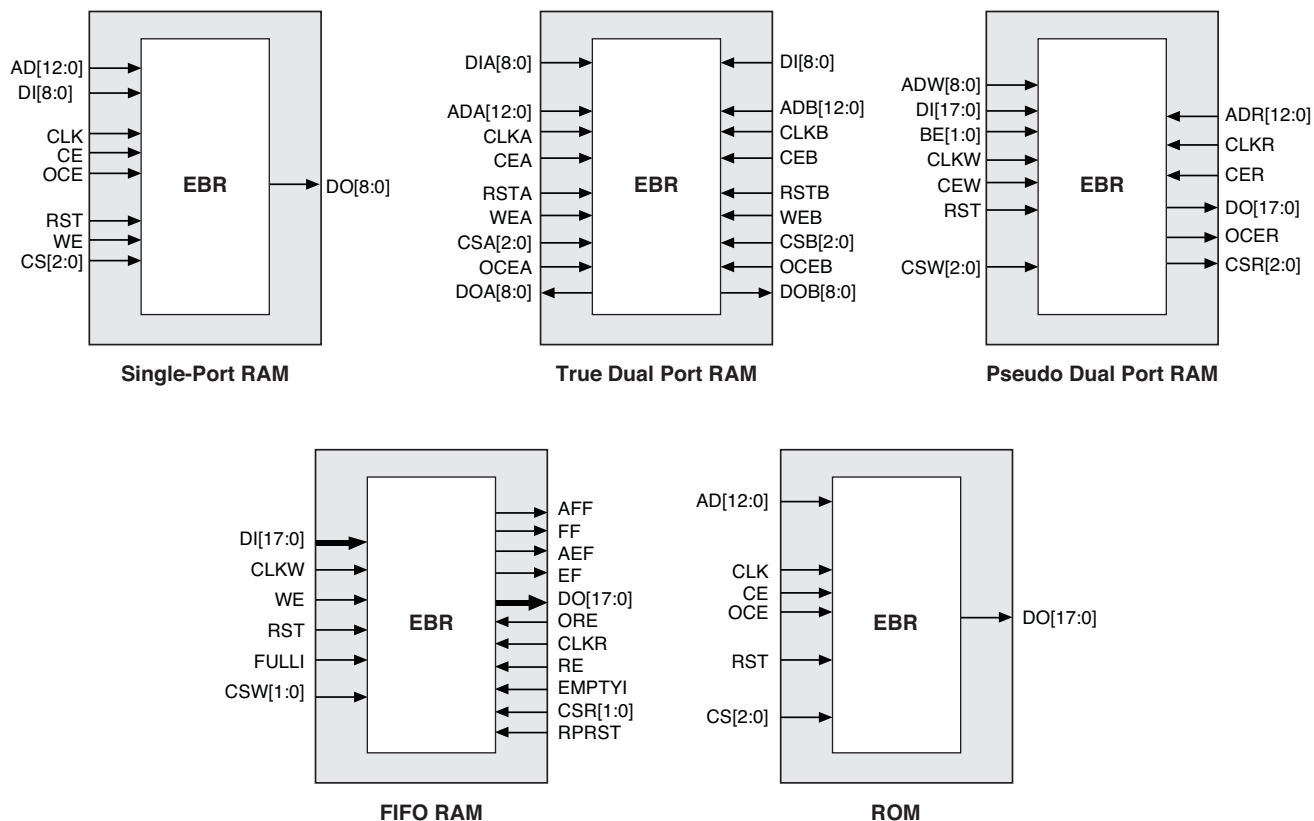
## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Active
Number of LABs/CLBs	32
Number of Logic Elements/Cells	256
Total RAM Bits	-
Number of I/O	21
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmx02-256ze-2sg32c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmx02-256ze-2sg32c</a>

**Figure 2-8. sysMEM Memory Primitives**



**Table 2-6. EBR Signal Descriptions**

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE <sup>1</sup>	Output Clock Enable	Active High
RST	Reset	Active High
BE <sup>1</sup>	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	—
DI	Data In	—
DO	Data Out	—
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	—
FF	FIFO RAM Full Flag	—
AEF	FIFO RAM Almost Empty Flag	—
EF	FIFO RAM Empty Flag	—
RPRST	FIFO RAM Read Pointer Reset	—

1. Optional signals.

2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.

3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.

4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).

5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

## PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

**Table 2-8. PIO Signal List**

Pin Name	I/O Type	Description
CE	Input	Clock Enable
D	Input	Pin input from sysIO buffer.
INDD	Output	Register bypassed input.
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysIO Buffer
TQ	Output	Tri-state output signals to sysIO Buffer
DQSR90 <sup>1</sup>	Input	DQS shift 90-degree read clock
DQSW90 <sup>1</sup>	Input	DQS shift 90-degree write clock
DDRCLKPOL <sup>1</sup>	Input	DDR input register polarity control signal from DQS
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

1. Available in PIO on right edge only.

### Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition to this functionality, the input register blocks for the PIOs on the right edge include built-in logic to interface to DDR memory.

Figure 2-12 shows the input register block for the PIOs located on the left, top and bottom edges. Figure 2-13 shows the input register block for the PIOs on the right edge.

#### Left, Top, Bottom Edges

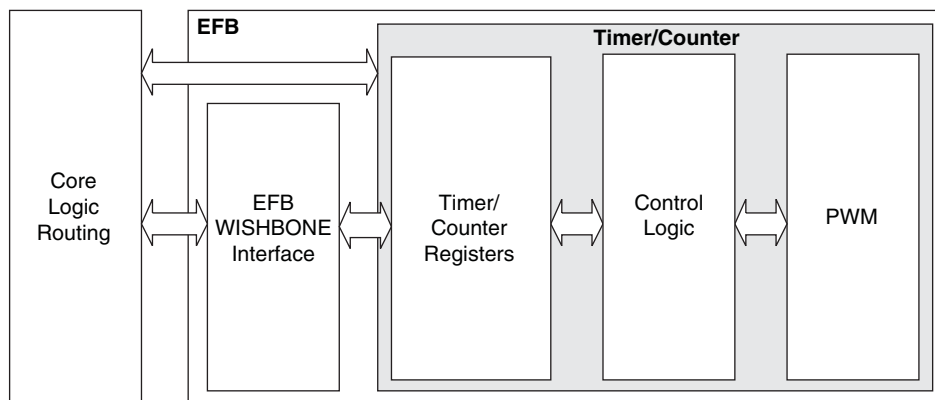
Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

## Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  - Watchdog timer
  - Clear timer on compare match
  - Fast PWM
  - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

**Figure 2-23. Timer/Counter Block Diagram**



**Table 2-17. Timer/Counter Signal Description**

Port	I/O	Description
tc_clk	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	O	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	O	Timer counter output signal

For more details on these embedded functions, please refer to TN1205, [Using User Flash Memory and Hardened Control Functions in MachXO2 Devices](#).

## User Flash Memory (UFM)

MachXO2-640/U and higher density devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I<sup>2</sup>C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1205, [Using User Flash Memory and Hardened Control Functions in MachXO2 Devices](#).

## Standby Mode and Power Saving Options

MachXO2 devices are available in three options for maximum flexibility: ZE, HC and HE devices. The ZE devices have ultra low static and dynamic power consumption. These devices use a 1.2 V core voltage that further reduces power consumption. The HC and HE devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V  $V_{CC}$  and 3.3 V  $V_{CC}$  while the HE devices operate at 1.2 V  $V_{CC}$ .

MachXO2 devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO2 devices support an ultra low power Stand-by mode. While most of these features are available in all three device types, these features are mainly intended for use with MachXO2 ZE devices to manage power consumption.

In the stand-by mode the MachXO2 devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I<sup>2</sup>C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO2 devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

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## Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

### IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with  $V_{CCIO}$  Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, [Boundary Scan Testability with Lattice sysIO Capability](#) and TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#).

### Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I<sup>2</sup>C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

1. Internal Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I<sup>2</sup>C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, [MachXO2 Programming and Configuration Usage Guide](#) for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

### TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#) for details.

When implementing background programming of the on-chip Flash, care must be taken for the operation of the PLL. For devices that have two PLLs (XO2-2000U, -4000 and -7000), the system must put the RPLL (Right-side PLL) in reset state during the background Flash programming. More detailed description can be found in TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

### **Security and One-Time Programmable Mode (OTP)**

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO2 devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile Flash memory spaces. The device can be in one of two modes:

1. Unlocked – Readback of the SRAM configuration and non-volatile Flash memory spaces is allowed.
2. Permanently Locked – The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

### **Dual Boot**

MachXO2 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the on-chip Flash. The golden image MUST reside in an external SPI Flash. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

### **Soft Error Detection**

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1206, [MachXO2 Soft Error Detection Usage Guide](#).

### **TraceID**

Each MachXO2 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I<sup>2</sup>C, or JTAG interfaces.

### **Density Shifting**

The MachXO2 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the [MachXO2 migration files](#).



# MachXO2 Family Data Sheet

## DC and Switching Characteristics

March 2017

Data Sheet DS1035

### Absolute Maximum Ratings<sup>1, 2, 3</sup>

	MachXO2 ZE/HE (1.2 V)	MachXO2 HC (2.5 V / 3.3 V)
Supply Voltage $V_{CC}$	–0.5 V to 1.32 V	–0.5 V to 3.75 V
Output Supply Voltage $V_{CCIO}$	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied <sup>4, 5</sup>	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied <sup>4</sup>	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature ( $T_J$ )	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to ( $V_{IHMAX} + 2$ ) volts is permitted for a duration of <20 ns.
5. The dual function I<sup>2</sup>C pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.

### Recommended Operating Conditions<sup>1</sup>

Symbol	Parameter	Min.	Max.	Units
$V_{CC}^1$	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V / 3.3 V Devices	2.375	3.6	V
$V_{CCIO}^{1, 2, 3}$	I/O Driver Supply Voltage	1.14	3.6	V
$t_{JCOM}$	Junction Temperature Commercial Operation	0	85	°C
$t_{JIND}$	Junction Temperature Industrial Operation	–40	100	°C

1. Like power supplies must be tied together. For example, if  $V_{CCIO}$  and  $V_{CC}$  are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3.  $V_{CCIO}$  pins of unused I/O banks should be connected to the  $V_{CC}$  power supply on boards.

### Power Supply Ramp Rates<sup>1</sup>

Symbol	Parameter	Min.	Typ.	Max.	Units
$t_{RAMP}$	Power supply ramp rates for all power supplies.	0.01	—	100	V/ms

1. Assumes monotonic ramp rates.



### Static Supply Current – HC/HE Devices<sup>1, 2, 3, 6</sup>

Symbol	Parameter	Device	Typ. <sup>4</sup>	Units
$I_{CC}$	Core Power Supply	LCMXO2-256HC	1.15	mA
		LCMXO2-640HC	1.84	mA
		LCMXO2-640UHC	3.48	mA
		LCMXO2-1200HC	3.49	mA
		LCMXO2-1200UHC	4.80	mA
		LCMXO2-2000HC	4.80	mA
		LCMXO2-2000UHC	8.44	mA
		LCMXO2-4000HC	8.45	mA
		LCMXO2-7000HC	12.87	mA
		LCMXO2-2000HE	1.39	mA
		LCMXO2-4000HE	2.55	mA
		LCMXO2-7000HE	4.06	mA
$I_{CCIO}$	Bank Power Supply <sup>5</sup> $V_{CCIO} = 2.5\text{ V}$	All devices	0	mA

- For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).
- Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at  $V_{CCIO}$  or GND, on-chip oscillator is off, on-chip PLL is off.
- Frequency = 0 MHz.
- $T_J = 25\text{ }^{\circ}\text{C}$ , power supplies at nominal voltage.
- Does not include pull-up/pull-down.
- To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

### Programming and Erase Flash Supply Current – HC/HE Devices<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Device	Typ. <sup>5</sup>	Units
$I_{CC}$	Core Power Supply	LCMXO2-256HC	14.6	mA
		LCMXO2-640HC	16.1	mA
		LCMXO2-640UHC	18.8	mA
		LCMXO2-1200HC	18.8	mA
		LCMXO2-1200UHC	22.1	mA
		LCMXO2-2000HC	22.1	mA
		LCMXO2-2000UHC	26.8	mA
		LCMXO2-4000HC	26.8	mA
		LCMXO2-7000HC	33.2	mA
		LCMXO2-2000HE	18.3	mA
		LCMXO2-2000UHE	20.4	mA
		LCMXO2-4000HE	20.4	mA
		LCMXO2-7000HE	23.9	mA
$I_{CCIO}$	Bank Power Supply <sup>6</sup>	All devices	0	mA

- For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).
- Assumes all inputs are held at  $V_{CCIO}$  or GND and all outputs are tri-stated.
- Typical user pattern.
- JTAG programming is at 25 MHz.
- $T_J = 25\text{ }^{\circ}\text{C}$ , power supplies at nominal voltage.
- Per bank.  $V_{CCIO} = 2.5\text{ V}$ . Does not include pull-up/pull-down.

## sysIO Recommended Operating Conditions

Standard	V <sub>CCIO</sub> (V)			V <sub>REF</sub> (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS 3.3	3.135	3.3	3.6	—	—	—
LVC MOS 2.5	2.375	2.5	2.625	—	—	—
LVC MOS 1.8	1.71	1.8	1.89	—	—	—
LVC MOS 1.5	1.425	1.5	1.575	—	—	—
LVC MOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.6	—	—	—
PCI <sup>3</sup>	3.135	3.3	3.6	—	—	—
SSTL25	2.375	2.5	2.625	1.15	1.25	1.35
SSTL18	1.71	1.8	1.89	0.833	0.9	0.969
HSTL18	1.71	1.8	1.89	0.816	0.9	1.08
LVC MOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVC MOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVC MOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVC MOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVC MOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVC MOS12R33 <sup>4</sup>	3.135	3.3	3.6	0.45	0.6	0.75
LVC MOS12R25 <sup>4</sup>	2.375	2.5	2.625	0.45	0.6	0.75
LVC MOS10R33 <sup>4</sup>	3.135	3.3	3.6	0.35	0.5	0.65
LVC MOS10R25 <sup>4</sup>	2.375	2.5	2.625	0.35	0.5	0.65
LVDS25 <sup>1, 2</sup>	2.375	2.5	2.625	—	—	—
LVDS33 <sup>1, 2</sup>	3.135	3.3	3.6	—	—	—
LVPECL <sup>1</sup>	3.135	3.3	3.6	—	—	—
BLVDS <sup>1</sup>	2.375	2.5	2.625	—	—	—
RSDS <sup>1</sup>	2.375	2.5	2.625	—	—	—
SSTL18D	1.71	1.8	1.89	—	—	—
SSTL25D	2.375	2.5	2.625	—	—	—
HSTL18D	1.71	1.8	1.89	—	—	—

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.

2. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.

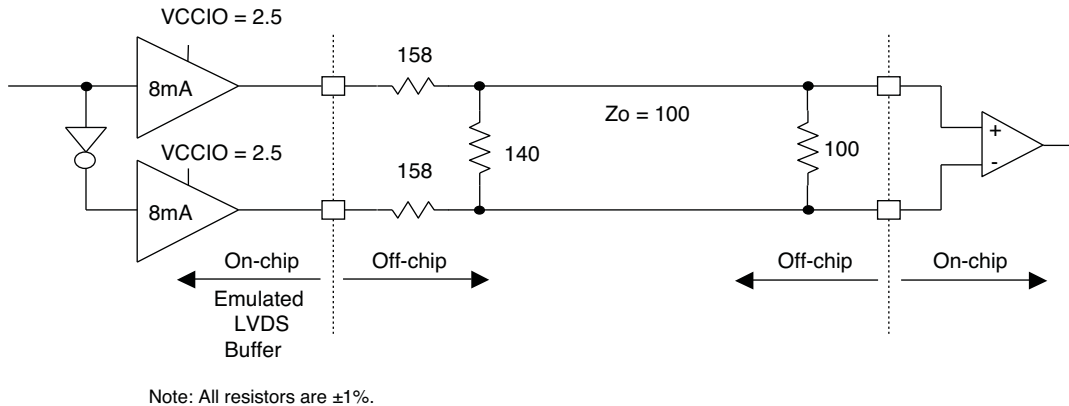
3. Input on the bottom bank of the MachXO2-640U, MachXO2-1200/U and larger devices only.

4. Supported only for inputs and BIDs for all ZE devices, and –6 speed grade for HE and HC devices.

### LVDS Emulation

MachXO2 devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

**Figure 3-1. LVDS Using External Resistors (LVDS25E)**



**Table 3-1. LVDS25E DC Conditions**

#### Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
$Z_{OUT}$	Output impedance	20	Ohms
$R_S$	Driver series resistor	158	Ohms
$R_P$	Driver parallel resistor	140	Ohms
$R_T$	Receiver termination	100	Ohms
$V_{OH}$	Output high voltage	1.43	V
$V_{OL}$	Output low voltage	1.07	V
$V_{OD}$	Output differential voltage	0.35	V
$V_{CM}$	Output common mode voltage	1.25	V
$Z_{BACK}$	Back impedance	100.5	Ohms
$I_{DC}$	DC output current	6.03	mA

## Typical Building Block Function Performance – HC/HE Devices<sup>1</sup>

### Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	-6 Timing	Units
<b>Basic Functions</b>		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

### Register-to-Register Performance

Function	-6 Timing	Units
<b>Basic Functions</b>		
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
<b>Embedded Memory Functions</b>		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
<b>Distributed Memory Functions</b>		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

Parameter	Description	Device	-6		-5		-4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR <sup>9, 12</sup>									
t <sub>DVADQ</sub>	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. <sup>13</sup>	—	0.369	—	0.395	—	0.421	UI
t <sub>DVEDQ</sub>	Input Data Hold After DQS Input		0.529	—	0.530	—	0.527	—	UI
t <sub>DQVBS</sub>	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t <sub>DQVAS</sub>	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f <sub>DATA</sub>	MEM LPDDR Serial Data Speed		—	280	—	250	—	208	Mbps
f <sub>SCLK</sub>	SCLK Frequency		—	140	—	125	—	104	MHz
f <sub>LPDDR</sub>	LPDDR Data Transfer Rate		0	280	0	250	0	208	Mbps
DDR <sup>9, 12</sup>									
t <sub>DVADQ</sub>	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. <sup>13</sup>	—	0.350	—	0.387	—	0.414	UI
t <sub>DVEDQ</sub>	Input Data Hold After DQS Input		0.545	—	0.538	—	0.532	—	UI
t <sub>DQVBS</sub>	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t <sub>DQVAS</sub>	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f <sub>DATA</sub>	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f <sub>SCLK</sub>	SCLK Frequency		—	150	—	125	—	104	MHz
f <sub>MEM_DDR</sub>	MEM DDR Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps
DDR2 <sup>9, 12</sup>									
t <sub>DVADQ</sub>	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. <sup>13</sup>	—	0.360	—	0.378	—	0.406	UI
t <sub>DVEDQ</sub>	Input Data Hold After DQS Input		0.555	—	0.549	—	0.542	—	UI
t <sub>DQVBS</sub>	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t <sub>DQVAS</sub>	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f <sub>DATA</sub>	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f <sub>SCLK</sub>	SCLK Frequency		—	150	—	125	—	104	MHz
f <sub>MEM_DDR2</sub>	MEM DDR2 Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps

- Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
- General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
- Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
- DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
- 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
- For Generic DDRX1 mode  $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$ .
- The  $t_{SU\_DEL}$  and  $t_{H\_DEL}$  values use the SCLK\_ZERHOLD default step size. Each step is 105 ps (-6), 113 ps (-5), 120 ps (-4).
- This number for general purpose usage. Duty cycle tolerance is +/- 10%.
- Duty cycle is +/-5% for system usage.
- The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
- High-speed DDR and LVDS not supported in SG32 (32 QFN) packages.
- Advance information for MachXO2 devices in 48 QFN packages.
- DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

### Signal Descriptions

Signal Name	I/O	Descriptions
<b>General Purpose</b>		
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	<p>[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).</p> <p>[Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.</p> <p>[A/B/C/D] indicates the PIO within the group to which the pad is connected.</p> <p>Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic.</p> <p>During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.</p>
NC	—	No connect.
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together. For QFN 48 package, the exposed die pad is the device ground.
VCC	—	VCC – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIOx	—	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.
<b>PLL and Clock Functions</b> (Used as user-programmable I/O pins when not used for PLL or clock pins)		
[LOC]_GPLL[T, C]_IN	—	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.
<b>Test and Programming</b> (Dual function pins used for test access port and during sysCONFIG™)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
JTAGENB	I	<p>Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then:</p> <p>If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O.</p> <p>If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.</p> <p>For more details, refer to TN1204, <a href="#">MachXO2 Programming and Configuration Usage Guide</a>.</p>
<b>Configuration</b> (Dual function pins used during sysCONFIG)		
PROGRAMN	I	Initiates configuration sequence when asserted low. During configuration, or when reserved as PROGRAMN in user mode, this pin always has an active pull-up.

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**Signal Descriptions (Cont.)**

Signal Name	I/O	Descriptions
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, or when reserved as INITn in user mode, this pin has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress. During configuration, or when reserved as DONE in user mode, this pin has an active pull-up.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.
SCL	I/O	Slave I <sup>2</sup> C clock input and master I <sup>2</sup> C clock output.
SDA	I/O	Slave I <sup>2</sup> C data input and master I <sup>2</sup> C data output.

	MachXO2-1200					MachXO2-1200U
	100 TQFP	132 csBGA	144 TQFP	25 WLCSP	32 QFN <sup>1</sup>	256 ftBGA
<b>General Purpose I/O per Bank</b>						
Bank 0	18	25	27	11	9	50
Bank 1	21	26	26	0	2	52
Bank 2	20	28	28	7	9	52
Bank 3	20	25	26	0	2	16
Bank 4	0	0	0	0	0	16
Bank 5	0	0	0	0	0	20
Total General Purpose Single Ended I/O	79	104	107	18	22	206
<b>Differential I/O per Bank</b>						
Bank 0	9	13	14	5	4	25
Bank 1	10	13	13	0	1	26
Bank 2	10	14	14	2	4	26
Bank 3	10	12	13	0	1	8
Bank 4	0	0	0	0	0	8
Bank 5	0	0	0	0	0	10
Total General Purpose Differential I/O	39	52	54	7	10	103
<b>Dual Function I/O</b>						
	31	33	33	18	22	33
<b>High-speed Differential I/O</b>						
Bank 0	4	7	7	0	0	14
<b>Gearboxes</b>						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	4	7	7	0	0	14
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	5	7	7	0	2	14
<b>DQS Groups</b>						
Bank 1	1	2	2	0	0	2
<b>VCCIO Pins</b>						
Bank 0	2	3	3	1	2	4
Bank 1	2	3	3	0	1	4
Bank 2	2	3	3	1	2	4
Bank 3	3	3	3	0	1	1
Bank 4	0	0	0	0	0	2
Bank 5	0	0	0	0	0	1
VCC	2	4	4	2	2	8
GND	8	10	12	2	2	24
NC	1	1	8	0	0	1
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	100	132	144	25	32	256

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.



## **For Further Information**

For further information regarding logic signal connections for various packages please refer to the MachXO2 Device Pinout Files.

## **Thermal Management**

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Users must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

## **For Further Information**

For further information regarding Thermal Management, refer to the following:

- [Thermal Management](#) document
- TN1198, [Power Estimation and Management for MachXO2 Devices](#)
- The Power Calculator tool is included with the Lattice design tools, or as a standalone download from [www.latticesemi.com/software](http://www.latticesemi.com/software)

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1UWG49ITR <sup>1</sup>	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR50 <sup>3</sup>	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR1K <sup>2</sup>	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1TG100I	2112	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-2TG100I	2112	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-3TG100I	2112	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-1MG132I	2112	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-2MG132I	2112	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-3MG132I	2112	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-1TG144I	2112	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-2TG144I	2112	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-3TG144I	2112	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-1BG256I	2112	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-2BG256I	2112	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-3BG256I	2112	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-1FTG256I	2112	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-2FTG256I	2112	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-3FTG256I	2112	1.2 V	–3	Halogen-Free ftBGA	256	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

# MachXO2 Family Data Sheet

## Revision History

March 2017

Data Sheet DS1035

Date	Version	Section	Change Summary
March 2017	3.3	DC and Switching Characteristics	Updated the <a href="#">Absolute Maximum Ratings</a> section. Added standards.
			Updated the <a href="#">sysIO Recommended Operating Conditions</a> section. Added standards.
			Updated the <a href="#">sysIO Single-Ended DC Electrical Characteristics</a> section. Added standards.
			Updated the <a href="#">MachXO2 External Switching Characteristics – HC/HE Devices</a> section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the $D_{VB}$ and the $D_{VA}$ parameters were changed to $D_{IB}$ and $D_{IA}$ . The parameter descriptions were also modified.
			Updated the <a href="#">MachXO2 External Switching Characteristics – ZE Devices</a> section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the $D_{VB}$ and the $D_{VA}$ parameters were changed to $D_{IB}$ and $D_{IA}$ . The parameter descriptions were also modified.
			Updated the <a href="#">sysCONFIG Port Timing Specifications</a> section. Corrected the $t_{INITL}$ units from ns to $\mu$ s.
		Pinout Information	Updated the <a href="#">Signal Descriptions</a> section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals.
			Updated the <a href="#">Pinout Information Summary</a> section. Added footnote to MachXO2-1200 32 QFN.
		Ordering Information	Updated the <a href="#">MachXO2 Part Number Description</a> section. Corrected the MG184, BG256, FTG256 package information. Added “(0.8 mm Pitch)” to BG332.
			Updated the <a href="#">Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging</a> section. — Updated LCMXO2-1200ZE-1UWG25ITR50 footnote. — Corrected footnote numbering typo. — Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2-2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s.

Date	Version	Section	Change Summary		
May 2016	3.2	All	Moved designation for 84 QFN package information from 'Advanced' to 'Final'.		
		Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 'Advanced' 48 QFN package. — Revised footnote 6. — Added footnote 9.		
		DC and Switching Characteristics	Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Added footnote 12.		
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Added footnote 12.		
		Pinout Information	Updated the Signal Descriptions section. Added information on GND signal.		
			Updated the Pinout Information Summary section. — Added 'Advanced' MachXO2-256 48 QFN values. — Added 'Advanced' MachXO2-640 48 QFN values. — Added footnote to GND. — Added footnotes 2 and 3.		
		Ordering Information	Updated the MachXO2 Part Number Description section. Added 'Advanced' SG48 package and revised footnote.		
			Updated the Ordering Information section. — Added part numbers for 'Advanced' QFN 48 package.		
March 2016	3.1	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 32 QFN value for XO2-1200. — Added 84 QFN (7 mm x 7 mm, 0.5 mm) package. — Modified package name to 100-pin TQFP. — Modified package name to 144-pin TQFP. — Added footnote.		
		Architecture	Updated the Typical I/O Behavior During Power-up section. Removed reference to TN1202.		
		DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications section. Revised t <sub>DPPDONE</sub> and t <sub>DPPINIT</sub> Max. values per PCN 03A-16, released March 2016.		
		Pinout Information	Updated the Pinout Information Summary section. — Added MachXO2-1200 32 QFN values. — Added 'Advanced' MachXO2-4000 84 QFN values.		
		Ordering Information	Updated the MachXO2 Part Number Description section. Added 'Advanced' QN84 package and footnote.		
			Updated the Ordering Information section. — Added part numbers for 1280 LUTs QFN 32 package. — Added part numbers for 4320 LUTs QFN 84 package.		
		March 2015	3.0	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Changed 64-ball ucBGA dimension.
				Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.

Date	Version	Section	Change Summary
May 2014	2.5	Architecture	Updated TransFR (Transparent Field Reconfiguration) section. Updated TransFR description for PLL use during background Flash programming.
February 2014	02.4	Introduction	Included the 49 WLCSP package in the MachXO2 Family Selection Guide table.
		Architecture	Added information to Standby Mode and Power Saving Options section.
		Pinout Information	Added the XO2-2000 49 WLCSP in the Pinout Information Summary table.
		Ordering Information	Added UW49 package in MachXO2 Part Number Description.
			Added and LCMXO2-2000ZE-1UWG49CTR in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging section.
December 2013	02.3	Architecture	Added and LCMXO2-2000ZE-1UWG49ITR in Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section.
			Updated information on CLKOS output divider in sysCLOCK Phase Locked Loops (PLLs) section.
		DC and Switching Characteristics	Updated Static Supply Current – ZE Devices table.
			Updated footnote 4 in sysIO Single-Ended DC Electrical Characteristics table; Updated $V_{IL}$ Max. (V) data for LVCMOS 25 and LVCMOS 28.
September 2013	02.2	Architecture	Updated $V_{OS}$ test condition in sysIO Differential Electrical Characteristics - LVDS table.
			Removed I <sup>2</sup> C Clock-Stretching feature per PCN #10A-13.
			Removed information on PDPR memory in RAM Mode section.
		DC and Switching Characteristics	Updated Supported Input Standards table.
June 2013	02.1	Architecture	Updated Power-On-Reset Voltage Levels table.
			Architecture Overview – Added information on the state of the register on power up and after configuration.
		DC and Switching Characteristics	sysCLOCK Phase Locked Loops (PLLs) section – Added missing cross reference to sysCLOCK PLL Timing table.
			Added slew rate information to footnote 2 of the MachXO2 External Switching Characteristics – HC/HE Devices and the MachXO2 External Switching Characteristics – ZE Devices tables.
			Power-On-Reset Voltage Levels table – Added symbols.