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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	32
Number of Logic Elements/Cells	256
Total RAM Bits	-
Number of I/O	55
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-256ze-3mg132c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the $t_{I,OCK}$ parameter has been satisfied.

The MachXO2 also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO2 PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the t_{LOCK} parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

For more details on the PLL and the WISHBONE interface, see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.



Figure 2-7. PLL Diagram

Table 2-4 provides signal descriptions of the PLL block.

Port Name	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	I	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	I	Dynamic Phase step – toggle shifts VCO phase adjust by one step.



Figure 2-8. sysMEM Memory Primitives



Table 2-6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE ¹	Output Clock Enable	Active High
RST	Reset	Active High
BE ¹	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	
DI	Data In	_
DO	Data Out	_
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	_
FF	FIFO RAM Full Flag	_
AEF	FIFO RAM Almost Empty Flag	_
EF	FIFO RAM Empty Flag	_
RPRST	FIFO RAM Read Pointer Reset	_

1. Optional signals.

2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.

3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.

4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).

5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.



Figure 2-12. MachXO2 Input Register Block Diagram (PIO on Left, Top and Bottom Edges)



Right Edge

The input register block on the right edge is a superset of the same block on the top, bottom, and left edges. In addition to the modes described above, the input register block on the right edge also supports DDR memory mode.

In DDR memory mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (DQSR90) in the DDR Memory mode creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the DQS domain. The DQSR90 and DDRCLKPOL signals are generated in the DQS read-write block.

Figure 2-13. MachXO2 Input Register Block Diagram (PIO on Right Edge)









Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

The tri-state register blocks on the right edge contain an additional register for DDR memory operation. In DDR memory mode, the register TS input is fed into another register that is clocked using the DQSW90 signal. The output of this register is used as a tri-state control.

Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

Table 2-9.	Input	Gearbox	Sianal List
14010 2 01	mpat	acaison	orginal Eloc

Name	I/O Type	Description		
D	Input	High-speed data input after programmable delay in PIO A input register block		
ALIGNWD	Input	Data alignment signal from device core		
SCLK	Input	Slow-speed system clock		
ECLK[1:0]	Input	High-speed edge clock		
RST	Input	Reset		
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3		



These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-16 shows a block diagram of the input gearbox.

Figure 2-16. Input Gearbox





There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology (Appendix B)
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices

Figure 2-22. SPI Core Block Diagram



Table 2-16 describes the signals interfacing with the SPI cores.

Table 2-16. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	0	Master	SPI master chip-select output
spi_csn[17]	0	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	0	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
ufm_sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the User Flash Memory (UFM).
cfg_stdby	0	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.
cfg_wake	0	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.



Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe V_{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1198, Power Estimation and Management for MachXO2 Devices.

Power On Reset

MachXO2 devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the V_{PORUP} level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices), V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators (HC devices), V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time (t_{REFRESH}) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tristate. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min) they should not shut down the bandgap or POR circuit.



MachXO2 Family Data Sheet DC and Switching Characteristics

March 2017

Data Sheet DS1035

Absolute Maximum Ratings^{1, 2, 3}

	MachXO2 ZE/HE (1.2 V)	MachXO2 HC (2.5 V / 3.3 V)
Supply Voltage V _{CC}	–0.5 V to 1.32 V	0.5 V to 3.75 V
Output Supply Voltage V _{CCIO}	–0.5 V to 3.75 V	0.5 V to 3.75 V
I/O Tri-state Voltage Applied ^{4, 5}	–0.5 V to 3.75 V	0.5 V to 3.75 V
Dedicated Input Voltage Applied ⁴	–0.5 V to 3.75 V	0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T_1)	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

2. Compliance with the Lattice Thermal Management document is required.

3. All voltages referenced to GND.

4. Overshoot and undershoot of -2 V to (V_{IHMAX} + 2) volts is permitted for a duration of <20 ns.

5. The dual function I^2C pins SCL and SDA are limited to -0.25 V to 3.75 V or to -0.3 V with a duration of <20 ns.

Recommended Operating Conditions¹

Symbol	Parameter	Min.	Max.	Units
V = = ¹	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
VCC	Core Supply Voltage for 2.5 V / 3.3 V Devices	2.375	3.6	V
V _{CCIO} ^{1, 2, 3}	I/O Driver Supply Voltage	1.14	3.6	V
t _{JCOM}	Junction Temperature Commercial Operation	0	85	°C
t _{JIND}	Junction Temperature Industrial Operation	-40	100	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.

2. See recommended voltages by I/O standard in subsequent table.

3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

Power Supply Ramp Rates¹

Symbol	Parameter	Min.	Тур.	Max.	Units
t _{RAMP}	Power supply ramp rates for all power supplies.	0.01		100	V/ms

1. Assumes monotonic ramp rates.

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Power-On-Reset Voltage Levels^{1, 2, 3, 4, 5}

Symbol	Parameter	Min.	Тур.	Max.	Units
V _{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and $V_{CCIO0})$	0.9	_	1.06	V
V _{PORUPEXT}	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	_	2.1	V
V _{PORDNBG}	Power-On-Reset ramp down trip point (band gap based circuit monitoring $V_{CCINT})$	0.75	_	0.93	V
V _{PORDNBGEXT}	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	_	1.33	V
V _{PORDNSRAM}	Power-On-Reset ramp down trip point (SRAM based circuit monitoring $V_{\mbox{CCINT}}$)	-	0.6	_	V
V _{PORDNSRAMEXT}	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	_	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.

3. Note that V_{PORUP} (min.) and V_{PORDNBG} (max.) are in different process corners. For any given process corner V_{PORDNBG} (max.) is always 12.0 mV below V_{PORUP} (min.).

4. V_{PORUPEXT} is for HC devices only. In these devices a separate POR circuit monitors the external V_{CC} power supply.

5. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

Programming/Erase Specifications

Symbol	Parameter	Min.	Max. ¹	Units
	Flash Programming cycles per t _{RETENTION}	—	10,000	Cycles
PROGCYC	Flash functional programming cycles	—	100,000	Oycles
t	Data retention at 100 °C junction temperature	10	—	Voars
RETENTION	Data retention at 85 °C junction temperature	20	—	leais

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

Hot Socketing Specifications^{1, 2, 3}

I_{DK} Input or I/O leakage Current $0 < V_{IN} < V_{IH}$ (MAX) +/-1000 μ A	Symbol	Parameter	Condition	Max.	Units
	I _{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/-1000	μΑ

1. Insensitive to sequence of V_{CC} and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO} .

2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).

3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

ESD Performance

Please refer to the MachXO2 Product Family Qualification Summary for complete qualification data, including ESD performance.



Programming and Erase Flash Supply Current – ZE Devices^{1, 2, 3, 4}

Symbol	Parameter	Device	Typ.⁵	Units
I _{CC}		LCMXO2-256ZE	13	mA
		LCMXO2-640ZE	14	mA
	Core Power Supply	LCMXO2-1200ZE	15	mA
		LCMXO2-2000ZE	17	mA
		LCMXO2-4000ZE	18	mA
		LCMXO2-7000ZE	20	mA
I _{CCIO}	Bank Power Supply ⁶	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.

2. Assumes all inputs are held at $V_{\mbox{CCIO}}$ or GND and all outputs are tri-stated.

3. Typical user pattern.

4. JTAG programming is at 25 MHz.

5. TJ = 25 °C, power supplies at nominal voltage.

6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.



RSDS

The MachXO2 family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.



Figure 3-4. RSDS (Reduced Swing Differential Standard)

Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z _{OUT}	Output impedance	20	Ohms
R _S	Driver series resistor	294	Ohms
R _P	Driver parallel resistor	121	Ohms
R _T	Receiver termination	100	Ohms
V _{OH}	Output high voltage	1.35	V
V _{OL}	Output low voltage	1.15	V
V _{OD}	Output differential voltage	0.20	V
V _{CM}	Output common mode voltage	1.25	V
Z _{BACK}	Back impedance	101.5	Ohms
I _{DC}	DC output current	3.66	mA





			-6		-6		_	5	_	4	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units		
		MachXO2-256HC-HE	1.42	_	1.59	_	1.96	_	ns		
		MachXO2-640HC-HE	1.41	_	1.58	_	1.96	_	ns		
	Clock to Data Setup – PIO	MachXO2-1200HC-HE	1.63	_	1.79	_	2.17	_	ns		
^I SU_DEL	Delav	MachXO2-2000HC-HE	1.61	_	1.76	_	2.13	_	ns		
		MachXO2-4000HC-HE	1.66	_	1.81	_	2.19	_	ns		
		MachXO2-7000HC-HE	1.53	_	1.67		2.03		ns		
		MachXO2-256HC-HE	-0.24	_	-0.24		-0.24		ns		
		MachXO2-640HC-HE	-0.23	_	-0.23	_	-0.23	_	ns		
+	Clock to Data Hold – PIO Input	MachXO2-1200HC-HE	-0.24	_	-0.24	_	-0.24	_	ns		
'H_DEL	Register with Input Data Delay	MachXO2-2000HC-HE	-0.23	_	-0.23		-0.23		ns		
		MachXO2-4000HC-HE	-0.25	_	-0.25		-0.25		ns		
		MachXO2-7000HC-HE	-0.21		-0.21		-0.21		ns		
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices		388	_	323	_	269	MHz		
General I/O	Pin Parameters (Using Edge C	lock without PLL)									
		MachXO2-1200HC-HE	_	7.53		7.76		8.10	ns		
+	Clock to Output – PIO Output	MachXO2-2000HC-HE		7.53		7.76		8.10	ns		
COE	Register	MachXO2-4000HC-HE		7.45		7.68		8.00	ns		
		MachXO2-7000HC-HE		7.53		7.76		8.10	ns		
		MachXO2-1200HC-HE	-0.19	_	-0.19	_	-0.19	_	ns		
	Clock to Data Setup – PIO Input Register	MachXO2-2000HC-HE	-0.19	_	-0.19	_	-0.19	_	ns		
t _{SUE} Input Re		MachXO2-4000HC-HE	-0.16	_	-0.16	_	-0.16	_	ns		
		MachXO2-7000HC-HE	-0.19	_	-0.19		-0.19		ns		
		MachXO2-1200HC-HE	1.97	_	2.24	_	2.52	_	ns		
	Clock to Data Hold – PIO Input	MachXO2-2000HC-HE	1.97	_	2.24	_	2.52	_	ns		
ΉE	Register	MachXO2-4000HC-HE	1.89	_	2.16	_	2.43		ns		
		MachXO2-7000HC-HE	1.97	_	2.24	_	2.52	_	ns		
		MachXO2-1200HC-HE	1.56	_	1.69	_	2.05	_	ns		
	Clock to Data Setup – PIO	MachXO2-2000HC-HE	1.56	_	1.69	_	2.05	_	ns		
^I SU_DELE	Delay	MachXO2-4000HC-HE	1.74	_	1.88	_	2.25	_	ns		
		MachXO2-7000HC-HE	1.66	_	1.81	_	2.17	_	ns		
		MachXO2-1200HC-HE	-0.23	_	-0.23	_	-0.23	_	ns		
+	Clock to Data Hold – PIO Input	MachXO2-2000HC-HE	-0.23	_	-0.23		-0.23		ns		
'H_DELE	Register with Input Data Delay	MachXO2-4000HC-HE	-0.34	_	-0.34		-0.34		ns		
		MachXO2-7000HC-HE	-0.29	_	-0.29		-0.29		ns		
General I/O	Pin Parameters (Using Primary	y Clock with PLL)									
t _{COPLL}		MachXO2-1200HC-HE	—	5.97		6.00		6.13	ns		
	Clock to Output – PIO Output	MachXO2-2000HC-HE		5.98		6.01		6.14	ns		
	Register	MachXO2-4000HC-HE		5.99		6.02		6.16	ns		
		MachXO2-7000HC-HE		6.02		6.06		6.20	ns		
		MachXO2-1200HC-HE	0.36	—	0.36	—	0.65	—	ns		
+.	Clock to Data Setup – PIO	MachXO2-2000HC-HE	0.36	—	0.36	—	0.63	—	ns		
SUPLL	Input Register	MachXO2-4000HC-HE	0.35	—	0.35	—	0.62	—	ns		
		MachXO2-7000HC-HE	0.34	—	0.34	—	0.59	—	ns		
	1	•			•		•				



			-	-3		-2	-	1	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Generic DDR4	Inputs with Clock and Data Cer	ntered at Pin Using PC	LK Pin fo	or Clock	Input –	GDDRX4	LRX.EC	LK.Cent	ered ^{9, 12}
t _{SU}	Input Data Setup Before ECLK		0.434		0.535		0.630	—	ns
t _{HO}	Input Data Hold After ECLK	MachXO2-640U,	0.385		0.395		0.463	—	ns
f _{DATA}	DDRX4 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	420	_	352	_	292	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency	bottom side only'		210		176	—	146	MHz
f _{SCLK}	SCLK Frequency		—	53		44	—	37	MHz
7:1 LVDS Inp	uts – GDDR71_RX.ECLK.7.1 ^{9, 1}	2							
t _{DVA}	Input Data Valid After ECLK		—	0.307		0.316	—	0.326	UI
t _{DVE}	Input Data Hold After ECLK		0.662		0.650		0.649	—	UI
f _{DATA}	DDR71 Serial Input Data Speed	MachXO2-640U, MachXO2-1200/U	—	420	_	352	_	292	Mbps
f _{DDR71}	DDR71 ECLK Frequency	and larger devices,		210		176	—	146	MHz
f _{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		_	60	_	50	_	42	MHz
Generic DDR	Outputs with Clock and Data A	ligned at Pin Using PC	LK Pin f	for Clock	k Input –	GDDRX	(1_TX.S	CLK.Aliç	gned ^{9, 12}
t _{DIA}	Output Data Invalid After CLK Output		—	0.850	—	0.910	—	0.970	ns
t _{DIB}	Output Data Invalid Before CLK Output	All MachXO2 devices, all sides		0.850	_	0.910	_	0.970	ns
f _{DATA}	DDRX1 Output Data Speed			140	—	116		98	Mbps
f _{DDRX1}	DDRX1 SCLK frequency			70		58		49	MHz
Generic DDR	Outputs with Clock and Data Ce	ntered at Pin Using PC	LK Pin f	or Clock	Input –	GDDRX	1_TX.SC	LK.Cen	tered ^{9, 12}
t _{DVB}	Output Data Valid Before CLK Output		2.720	_	3.380	_	4.140	_	ns
t _{DVA}	Output Data Valid After CLK Output	All MachXO2	2.720	_	3.380	_	4.140	_	ns
f _{DATA}	DDRX1 Output Data Speed	devices, all sides		140	—	116		98	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)			70	_	58	_	49	MHz
Generic DDR	X2 Outputs with Clock and Data	Aligned at Pin Using P	CLK Pin	for Cloc	k Input	- GDDR	X2_TX.E	CLK.Ali	gned ^{9, 12}
t _{DIA}	Output Data Invalid After CLK Output			0.270	_	0.300	_	0.330	ns
t _{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U	_	0.270	_	0.300	_	0.330	ns
f _{DATA}	DDRX2 Serial Output Data Speed	and larger devices, top side only		280	_	234	_	194	Mbps
f _{DDRX2}	DDRX2 ECLK frequency	1	—	140	—	117	—	97	MHz
f _{SCLK}	SCLK Frequency			70		59	_	49	MHz



MachXO2 Family Data Sheet Ordering Information

March 2017

Data Sheet DS1035

MachXO2 Part Number Description



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Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144C	6864	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	СОМ
LCMXO2-7000HC-5TG144C	6864	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-6TG144C	6864	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-4BG256C	6864	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-5BG256C	6864	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-6BG256C	6864	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-4FTG256C	6864	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-5FTG256C	6864	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-6FTG256C	6864	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-4BG332C	6864	2.5 V / 3.3 V	-4	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-5BG332C	6864	2.5 V / 3.3 V	-5	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-6BG332C	6864	2.5 V / 3.3 V	-6	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-4FG400C	6864	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-5FG400C	6864	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-6FG400C	6864	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-4FG484C	6864	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-5FG484C	6864	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-6FG484C	6864	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100CR1 ¹	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100CR1 ¹	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100CR1 ¹	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132CR11	1280	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132CR11	1280	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132CR11	1280	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144CR1 ¹	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144CR1 ¹	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144CR11	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	COM

1. Specifications for the "LCMXO2-1200HC-speed package CR1" are the same as the "LCMXO2-1200HC-speed package C" devices respectively, except as specified in the R1 Device Specifications section of this data sheet.



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100IR11	1280	1.2 V	-1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100IR11	1280	1.2 V	-2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100IR11	1280	1.2 V	-3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132IR1 ¹	1280	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132IR1 ¹	1280	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132IR11	1280	1.2 V	-3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144IR11	1280	1.2 V	-1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144IR11	1280	1.2 V	-2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144IR11	1280	1.2 V	-3	Halogen-Free TQFP	144	IND

1. Specifications for the "LCMXO2-1200ZE-speed package IR1" are the same as the "LCMXO2-1200ZE-speed package I" devices respectively, except as specified in the R1 Device Specifications section of this data sheet.



Date	Version	Section	Change Summary
May 2014	2.5	Architecture	Updated TransFR (Transparent Field Reconfiguration) section. Updated TransFR description for PLL use during background Flash programming.
February 2014	02.4	Introduction	Included the 49 WLCSP package in the MachXO2 Family Selection Guide table.
		Architecture	Added information to Standby Mode and Power Saving Options sec- tion.
		Pinout Information	Added the XO2-2000 49 WLCSP in the Pinout Information Summary table.
		Ordering Information	Added UW49 package in MachXO2 Part Number Description.
			Added and LCMXO2-2000ZE-1UWG49CTR in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging sec- tion.
			Added and LCMXO2-2000ZE-1UWG49ITR in Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section.
December 2013	02.3	Architecture	Updated information on CLKOS output divider in sysCLOCK Phase Locked Loops (PLLs) section.
	DC and Switching	Updated Static Supply Current – ZE Devices table.	
		Characteristics	Updated footnote 4 in sysIO Single-Ended DC Electrical Characteristics table; Updated V_{IL} Max. (V) data for LVCMOS 25 and LVCMOS 28.
			Updated $\rm V_{OS}$ test condition in sysIO Differential Electrical Characteristics - LVDS table.
September 2013	02.2	Architecture	Removed I ² C Clock-Stretching feature per PCN #10A-13.
			Removed information on PDPR memory in RAM Mode section.
			Updated Supported Input Standards table.
		DC and Switching Characteristics	Updated Power-On-Reset Voltage Levels table.
June 2013	02.1	Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.
			sysCLOCK Phase Locked Loops (PLLs) section – Added missing cross reference to sysCLOCK PLL Timing table.
		DC and Switching Characteristics	Added slew rate information to footnote 2 of the MachXO2 External Switching Characteristics – HC/HE Devices and the MachXO2 Exter- nal Switching Characteristics – ZE Devices tables.
			Power-On-Reset Voltage Levels table – Added symbols.



Date	Version	Section	Change Summary
January 2013	02.0	Introduction	Updated the total number IOs to include JTAGENB.
		Architecture	Supported Output Standards table – Added 3.3 $\rm V_{\rm CCIO}$ (Typ.) to LVDS row.
			Changed SRAM CRC Error Detection to Soft Error Detection.
		DC and Switching Characteristics	Power Supply Ramp Rates table – Updated Units column for t _{RAMP} symbol.
			Added new Maximum sysIO Buffer Performance table.
			sysCLOCK PLL Timing table – Updated Min. column values for f_{IN} ,
			f_{OUT},f_{OUT2} and f_{PFD} parameters. Added t_{SPO} parameter. Updated footnote 6.
			MachXO2 Oscillator Output Frequency table – Updated symbol name for t _{STABLEOSC} .
			DC Electrical Characteristics table – Updated conditions for ${\rm I}_{\rm IL,}~{\rm I}_{\rm IH}$ symbols.
			Corrected parameters tDQVBS and tDQVAS
			Corrected MachXO2 ZE parameters tDVADQ and tDVEDQ
		Pinout Information	Included the MachXO2-4000HE 184 csBGA package.
		Ordering Information	Updated part number.
April 2012	01.9	Architecture	Removed references to TN1200.
		Ordering Information	Updated the Device Status portion of the MachXO2 Part Number Description to include the 50 parts per reel for the WLCSP package.
			Added new part number and footnote 2 for LCMXO2-1200ZE- 1UWG25ITR50.
			Updated footnote 1 for LCMXO2-1200ZE-1UWG25ITR.
		Supplemental Information	Removed references to TN1200.
March 2012	01.8	Introduction	Added 32 QFN packaging information to Features bullets and MachXO2 Family Selection Guide table.
	DC and Switching Characteristics	Changed 'STANDBY' to 'USERSTDBY' in Standby Mode timing dia- gram.	
		Pinout Information	Removed footnote from Pin Information Summary tables.
			Added 32 QFN package to Pin Information Summary table.
		Ordering Information	Updated Part Number Description and Ordering Information tables for 32 QFN package.
			Updated topside mark diagram in the Ordering Information section.



Date	Version	Section	Change Summary
February 2012	01.7	All	Updated document with new corporate logo.
	01.6	—	Data sheet status changed from preliminary to final.
		Introduction	MachXO2 Family Selection Guide table – Removed references to 49-ball WLCSP.
		DC and Switching Characteristics	Updated Flash Download Time table.
			Modified Storage Temperature in the Absolute Maximum Ratings section.
			Updated I _{DK} max in Hot Socket Specifications table.
			Modified Static Supply Current tables for ZE and HC/HE devices.
			Updated Power Supply Ramp Rates table.
			Updated Programming and Erase Supply Current tables.
			Updated data in the External Switching Characteristics table.
			Corrected Absolute Maximum Ratings for Dedicated Input Voltage Applied for LCMXO2 HC.
			DC Electrical Characteristics table – Minor corrections to conditions for $\mathbf{I}_{IL}, \mathbf{I}_{IH.}$
		Pinout Information	Removed references to 49-ball WLCSP.
			Signal Descriptions table – Updated description for GND, VCC, and VCCIOx.
			Updated Pin Information Summary table – Number of VCCIOs, GNDs, VCCs, and Total Count of Bonded Pins for MachXO2-256, 640, and 640U and Dual Function I/O for MachXO2-4000 332caBGA.
		Ordering Information	Removed references to 49-ball WLCSP
August 2011	01.5	DC and Switching Characteristics	Updated ESD information.
		Ordering Information	Updated footnote for ordering WLCSP devices.
	01.4	Architecture	Updated information in Clock/Control Distribution Network and sys- CLOCK Phase Locked Loops (PLLs).
		DC and Switching Characteristics	Updated ${\rm I}_{\rm IL}$ and ${\rm I}_{\rm IH}$ conditions in the DC Electrical Characteristics table.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Updated Pin Information Summary table: Dual Function I/O, DQS Groups Bank 1, Total General Purpose Single-Ended I/O, Differential I/O Per Bank, Total Count of Bonded Pins, Gearboxes.
			Added column of data for MachXO2-2000 49 WLCSP.
		Ordering Information	Updated R1 Device Specifications text section with information on migration from MachXO2-1200-R1 to Standard (non-R1) devices.
			Corrected Supply Voltage typo for part numbers: LCMX02-2000UHE- 4FG484I, LCMX02-2000UHE-5FG484I, LCMX02-2000UHE- 6FG484I.
			Added footnote for WLCSP package parts.
		Supplemental Information	Removed reference to Stand-alone Power Calculator for MachXO2 Devices. Added reference to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices.



Date	Version	Section	Change Summary
May 2011	01.3	Multiple	Replaced "SED" with "SRAM CRC Error Detection" throughout the document.
		DC and Switching Characteristics	Added footnote 1 to Program Erase Specifications table.
		Pinout Information	Updated Pin Information Summary tables.
			Signal name SO/SISPISO changed to SO/SPISO in the Signal Descriptions table.
April 2011	01.2	—	Data sheet status changed from Advance to Preliminary.
		Introduction	Updated MachXO2 Family Selection Guide table.
		Architecture	Updated Supported Input Standards table.
			Updated sysMEM Memory Primitives diagram.
			Added differential SSTL and HSTL IO standards.
		DC and Switching Characteristics	Updates following parameters: POR voltage levels, DC electrical characteristics, static supply current for ZE/HE/HC devices, static power consumption contribution of different components – ZE devices, programming and erase Flash supply current.
			Added VREF specifications to sysIO recommended operating condi- tions.
			Updating timing information based on characterization.
			Added differential SSTL and HSTL IO standards.
		Ordering Information	Added Ordering Part Numbers for R1 devices, and devices in WLCSP packages.
			Added R1 device specifications.
January 2011	01.1	All	Included ultra-high I/O devices.
		DC and Switching Characteristics	Recommended Operating Conditions table – Added footnote 3.
			DC Electrical Characteristics table – Updated data for $\rm I_{IL}, I_{IH}, V_{HYST}$ typical values updated.
			Generic DDRX2 Outputs with Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB} .
			Generic DDRX4 Outputs with Clock and Data Aligned at Pin (GDDRX4_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T _{DIA} and T _{DIB.}
			Power-On-Reset Voltage Levels table - clarified note 3.
			Clarified VCCIO related recommended operating conditions specifications.
			Added power supply ramp rate requirements.
			Added Power Supply Ramp Rates table.
			Updated Programming/Erase Specifications table.
			Removed references to V _{CCP.}
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Removed references to V _{CCP.}
November 2010	01.0	_	Initial release.