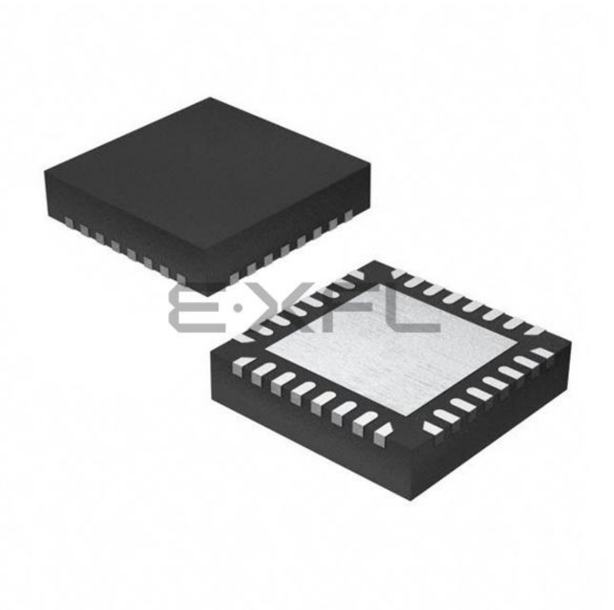

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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

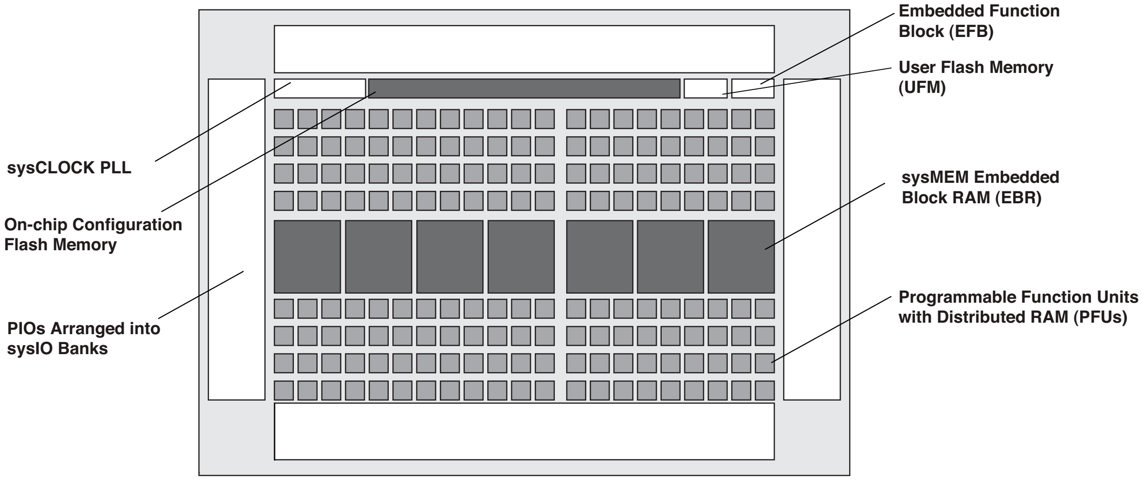
| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 32 |
| Number of Logic Elements/Cells | 256 |
| Total RAM Bits | - |
| Number of I/O | 21 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 32-UFQFN Exposed Pad |
| Supplier Device Package | 32-QFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-256ze-3sg32i |

March 2016 Data Sheet DS1035

## Architecture Overview

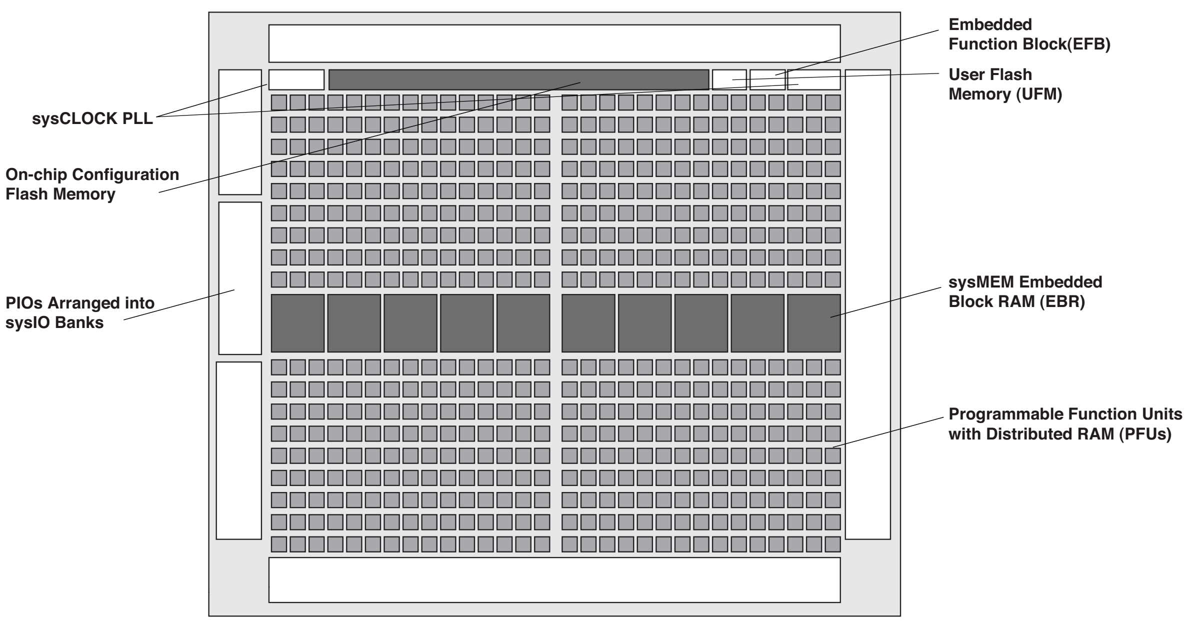
The MachXO2 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.

***Figure 2-1. Top View of the MachXO2-1200 Device***



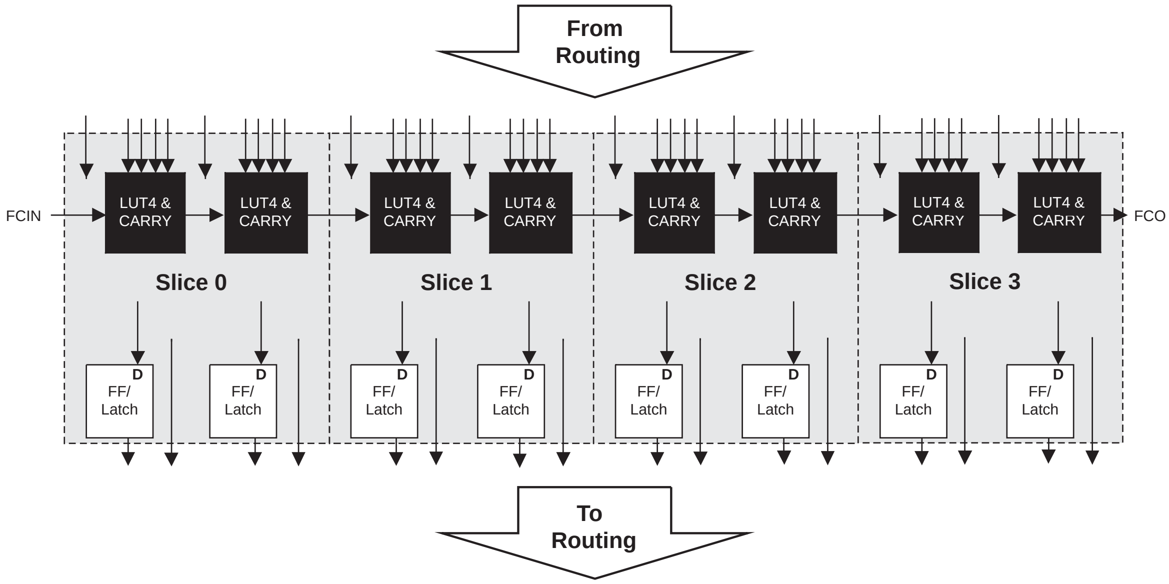

Note: MachXO2-256, and MachXO2-640/U are similar to MachXO2-1200. MachXO2-256 has a lower LUT count and no PLL or EBR blocks. MachXO2-640 has no PLL, a lower LUT count and two EBR blocks. MachXO2-640U has a lower LUT count, one PLL and seven EBR blocks.

***Figure 2-2. Top View of the MachXO2-4000 Device***




Note: MachXO2-1200U, MachXO2-2000/U and MachXO2-7000 are similar to MachXO2-4000. MachXO2-1200U and MachXO2-2000 have a lower LUT count, one PLL, and eight EBR blocks. MachXO2-2000U has a lower LUT count, two PLLs, and 10 EBR blocks. MachXO2-7000 has a higher LUT count, two PLLs, and 26 EBR blocks.

*Figure 2-3. PFU Block Diagram*




## Slices

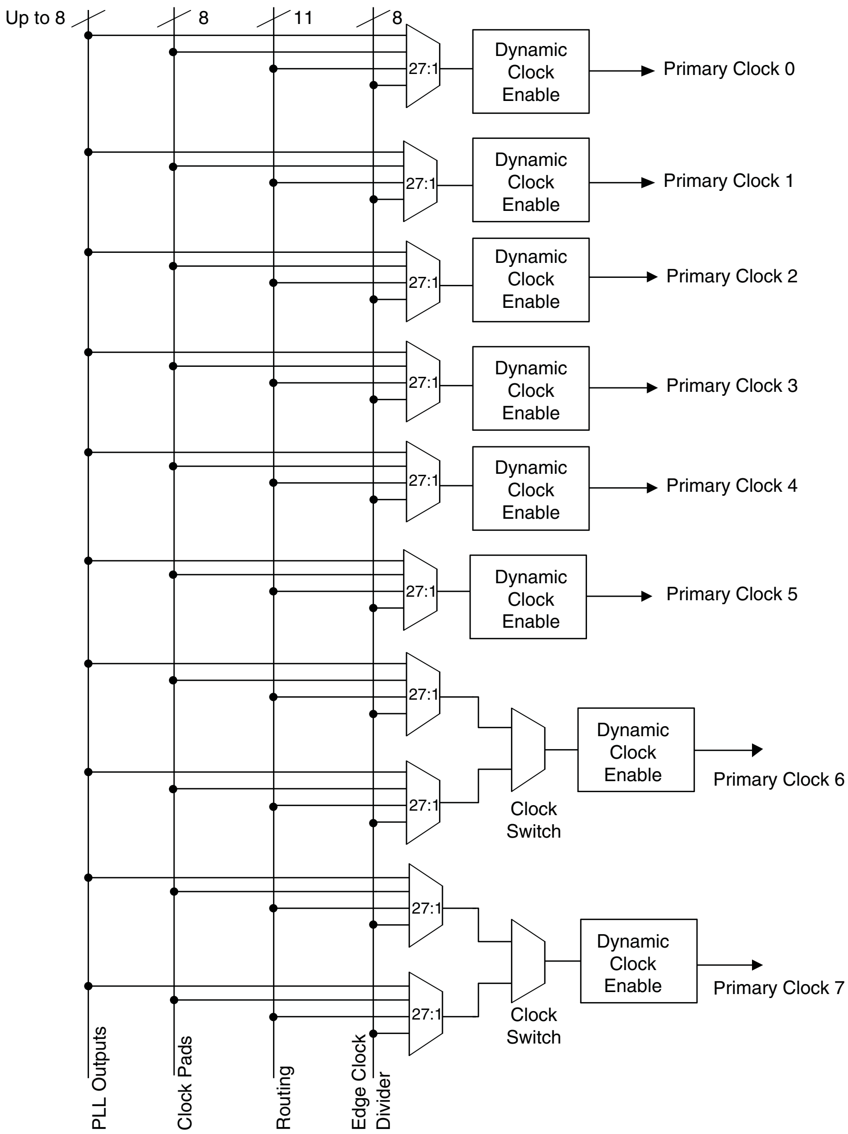
Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

*Table 2-1. Resources and Modes Available per Slice*

| | PFU Block | |
|---|---|---|
| **Slice** | **Resources** | **Modes** |
| Slice 0 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 1 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 2 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 3 | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.

*Figure 2-5. Primary Clocks for MachXO2 Devices*




Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO2 External Switching Characteristics table.

This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the $t_{LOCK}$ parameter has been satisfied.

The MachXO2 also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO2 PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the $t_{LOCK}$ parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

For more details on the PLL and the WISHBONE interface, see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

***Figure 2-7. PLL Diagram***

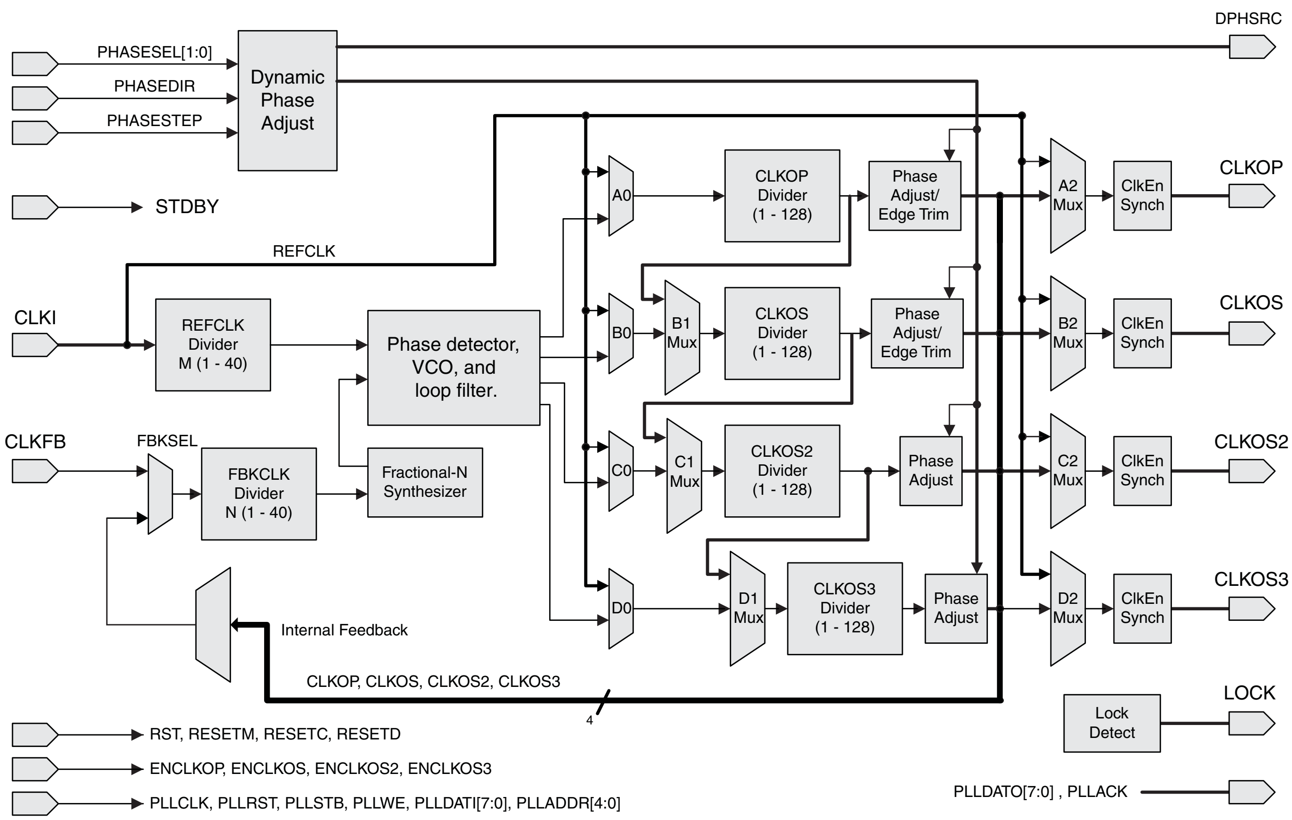



Table 2-4 provides signal descriptions of the PLL block.

***Table 2-4. PLL Signal Descriptions***

| Port Name | I/O | Description |
|---|---|---|
| CLKI | I | Input clock to PLL |
| CLKFB | I | Feedback clock |
| PHASESEL[1:0] | I | Select which output is affected by Dynamic Phase adjustment ports |
| PHASEDIR | I | Dynamic Phase adjustment direction |
| PHASESTEP | I | Dynamic Phase step – toggle shifts VCO phase adjust by one step. |

*Table 2-4. PLL Signal Descriptions (Continued)*

| Port Name | I/O | Description |
|---|---|---|
| CLKOP | O | Primary PLL output clock (with phase shift adjustment) |
| CLKOS | O | Secondary PLL output clock (with phase shift adjust) |
| CLKOS2 | O | Secondary PLL output clock2 (with phase shift adjust) |
| CLKOS3 | O | Secondary PLL output clock3 (with phase shift adjust) |
| LOCK | O | PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feedback signals. |
| DPHSRC | O | Dynamic Phase source – ports or WISHBONE is active |
| STDBY | I | Standby signal to power down the PLL |
| RST | I | PLL reset without resetting the M-divider. Active high reset. |
| RESETM | I | PLL reset - includes resetting the M-divider. Active high reset. |
| RESETC | I | Reset for CLKOS2 output divider only. Active high reset. |
| RESETD | I | Reset for CLKOS3 output divider only. Active high reset. |
| ENCLKOP | I | Enable PLL output CLKOP |
| ENCLKOS | I | Enable PLL output CLKOS when port is active |
| ENCLKOS2 | I | Enable PLL output CLKOS2 when port is active |
| ENCLKOS3 | I | Enable PLL output CLKOS3 when port is active |
| PLLCLK | I | PLL data bus clock input signal |
| PLLRST | I | PLL data bus reset. This resets only the data bus not any register values. |
| PLLSTB | I | PLL data bus strobe signal |
| PLLWE | I | PLL data bus write enable signal |
| PLLADDR [4:0] | I | PLL data bus address |
| PLLDATI [7:0] | I | PLL data bus data input |
| PLLDATO [7:0] | O | PLL data bus data output |
| PLLACK | O | PLL data bus acknowledge signal |

## sysMEM Embedded Block RAM Memory

The MachXO2-640/U and larger devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

### sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.

*Figure 2-8. sysMEM Memory Primitives*

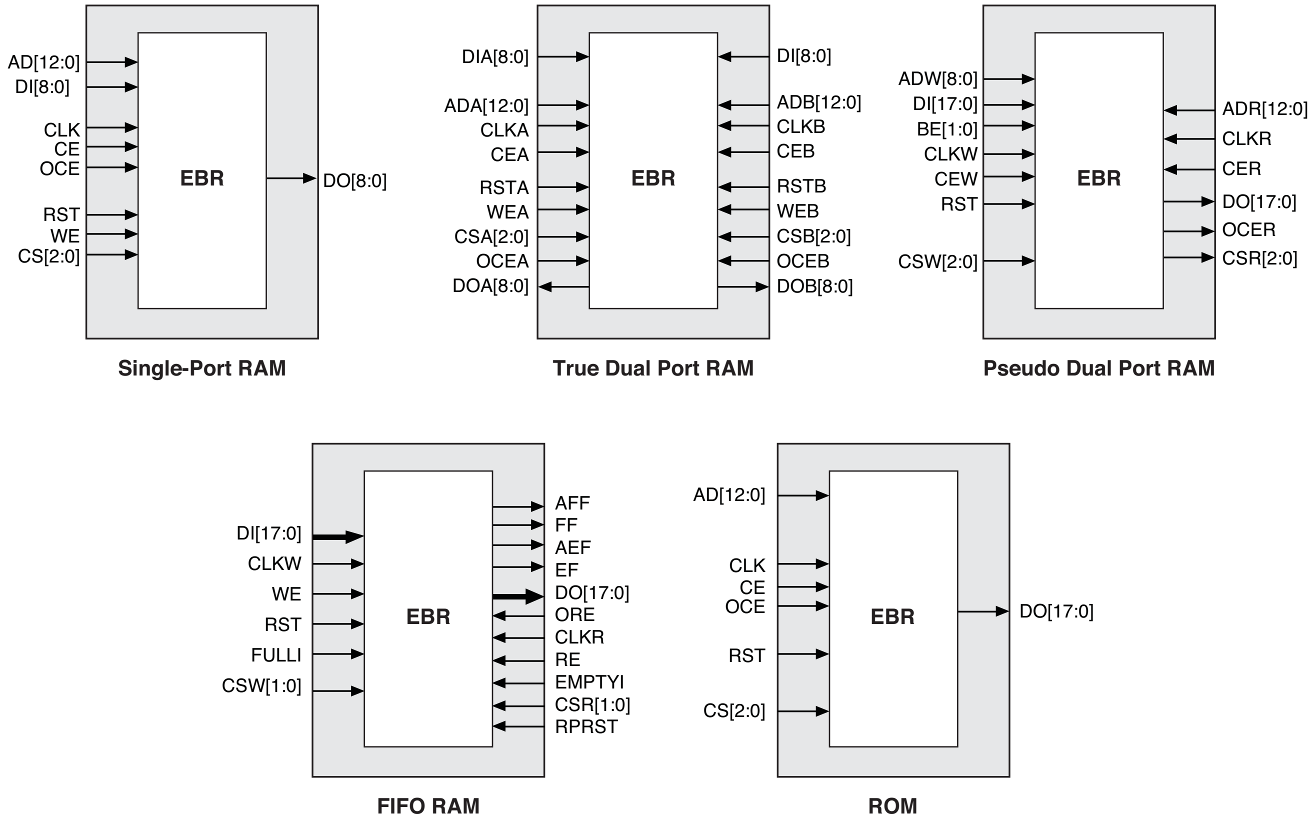



*Table 2-6. EBR Signal Descriptions*

| Port Name | Description | Active State |
|---|---|---|
| CLK | Clock | Rising Clock Edge |
| CE | Clock Enable | Active High |
| OCE[1] | Output Clock Enable | Active High |
| RST | Reset | Active High |
| BE[1] | Byte Enable | Active High |
| WE | Write Enable | Active High |
| AD | Address Bus | — |
| DI | Data In | — |
| DO | Data Out | — |
| CS | Chip Select | Active High |
| AFF | FIFO RAM Almost Full Flag | — |
| FF | FIFO RAM Full Flag | — |
| AEF | FIFO RAM Almost Empty Flag | — |
| EF | FIFO RAM Empty Flag | — |
| RPRST | FIFO RAM Read Pointer Reset | — |

1. Optional signals.
2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.

3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

### FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

***Table 2-7. Programmable FIFO Flag Ranges***

| Flag Name | Programming Range |
|---|---|
| Full (FF) | 1 to max (up to $2^N$-1) |
| Almost Full (AF) | 1 to Full-1 |
| Almost Empty (AE) | 1 to Full-1 |
| Empty (EF) | 0 |

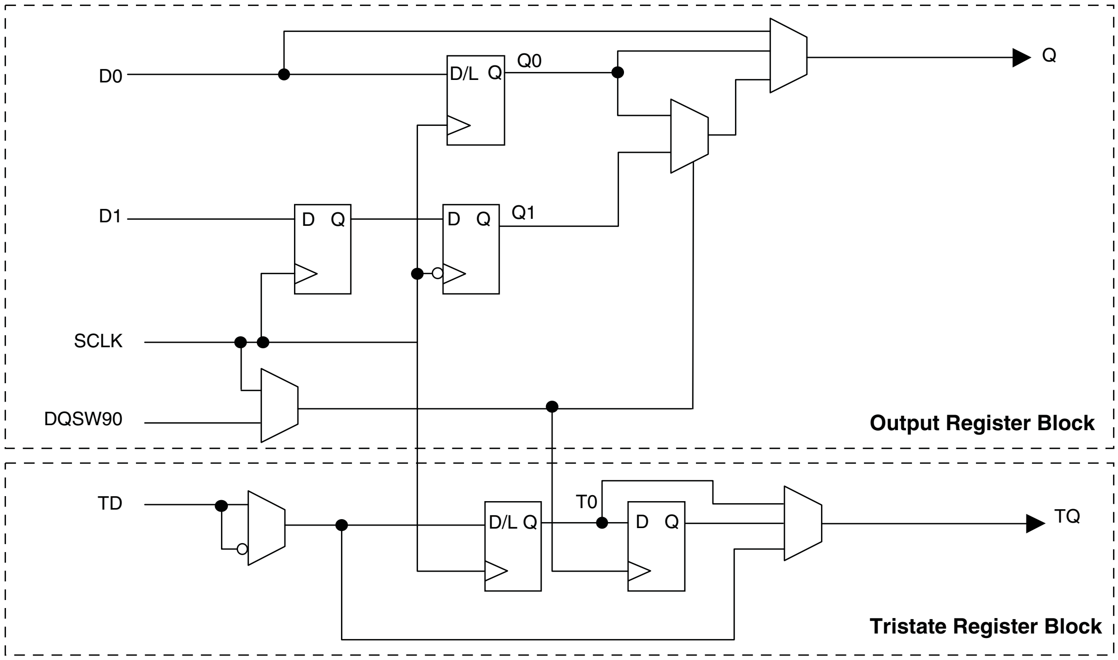
N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

### Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

*Figure 2-15. MachXO2 Output Register Block Diagram (PIO on the Right Edges)*




## Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

The tri-state register blocks on the right edge contain an additional register for DDR memory operation. In DDR memory mode, the register TS input is fed into another register that is clocked using the DQSW90 signal. The output of this register is used as a tri-state control.

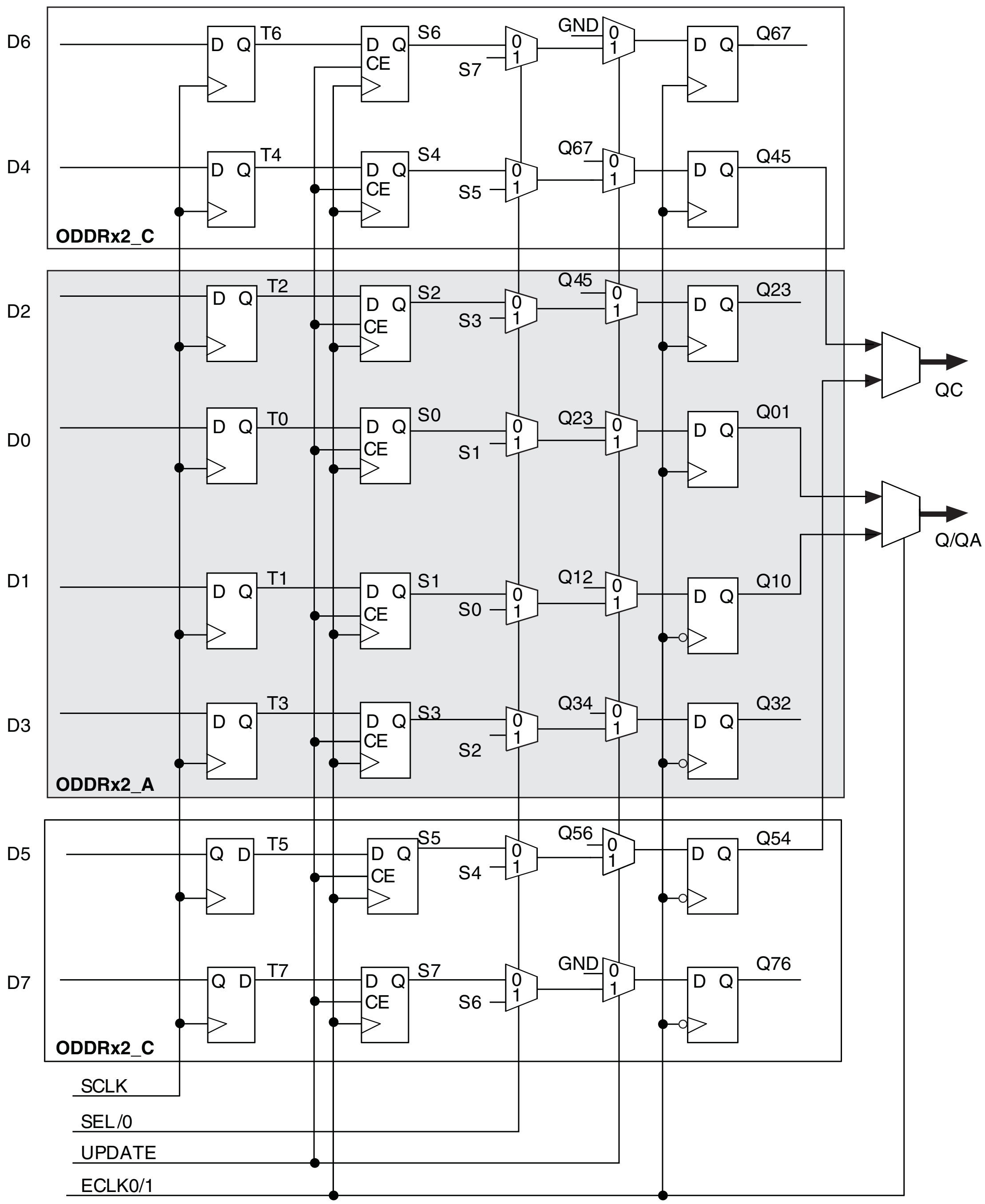
# Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

*Table 2-9. Input Gearbox Signal List*

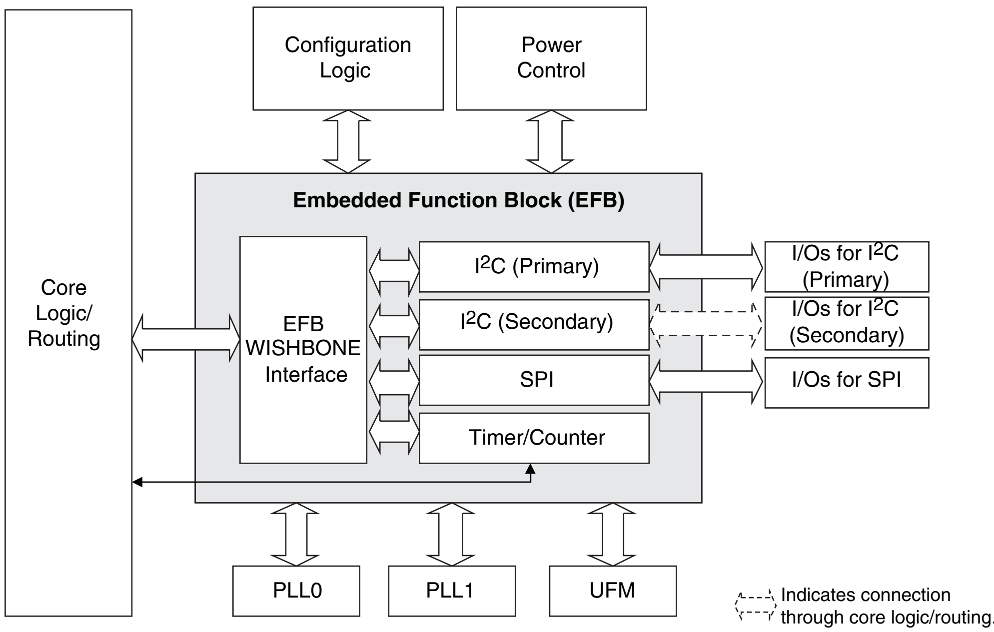
| Name | I/O Type | Description |
|---|---|---|
| D | Input | High-speed data input after programmable delay in PIO A input register block |
| ALIGNWD | Input | Data alignment signal from device core |
| SCLK | Input | Slow-speed system clock |
| ECLK[1:0] | Input | High-speed edge clock |
| RST | Input | Reset |
| Q[7:0] | Output | Low-speed data to device core:<br>Video RX(1:7): Q[6:0]<br>GDDRX4(1:8): Q[7:0]<br>GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7<br>GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3 |

*Figure 2-17. Output Gearbox*




More information on the output gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.

*Figure 2-20. Embedded Function Block Interface*




## Hardened I²C IP Core

Every MachXO2 device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I²C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface

# Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

## IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with $V_{CCIO}$ Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

## Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through $I^2C$ or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

1. Internal Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard $I^2C$ Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, MachXO2 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

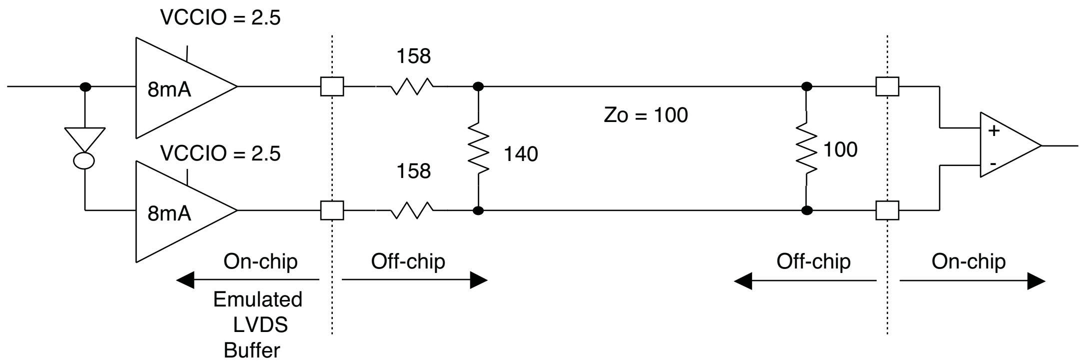
**TransFR (Transparent Field Reconfiguration)**

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

## LVDS Emulation

MachXO2 devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

***Figure 3-1. LVDS Using External Resistors (LVDS25E)***




Note: All resistors are ±1%.

***Table 3-1. LVDS25E DC Conditions***

**Over Recommended Operating Conditions**

| Parameter | Description | Typ. | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ohms |
| $R_S$ | Driver series resistor | 158 | Ohms |
| $R_P$ | Driver parallel resistor | 140 | Ohms |
| $R_T$ | Receiver termination | 100 | Ohms |
| $V_{OH}$ | Output high voltage | 1.43 | V |
| $V_{OL}$ | Output low voltage | 1.07 | V |
| $V_{OD}$ | Output differential voltage | 0.35 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 100.5 | Ohms |
| $I_{DC}$ | DC output current | 6.03 | mA |

## MachXO2 External Switching Characteristics – ZE Devices[1, 2, 3, 4, 5, 6, 7]

**Over Recommended Operating Conditions**

| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Clocks** | | | | | | | | | |
| **Primary Clocks** | | | | | | | | | |
| $f_{MAX\_PRI}$[8] | Frequency for Primary Clock Tree | All MachXO2 devices | — | 150 | — | 125 | — | 104 | MHz |
| $t_{W\_PRI}$ | Clock Pulse Width for Primary Clock | All MachXO2 devices | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| $t_{SKEW\_PRI}$ | Primary Clock Skew Within a Device | MachXO2-256ZE | — | 1250 | — | 1272 | — | 1296 | ps |
| | | MachXO2-640ZE | — | 1161 | — | 1183 | — | 1206 | ps |
| | | MachXO2-1200ZE | — | 1213 | — | 1267 | — | 1322 | ps |
| | | MachXO2-2000ZE | — | 1204 | — | 1250 | — | 1296 | ps |
| | | MachXO2-4000ZE | — | 1195 | — | 1233 | — | 1269 | ps |
| | | MachXO2-7000ZE | — | 1243 | — | 1268 | — | 1296 | ps |
| **Edge Clock** | | | | | | | | | |
| $f_{MAX\_EDGE}$[8] | Frequency for Edge Clock | MachXO2-1200 and larger devices | — | 210 | — | 175 | — | 146 | MHz |
| **Pin-LUT-Pin Propagation Delay** | | | | | | | | | |
| $t_{PD}$ | Best case propagation delay through one LUT-4 | All MachXO2 devices | — | 9.35 | — | 9.78 | — | 10.21 | ns |
| **General I/O Pin Parameters (Using Primary Clock without PLL)** | | | | | | | | | |
| $t_{CO}$ | Clock to Output – PIO Output Register | MachXO2-256ZE | — | 10.46 | — | 10.86 | — | 11.25 | ns |
| | | MachXO2-640ZE | — | 10.52 | — | 10.92 | — | 11.32 | ns |
| | | MachXO2-1200ZE | — | 11.24 | — | 11.68 | — | 12.12 | ns |
| | | MachXO2-2000ZE | — | 11.27 | — | 11.71 | — | 12.16 | ns |
| | | MachXO2-4000ZE | — | 11.28 | — | 11.78 | — | 12.28 | ns |
| | | MachXO2-7000ZE | — | 11.22 | — | 11.76 | — | 12.30 | ns |
| $t_{SU}$ | Clock to Data Setup – PIO Input Register | MachXO2-256ZE | –0.21 | — | –0.21 | — | –0.21 | — | ns |
| | | MachXO2-640ZE | –0.22 | — | –0.22 | — | –0.22 | — | ns |
| | | MachXO2-1200ZE | –0.25 | — | –0.25 | — | –0.25 | — | ns |
| | | MachXO2-2000ZE | –0.27 | — | –0.27 | — | –0.27 | — | ns |
| | | MachXO2-4000ZE | –0.31 | — | –0.31 | — | –0.31 | — | ns |
| | | MachXO2-7000ZE | –0.33 | — | –0.33 | — | –0.33 | — | ns |
| $t_H$ | Clock to Data Hold – PIO Input Register | MachXO2-256ZE | 3.96 | — | 4.25 | — | 4.65 | — | ns |
| | | MachXO2-640ZE | 4.01 | — | 4.31 | — | 4.71 | — | ns |
| | | MachXO2-1200ZE | 3.95 | — | 4.29 | — | 4.73 | — | ns |
| | | MachXO2-2000ZE | 3.94 | — | 4.29 | — | 4.74 | — | ns |
| | | MachXO2-4000ZE | 3.96 | — | 4.36 | — | 4.87 | — | ns |
| | | MachXO2-7000ZE | 3.93 | — | 4.37 | — | 4.91 | — | ns |

| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **LPDDR**[9, 12] | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only.[13] | — | 0.349 | — | 0.381 | — | 0.396 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.665 | — | 0.630 | — | 0.613 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM LPDDR Serial Data Speed | | — | 120 | — | 110 | — | 96 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 60 | — | 55 | — | 48 | MHz |
| $f_{LPDDR}$ | LPDDR Data Transfer Rate | | 0 | 120 | 0 | 110 | 0 | 96 | Mbps |
| **DDR**[9, 12] | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only.[13] | — | 0.347 | — | 0.374 | — | 0.393 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.665 | — | 0.637 | — | 0.616 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM DDR Serial Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 58 | — | 49 | MHz |
| $f_{MEM\_DDR}$ | MEM DDR Data Transfer Rate | | N/A | 140 | N/A | 116 | N/A | 98 | Mbps |
| **DDR2**[9, 12] | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only.[13] | — | 0.372 | — | 0.394 | — | 0.410 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.690 | — | 0.658 | — | 0.618 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM DDR Serial Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 58 | — | 49 | MHz |
| $f_{MEM\_DDR2}$ | MEM DDR2 Data Transfer Rate | | N/A | 140 | N/A | 116 | N/A | 98 | Mbps |

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
7. The $t_{SU\_DEL}$ and $t_{H\_DEL}$ values use the SCLK_ZERHOLD default step size. Each step is 167 ps (–3), 182 ps (–2), 195 ps (–1).
8. This number for general purpose usage. Duty cycle tolerance is +/–10%.
9. Duty cycle is +/– 5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

## Signal Descriptions (Cont.)

| Signal Name | I/O | Descriptions |
|---|---|---|
| INITN | I/O | Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, or when reserved as INITn in user mode, this pin has an active pull-up. |
| DONE | I/O | Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress. During configuration, or when reserved as DONE in user mode, this pin has an active pull-up. |
| MCLK/CCLK | I/O | Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes. |
| SN | I | Slave SPI active low chip select input. |
| CSSPIN | I/O | Master SPI active low chip select output. |
| SI/SPISI | I/O | Slave SPI serial data input and master SPI serial data output. |
| SO/SPISO | I/O | Slave SPI serial data output and master SPI serial data input. |
| SCL | I/O | Slave $I^2C$ clock input and master $I^2C$ clock output. |
| SDA | I/O | Slave $I^2C$ data input and master $I^2C$ data output. |

| | MachXO2-1200 | | | | | MachXO2-1200U |
|---|---|---|---|---|---|---|
| | 100 TQFP | 132 csBGA | 144 TQFP | 25 WLCSP | 32 QFN[1] | 256 ftBGA |
| **General Purpose I/O per Bank** | | | | | | |
| Bank 0 | 18 | 25 | 27 | 11 | 9 | 50 |
| Bank 1 | 21 | 26 | 26 | 0 | 2 | 52 |
| Bank 2 | 20 | 28 | 28 | 7 | 9 | 52 |
| Bank 3 | 20 | 25 | 26 | 0 | 2 | 16 |
| Bank 4 | 0 | 0 | 0 | 0 | 0 | 16 |
| Bank 5 | 0 | 0 | 0 | 0 | 0 | 20 |
| Total General Purpose Single Ended I/O | 79 | 104 | 107 | 18 | 22 | 206 |
| | | | | | | |
| **Differential I/O per Bank** | | | | | | |
| Bank 0 | 9 | 13 | 14 | 5 | 4 | 25 |
| Bank 1 | 10 | 13 | 13 | 0 | 1 | 26 |
| Bank 2 | 10 | 14 | 14 | 2 | 4 | 26 |
| Bank 3 | 10 | 12 | 13 | 0 | 1 | 8 |
| Bank 4 | 0 | 0 | 0 | 0 | 0 | 8 |
| Bank 5 | 0 | 0 | 0 | 0 | 0 | 10 |
| Total General Purpose Differential I/O | 39 | 52 | 54 | 7 | 10 | 103 |
| | | | | | | |
| **Dual Function I/O** | 31 | 33 | 33 | 18 | 22 | 33 |
| **High-speed Differential I/O** | | | | | | |
| Bank 0 | 4 | 7 | 7 | 0 | 0 | 14 |
| **Gearboxes** | | | | | | |
| Number of 7:1 or 8:1 Output Gearbox Available (Bank 0) | 4 | 7 | 7 | 0 | 0 | 14 |
| Number of 7:1 or 8:1 Input Gearbox Available (Bank 2) | 5 | 7 | 7 | 0 | 2 | 14 |
| **DQS Groups** | | | | | | |
| Bank 1 | 1 | 2 | 2 | 0 | 0 | 2 |
| | | | | | | |
| **VCCIO Pins** | | | | | | |
| Bank 0 | 2 | 3 | 3 | 1 | 2 | 4 |
| Bank 1 | 2 | 3 | 3 | 0 | 1 | 4 |
| Bank 2 | 2 | 3 | 3 | 1 | 2 | 4 |
| Bank 3 | 3 | 3 | 3 | 0 | 1 | 1 |
| Bank 4 | 0 | 0 | 0 | 0 | 0 | 2 |
| Bank 5 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | | | | | |
| VCC | 2 | 4 | 4 | 2 | 2 | 8 |
| GND | 8 | 10 | 12 | 2 | 2 | 24 |
| NC | 1 | 1 | 8 | 0 | 0 | 1 |
| Reserved for Configuration | 1 | 1 | 1 | 1 | 1 | 1 |
| Total Count of Bonded Pins | 100 | 132 | 144 | 25 | 32 | 256 |

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000UHC-4FG484C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-2000UHC-5FG484C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-2000UHC-6FG484C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000HC-4QN84C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000HC-5QN84C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000HC-6QN84C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000HC-4MG132C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HC-5MG132C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HC-6MG132C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HC-4TG144C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HC-5TG144C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HC-6TG144C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HC-4BG256C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HC-5BG256C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HC-6BG256C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HC-4FTG256C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HC-5FTG256C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HC-6FTG256C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HC-4BG332C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HC-5BG332C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HC-6BG332C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HC-4FG484C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HC-5FG484C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HC-6FG484C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000HE-6BG332C | 4320 | 1.2 V | –6 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HE-4FG484C | 4320 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HE-5FG484C | 4320 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HE-6FG484C | 4320 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000HE-4TG144C | 6864 | 1.2 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000HE-5TG144C | 6864 | 1.2 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000HE-6TG144C | 6864 | 1.2 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000HE-4BG256C | 6864 | 1.2 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000HE-5BG256C | 6864 | 1.2 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000HE-6BG256C | 6864 | 1.2 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000HE-4FTG256C | 6864 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000HE-5FTG256C | 6864 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000HE-6FTG256C | 6864 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000HE-4BG332C | 6864 | 1.2 V | –4 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000HE-5BG332C | 6864 | 1.2 V | –5 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000HE-6BG332C | 6864 | 1.2 V | –6 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000HE-4FG484C | 6864 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000HE-5FG484C | 6864 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000HE-6FG484C | 6864 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000HC-4QN84I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000HC-5QN84I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000HC-6QN84I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000HC-4TG144I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HC-5TG144I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HC-6TG144I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HC-4MG132I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HC-5MG132I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HC-6MG132I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HC-4BG256I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HC-5BG256I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HC-6BG256I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HC-4FTG256I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HC-5FTG256I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HC-6FTG256I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HC-4BG332I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HC-5BG332I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HC-6BG332I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HC-4FG484I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HC-5FG484I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HC-6FG484I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000HC-4TG144I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HC-5TG144I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HC-6TG144I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HC-4BG256I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HC-5BG256I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HC-6BG256I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HC-4FTG256I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HC-5FTG256I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HC-6FTG256I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HC-4BG332I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HC-5BG332I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HC-6BG332I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HC-4FG400I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 400 | IND |
| LCMXO2-7000HC-5FG400I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 400 | IND |
| LCMXO2-7000HC-6FG400I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 400 | IND |
| LCMXO2-7000HC-4FG484I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HC-5FG484I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HC-6FG484I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | IND |

| Date | Version | Section | Change Summary |
| --- | --- | --- | --- |
| January 2013 | 02.0 | Introduction | Updated the total number IOs to include JTAGENB. |
| | | Architecture | Supported Output Standards table – Added 3.3 $V_{CCIO}$ (Typ.) to LVDS row. |
| | | | Changed SRAM CRC Error Detection to Soft Error Detection. |
| | | DC and Switching Characteristics | Power Supply Ramp Rates table – Updated Units column for $t_{RAMP}$ symbol. |
| | | | Added new Maximum sysIO Buffer Performance table. |
| | | | sysCLOCK PLL Timing table – Updated Min. column values for $f_{IN}$, $f_{OUT}$, $f_{OUT2}$ and $f_{PFD}$ parameters. Added $t_{SPO}$ parameter. Updated footnote 6. |
| | | | MachXO2 Oscillator Output Frequency table – Updated symbol name for $t_{STABLEOSC}$. |
| | | | DC Electrical Characteristics table – Updated conditions for $I_{IL}$, $I_{IH}$ symbols. |
| | | | Corrected parameters tDQVBS and tDQVAS |
| | | | Corrected MachXO2 ZE parameters tDVADQ and tDVEDQ |
| | | Pinout Information | Included the MachXO2-4000HE 184 csBGA package. |
| | | Ordering Information | Updated part number. |
| April 2012 | 01.9 | Architecture | Removed references to TN1200. |
| | | Ordering Information | Updated the Device Status portion of the MachXO2 Part Number Description to include the 50 parts per reel for the WLCSP package. |
| | | | Added new part number and footnote 2 for LCMXO2-1200ZE-1UWG25ITR50. |
| | | | Updated footnote 1 for LCMXO2-1200ZE-1UWG25ITR. |
| | | Supplemental Information | Removed references to TN1200. |
| March 2012 | 01.8 | Introduction | Added 32 QFN packaging information to Features bullets and MachXO2 Family Selection Guide table. |
| | | DC and Switching Characteristics | Changed ‘STANDBY’ to ‘USERSTDBY’ in Standby Mode timing diagram. |
| | | Pinout Information | Removed footnote from Pin Information Summary tables. |
| | | | Added 32 QFN package to Pin Information Summary table. |
| | | Ordering Information | Updated Part Number Description and Ordering Information tables for 32 QFN package. |
| | | | Updated topside mark diagram in the Ordering Information section. |