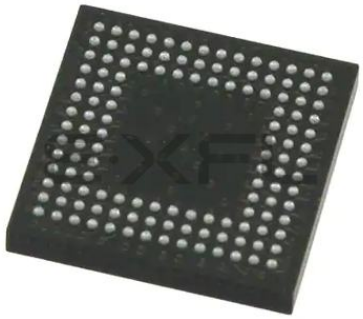
Lattice Semiconductor Corporation - LCMXO2-4000HC-4MG132I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	540
Number of Logic Elements/Cells	4320
Total RAM Bits	94208
Number of I/O	104
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-4000hc-4mg132i

Table 2-4. PLL Signal Descriptions (Continued)

Port Name	I/O	Description
CLKOP	O	Primary PLL output clock (with phase shift adjustment)
CLKOS	O	Secondary PLL output clock (with phase shift adjust)
CLKOS2	O	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	O	Secondary PLL output clock3 (with phase shift adjust)
LOCK	O	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feedback signals.
DPHSRC	O	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset - includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	O	PLL data bus data output
PLLACK	O	PLL data bus acknowledge signal

sysMEM Embedded Block RAM Memory

The MachXO2-640/U and larger devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.

Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO2 devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO2 devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

The MachXO2-640U, MachXO2-1200/U and higher density devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these higher density devices have on-chip differential termination and also provide PCI support.

PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Table 2-8. PIO Signal List

Pin Name	I/O Type	Description
CE	Input	Clock Enable
D	Input	Pin input from sysIO buffer.
INDD	Output	Register bypassed input.
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysIO Buffer
TQ	Output	Tri-state output signals to sysIO Buffer
DQSR90[1]	Input	DQS shift 90-degree read clock
DQSW90[1]	Input	DQS shift 90-degree write clock
DDRCLKPOL[1]	Input	DDR input register polarity control signal from DQS
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

1. Available in PIO on right edge only.

Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition to this functionality, the input register blocks for the PIOs on the right edge include built-in logic to interface to DDR memory.

Figure 2-12 shows the input register block for the PIOs located on the left, top and bottom edges. Figure 2-13 shows the input register block for the PIOs on the right edge.

Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

Figure 2-18. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 Banks

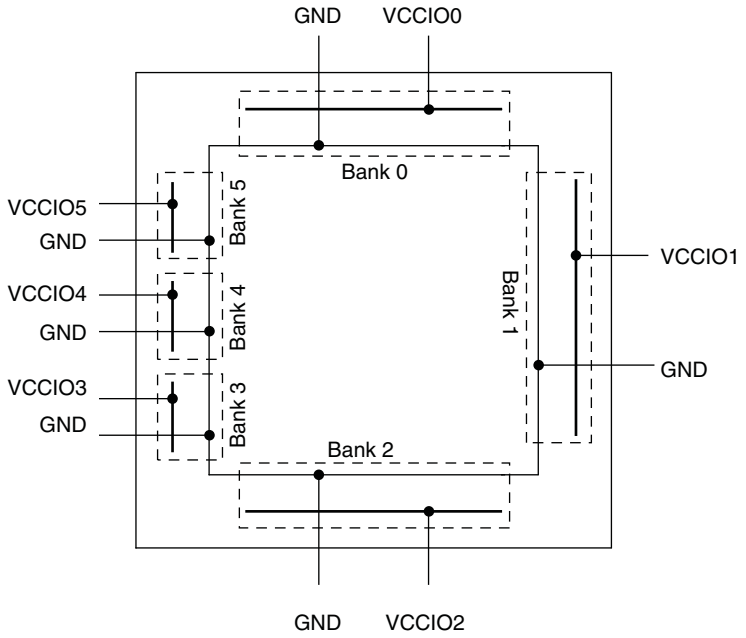


Figure 2-19. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks

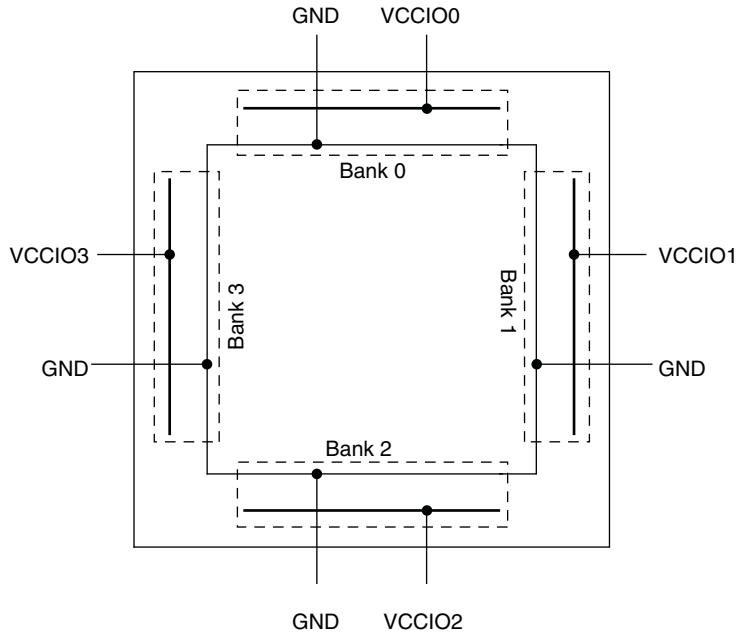


Figure 2-21. I²C Core Block Diagram

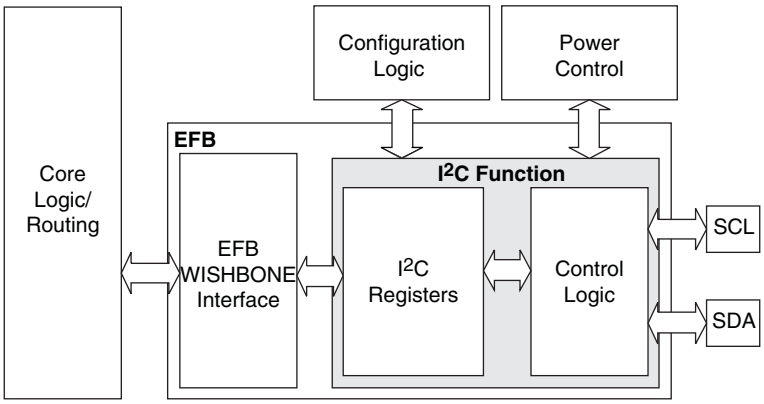


Table 2-15 describes the signals interfacing with the I²C cores.

Table 2-15. I²C Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I²C core. The signal is an output if the I²C core is in master mode. The signal is an input if the I²C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device.
i2c_sda	Bi-directional	Bi-directional data line of the I²C core. The signal is an output when data is transmitted from the I²C core. The signal is an input when data is received into the I²C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device.
i2c_irqo	Output	Interrupt request output signal of the I²C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I²C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.

Hardened SPI IP Core

Every MachXO2 device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO2 devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface

For more details on these embedded functions, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

User Flash Memory (UFM)

MachXO2-640/U and higher density devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I^2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

Standby Mode and Power Saving Options

MachXO2 devices are available in three options for maximum flexibility: ZE, HC and HE devices. The ZE devices have ultra low static and dynamic power consumption. These devices use a 1.2 V core voltage that further reduces power consumption. The HC and HE devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the HE devices operate at 1.2 V V_{CC}.

MachXO2 devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO2 devices support an ultra low power Stand-by mode. While most of these features are available in all three device types, these features are mainly intended for use with MachXO2 ZE devices to manage power consumption.

In the stand-by mode the MachXO2 devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I^2C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO2 devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

sysIO Single-Ended DC Electrical Characteristics[1, 2]

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max.[4] (mA)	I_{OH} Max.[4] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3 LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
							16	–16
							24	–24
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
							16	–16
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.5	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.2	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} – 0.4	4	–2
							8	–6
					0.2	V_{CCIO} – 0.2	0.1	–0.1
PCI	–0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	–0.5
SSTL25 Class I	–0.3	V_{REF} – 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	8	8
SSTL25 Class II	–0.3	V_{REF} – 0.18	V_{REF} + 0.18	3.6	NA	NA	NA	NA
SSTL18 Class I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	3.6	0.40	V_{CCIO} - 0.40	8	8
SSTL18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	3.6	NA	NA	NA	NA
HSTL18 Class I	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	V_{CCIO} - 0.40	8	8
HSTL18 Class II	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS25R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS12R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain

BLVDS

The MachXO2 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

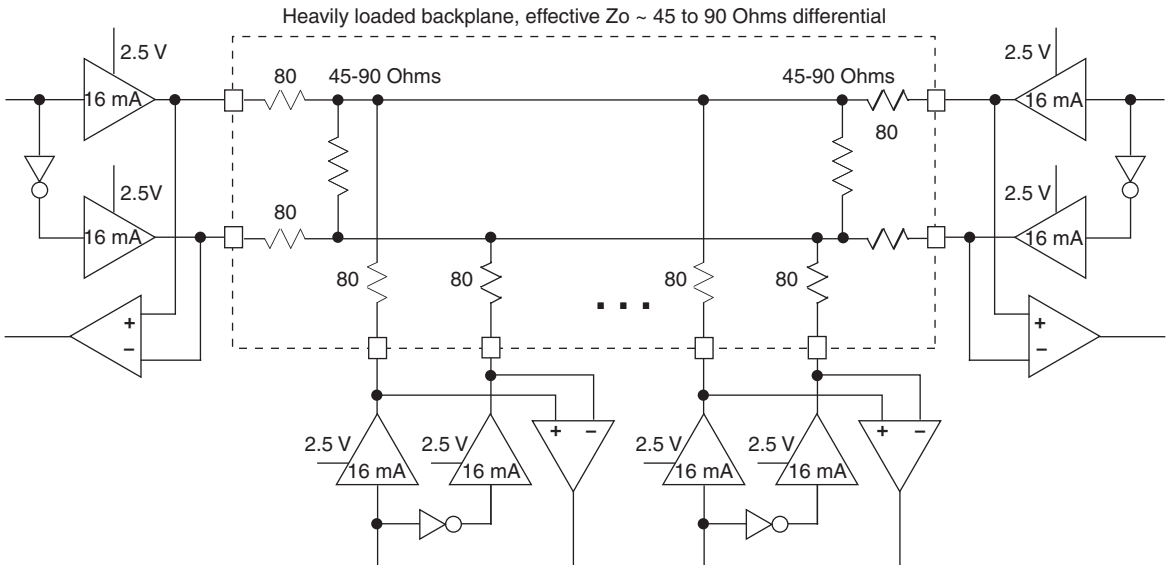


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	20	20	Ohms
R_S	Driver series resistance	80	80	Ohms
R_{TLEFT}	Left end termination	45	90	Ohms
R_{TRIGHT}	Right end termination	45	90	Ohms
V_{OH}	Output high voltage	1.376	1.480	V
V_{OL}	Output low voltage	1.124	1.020	V
V_{OD}	Output differential voltage	0.253	0.459	V
V_{CM}	Output common mode voltage	1.250	1.250	V
I_{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.

LVPECL

The MachXO2 family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

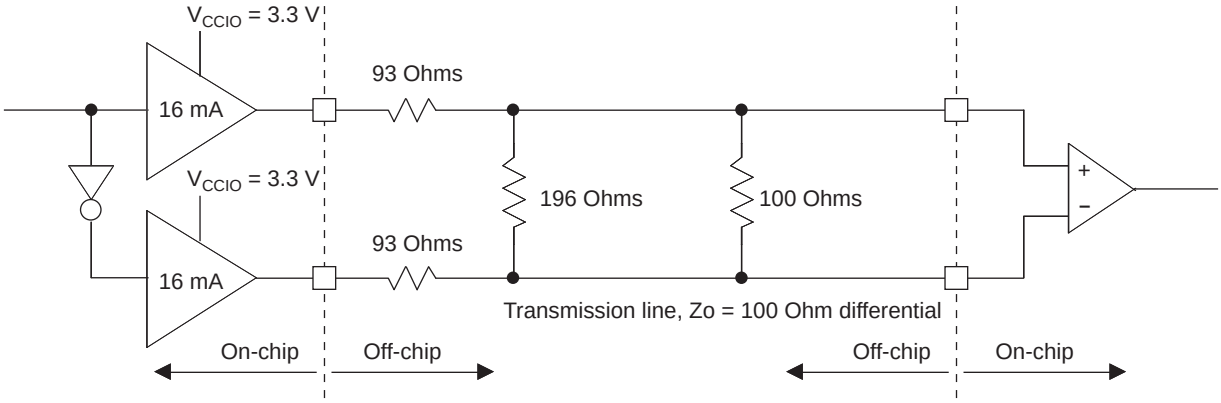


Table 3-3. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	93	Ohms
R_P	Driver parallel resistor	196	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	2.05	V
V_{OL}	Output low voltage	1.25	V
V_{OD}	Output differential voltage	0.80	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	12.11	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only.[11]	—	0.290	—	0.320	—	0.345	UI
t_{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	0.703	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only.[11]	0.233	—	0.219	—	0.198	—	ns
t_{HO}	Input Data Hold After ECLK		0.287	—	0.287	—	0.344	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1)[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only.[11]	—	0.290	—	0.320	—	0.345	UI
t_{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	0.703	—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	All MachXO2 devices, all sides.	—	0.520	—	0.550	—	0.580	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.520	—	0.550	—	0.580	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK frequency		—	150	—	125	—	104	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	All MachXO2 devices, all sides.	1.210	—	1.510	—	1.870	—	ns
t_{DVA}	Output Data Valid After CLK Output		1.210	—	1.510	—	1.870	—	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		—	150	—	125	—	104	MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.349	—	0.381	—	0.396	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.630	—	0.613	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM LPDDR Serial Data Speed		—	120	—	110	—	96	Mbps
f_{SCLK}	SCLK Frequency		—	60	—	55	—	48	MHz
f_{LPDDR}	LPDDR Data Transfer Rate		0	120	0	110	0	96	Mbps
DDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.347	—	0.374	—	0.393	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.637	—	0.616	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f_{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f_{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps
DDR2[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.372	—	0.394	—	0.410	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.690	—	0.658	—	0.618	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f_{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f_{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
7. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 167 ps (–3), 182 ps (–2), 195 ps (–1).
8. This number for general purpose usage. Duty cycle tolerance is +/–10%.
9. Duty cycle is +/– 5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

Figure 3-9. GDDR71 Video Timing Waveforms

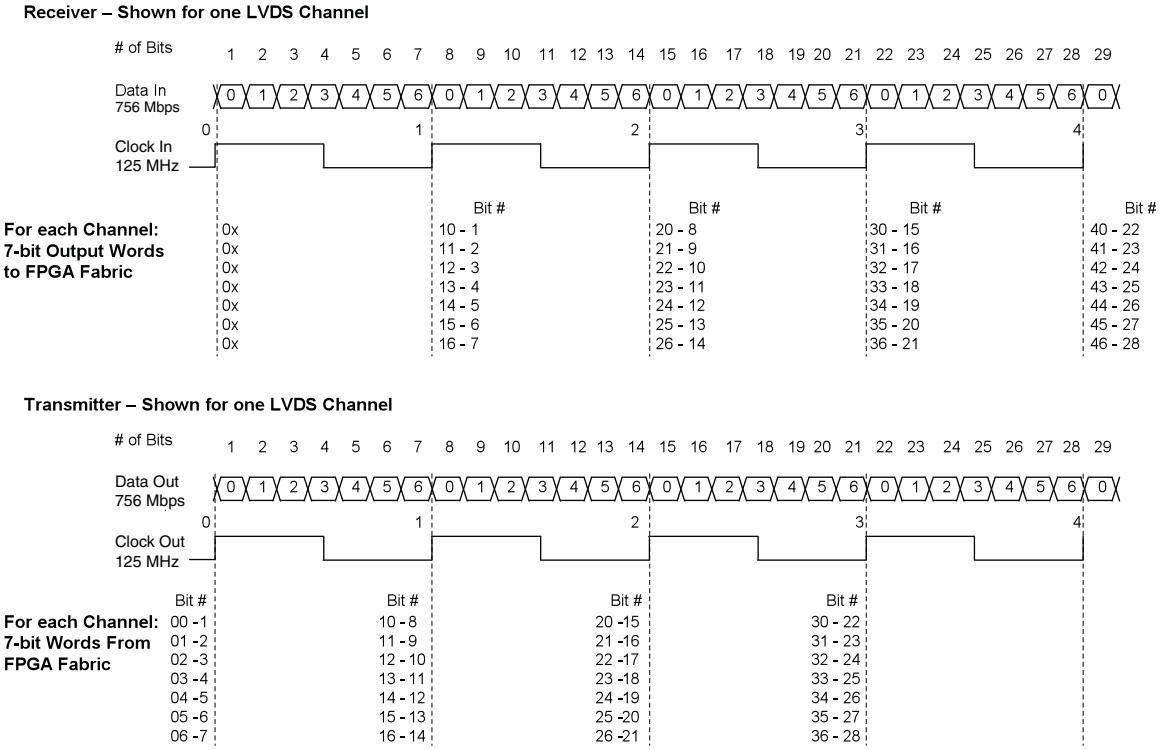


Figure 3-10. Receiver GDDR71_RX. Waveforms

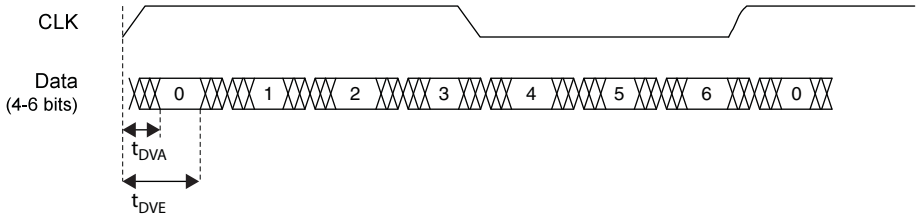
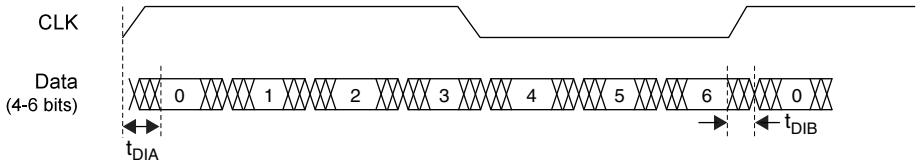


Figure 3-11. Transmitter GDDR71_TX. Waveforms



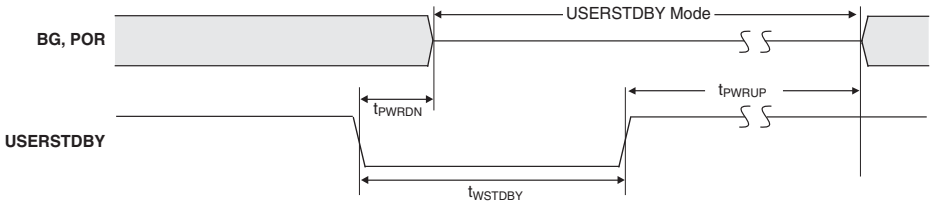
MachXO2 Oscillator Output Frequency

Symbol	Parameter	Min.	Typ.	Max	Units
f_{MAX}	Oscillator Output Frequency (Commercial Grade Devices, 0 to 85°C)	125.685	133	140.315	MHz
	Oscillator Output Frequency (Industrial Grade Devices, –40 °C to 100 °C)	124.355	133	141.645	MHz
t_{DT}	Output Clock Duty Cycle	43	50	57	%
t_{OPJIT}[1]	Output Clock Period Jitter	0.01	0.012	0.02	UIPP
$t_{STABLEOSC}$	STDBY Low to Oscillator Stable	0.01	0.05	0.1	µs

1. Output Clock Period Jitter specified at 133 MHz. The values for lower frequencies will be smaller UIPP. The typical value for 133 MHz is 95 ps and for 2.08 MHz the typical value is 1.54 ns.

MachXO2 Standby Mode Timing – HC/HE Devices

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	USERSTDBY High to Stop	All	—	—	9	ns
t_{PWRUP}	USERSTDBY Low to Power Up	LCMXO2-256		—		µs
		LCMXO2-640		—		µs
		LCMXO2-640U		—		µs
		LCMXO2-1200	20	—	50	µs
		LCMXO2-1200U		—		µs
		LCMXO2-2000		—		µs
		LCMXO2-2000U		—		µs
		LCMXO2-4000		—		µs
		LCMXO2-7000		—		µs
t_{WSTDBY}	USERSTDBY Pulse Width	All	18	—	—	ns



MachXO2 Standby Mode Timing – ZE Devices

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	USERSTDBY High to Stop	All	—	—	13	ns
t_{PWRUP}	USERSTDBY Low to Power Up	LCMXO2-256		—		µs
		LCMXO2-640		—		µs
		LCMXO2-1200	20	—	50	µs
		LCMXO2-2000		—		µs
		LCMXO2-4000		—		µs
		LCMXO2-7000		—		µs
t_{WSTDBY}	USERSTDBY Pulse Width	All	19	—	—	ns
$t_{BNDGAPSTBL}$	USERSTDBY High to Bandgap Stable	All	—	—	15	ns

Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, or when reserved as INITn in user mode, this pin has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress. During configuration, or when reserved as DONE in user mode, this pin has an active pull-up.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.
SCL	I/O	Slave I^2C clock input and master I^2C clock output.
SDA	I/O	Slave I^2C data input and master I^2C data output.

MachXO2 Family Data Sheet Ordering Information

MachXO2 Part Number Description

LCMXO2 – XXXX X X X – X XXXXXX X XX XX

Device Family
MachXO2 PLD

Logic Capacity
256 = 256 LUTs
640 = 640 LUTs
1200 = 1280 LUTs
2000 = 2112 LUTs
4000 = 4320 LUTs
7000 = 6864 LUTs

I/O Count
Blank = Standard Device
U = Ultra High I/O Device

Power/Performance
Z = Low Power
H = High Performance

Supply Voltage
C = 2.5 V / 3.3 V
E = 1.2 V

Speed
1 = Slowest
2
3 = Fastest
} Low Power

4 = Slowest
5
6 = Fastest
} High Performance

Device Status
Blank = Production Device
ES = Engineering Sample
R1 = Production Release 1 Device
1K = WLCSP Package, 1,000 parts per reel

Shipping Method
Blank = Trays
TR = Tape and Reel

Grade
C = Commercial
I = Industrial

Package
UWG25 = 25-Ball Halogen-Free WLCSP (0.4 mm Pitch)
SG32 = 32-Pin Halogen-Free QFN (0.5 mm Pitch)
SG48 = 48-Pin Halogen-Free QFN (0.5 mm Pitch)
UWG49 = 49-ball Halogen-Free WLCSP (0.4 mm Pitch)
UMG64 = 64-Ball Halogen-Free ucBGA (0.4 mm Pitch)
QN84 = 84-Pin Halogen-Free QFN (0.5 mm Pitch)
TG100 = 100-Pin Halogen-Free TQFP
TG144 = 144-Pin Halogen-Free TQFP
MG132 = 132-Ball Halogen-Free csBGA (0.5 mm Pitch)
MG184 = 184-Ball Halogen-Free csBGA (0.5 mm Pitch)
BG256 = 256-Ball Halogen-Free caBGA (0.8 mm Pitch)
FTG256 = 256-Ball Halogen-Free ftBGA (1.0 mm Pitch)
BG332 = 332-Ball Halogen-Free caBGA (0.8 mm Pitch)
FG484 = 484-Ball Halogen-Free fpBGA (1.0 mm Pitch)

* 48-pin QFN information is 'Advanced'.

Ordering Information

MachXO2 devices have top-side markings, for commercial and industrial grades, as shown below:

Notes:

1. Markings are abbreviated for small packages.

2. See PCN 05A-12 for information regarding a change to the top-side mark logo.

High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100C	2112	1.2 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-5TG100C	2112	1.2 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-6TG100C	2112	1.2 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-4TG144C	2112	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-5TG144C	2112	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-6TG144C	2112	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-4MG132C	2112	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-5MG132C	2112	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-6MG132C	2112	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-4BG256C	2112	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-5BG256C	2112	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-6BG256C	2112	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-4FTG256C	2112	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-5FTG256C	2112	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-6FTG256C	2112	1.2 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484C	2112	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-5FG484C	2112	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-6FG484C	2112	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4TG144C	4320	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-5TG144C	4320	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-6TG144C	4320	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-4MG132C	4320	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-5MG132C	4320	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-6MG132C	4320	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-4BG256C	4320	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4MG184C	4320	1.2 V	–4	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5MG184C	4320	1.2 V	–5	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-6MG184C	4320	1.2 V	–6	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5BG256C	4320	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-6BG256C	4320	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4FTG256C	4320	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-5FTG256C	4320	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-6FTG256C	4320	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-4BG332C	4320	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-5BG332C	4320	1.2 V	–5	Halogen-Free caBGA	332	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-6BG332C	4320	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-4FG484C	4320	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-5FG484C	4320	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-6FG484C	4320	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144C	6864	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-5TG144C	6864	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-6TG144C	6864	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-4BG256C	6864	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-5BG256C	6864	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-6BG256C	6864	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-4FTG256C	6864	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-5FTG256C	6864	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-6FTG256C	6864	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-4BG332C	6864	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-5BG332C	6864	1.2 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-6BG332C	6864	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-4FG484C	6864	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-5FG484C	6864	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-6FG484C	6864	1.2 V	–6	Halogen-Free fpBGA	484	COM

Date	Version	Section	Change Summary
December 2014	2.9	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Removed XO2-4000U data. — Removed 400-ball ftBGA. — Removed 25-ball WLCSP value for XO2-2000U.
		DC and Switching Characteristics	Updated the Recommended Operating Conditions section. Adjusted Max. values for V_{CC} and V_{CCIO}.
			Updated the sysIO Recommended Operating Conditions section. Adjusted Max. values for LVCMOS 3.3, LVTTL, PCI, LVDS33 and LVPECL.
		Pinout Information	Updated the Pinout Information Summary section. Removed MachXO2-4000U.
		Ordering Information	Updated the MachXO2 Part Number Description section. Removed BG400 package.
			Updated the High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
			Updated the High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
November 2014	2.8	Introduction	Updated the Features section. — Revised I/Os under Flexible Logic Architecture. — Revised standby power under Ultra Low Power Devices. — Revise input frequency range under Flexible On-Chip Clocking.
			Updated Table 1-1, MachXO2 Family Selection Guide. — Added XO2-4000U data. — Removed HE and ZE device options for XO2-4000. — Added 400-ball ftBGA.
		Pinout Information	Updated the Pinout Information Summary section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added BG400 package.
			Updated the Ordering Information section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400 part numbers.
October 2014	2.7	Ordering Information	Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Fixed typo in LCMXO2-2000ZE-1UWG49ITR part number package.
		Architecture	Updated the Supported Standards section. Added MIPI information to Table 2-12. Supported Input Standards and Table 2-13. Supported Output Standards.
		DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition.
			Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition.
			Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.
July 2014	2.6	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics[1, 2] section. Updated footnote 4.
			Updated Register-to-Register Performance section. Updated footnote.
		Ordering Information	Updated UW49 package to UWG49 in MachXO2 Part Number Description.
			Updated LCMXO2-2000ZE-1UWG49CTR package in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging.

Date	Version	Section	Change Summary
February 2012	01.7	All	Updated document with new corporate logo.
	01.6	—	Data sheet status changed from preliminary to final.
		Introduction	MachXO2 Family Selection Guide table – Removed references to 49-ball WLCSP.
		DC and Switching Characteristics	Updated Flash Download Time table.
			Modified Storage Temperature in the Absolute Maximum Ratings section.
			Updated I_{DK} max in Hot Socket Specifications table.
			Modified Static Supply Current tables for ZE and HC/HE devices.
			Updated Power Supply Ramp Rates table.
			Updated Programming and Erase Supply Current tables.
			Updated data in the External Switching Characteristics table.
			Corrected Absolute Maximum Ratings for Dedicated Input Voltage Applied for LCMXO2 HC.
			DC Electrical Characteristics table – Minor corrections to conditions for I_{IL}, I_{IH}.
		Pinout Information	Removed references to 49-ball WLCSP.
			Signal Descriptions table – Updated description for GND, VCC, and VCCIOx.
			Updated Pin Information Summary table – Number of VCCIOs, GNDs, VCCs, and Total Count of Bonded Pins for MachXO2-256, 640, and 640U and Dual Function I/O for MachXO2-4000 332caBGA.
		Ordering Information	Removed references to 49-ball WLCSP
August 2011	01.5	DC and Switching Characteristics	Updated ESD information.
		Ordering Information	Updated footnote for ordering WLCSP devices.
	01.4	Architecture	Updated information in Clock/Control Distribution Network and sysCLOCK Phase Locked Loops (PLLs).
		DC and Switching Characteristics	Updated I_{IL} and I_{IH} conditions in the DC Electrical Characteristics table.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Updated Pin Information Summary table: Dual Function I/O, DQS Groups Bank 1, Total General Purpose Single-Ended I/O, Differential I/O Per Bank, Total Count of Bonded Pins, Gearboxes. Added column of data for MachXO2-2000 49 WLCSP.
		Ordering Information	Updated R1 Device Specifications text section with information on migration from MachXO2-1200-R1 to Standard (non-R1) devices.
			Corrected Supply Voltage typo for part numbers: LCMX02-2000UHE-4FG484I, LCMX02-2000UHE-5FG484I, LCMX02-2000UHE-6FG484I.
			Added footnote for WLCSP package parts.
		Supplemental Information	Removed reference to Stand-alone Power Calculator for MachXO2 Devices. Added reference to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices.