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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Active
Number of LABs/CLBs	540
Number of Logic Elements/Cells	4320
Total RAM Bits	94208
Number of I/O	278
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-4000hc-5fg484c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-4000hc-5fg484c</a>

## Features

### ■ Flexible Logic Architecture

- Six devices with 256 to 6864 LUT4s and 18 to 334 I/Os

### ■ Ultra Low Power Devices

- Advanced 65 nm low power process
- As low as 22  $\mu$ W standby power
- Programmable low swing differential I/Os
- Stand-by mode and other power saving options

### ■ Embedded and Distributed Memory

- Up to 240 kbits sysMEM™ Embedded Block RAM
- Up to 54 kbits Distributed RAM
- Dedicated FIFO control logic

### ■ On-Chip User Flash Memory

- Up to 256 kbits of User Flash Memory
- 100,000 write cycles
- Accessible through WISHBONE, SPI, I<sup>2</sup>C and JTAG interfaces
- Can be used as soft processor PROM or as Flash memory

### ■ Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/Os
- Generic DDR, DDRX2, DDRX4
- Dedicated DDR/DDR2/LPDDR memory with QDS support

### ■ High Performance, Flexible I/O Buffer

- Programmable sysIO™ buffer supports wide range of interfaces:
  - LVCMOS 3.3/2.5/1.8/1.5/1.2
  - LVTTTL
  - PCI
  - LVDS, Bus-LVDS, MLVDS, RSDS, LVPECL
  - SSTL 25/18
  - HSTL 18
  - Schmitt trigger inputs, up to 0.5 V hysteresis
- I/Os support hot socketing
- On-chip differential termination
- Programmable pull-up or pull-down mode

### ■ Flexible On-Chip Clocking

- Eight primary clocks
- Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
- Up to two analog PLLs per device with fractional-n frequency synthesis
  - Wide input frequency range (7 MHz to 400 MHz)

### ■ Non-volatile, Infinitely Reconfigurable

- Instant-on – powers up in microseconds
- Single-chip, secure solution
- Programmable through JTAG, SPI or I<sup>2</sup>C
- Supports background programming of non-volatile memory
- Optional dual boot with external SPI memory

### ■ TransFR™ Reconfiguration

- In-field logic update while system operates

### ■ Enhanced System Level Support

- On-chip hardened functions: SPI, I<sup>2</sup>C, timer/counter
- On-chip oscillator with 5.5% accuracy
- Unique TraceID for system tracking
- One Time Programmable (OTP) mode
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming

### ■ Broad Range of Package Options

- TQFP, WLCSP, ucBGA, csBGA, caBGA, ftBGA, fpBGA, QFN package options
- Small footprint package options
  - As small as 2.5 mm x 2.5 mm
- Density migration supported
- Advanced halogen-free packaging

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2-640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO2 devices provide commonly used hardened functions such as SPI controller, I<sup>2</sup>C controller and timer/counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I<sup>2</sup>C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

## **PFU Blocks**

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.
3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

### FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

**Table 2-7. Programmable FIFO Flag Ranges**

Flag Name	Programming Range
Full (FF)	1 to max (up to $2^N-1$ )
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

### Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

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## DDR Memory Support

Certain PICs on the right edge of MachXO2-640U, MachXO2-1200/U and larger devices, have additional circuitry to allow the implementation of DDR memory interfaces. There are two groups of 14 or 12 PIOs each on the right edge with additional circuitry to implement DDR memory interfaces. This capability allows the implementation of up to 16-bit wide memory interfaces. One PIO from each group contains a control element, the DQS Read/Write Block, to facilitate the generation of clock and control signals (DQSR90, DQSW90, DDRCLKPOL and DATAVALID). These clock and control signals are distributed to the other PIO in the group through dedicated low skew routing.

### DQS Read Write Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Read Write block provides the required clock alignment for DDR memory interfaces. DQSR90 and DQSW90 signals are generated by the DQS Read Write block from the DQS input.

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the read cycle) is unknown. The MachXO2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This circuit changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each read cycle for the correct clock polarity. Prior to the read operation in DDR memories, DQS is in tri-state (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit in the DQS Read Write block detects the first DQS rising edge after the preamble state and generates the DDRCLKPOL signal. This signal is used to control the polarity of the clock to the synchronizing registers.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration signals (6-bit bus) from a DLL on the right edge of the device. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

### sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, PCI, SSTL, HSTL, LVDS, BLVDS, MLVDS and LVPECL.

Each bank is capable of supporting multiple I/O standards. In the MachXO2 devices, single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS and PCI), differential (LVDS) and referenced input buffers (SSTL and HSTL) are powered using I/O supply voltage ( $V_{CCIO}$ ). Each sysIO bank has its own  $V_{CCIO}$ . In addition, each bank has a voltage reference,  $V_{REF}$  which allows the use of referenced input buffers independent of the bank  $V_{CCIO}$ .

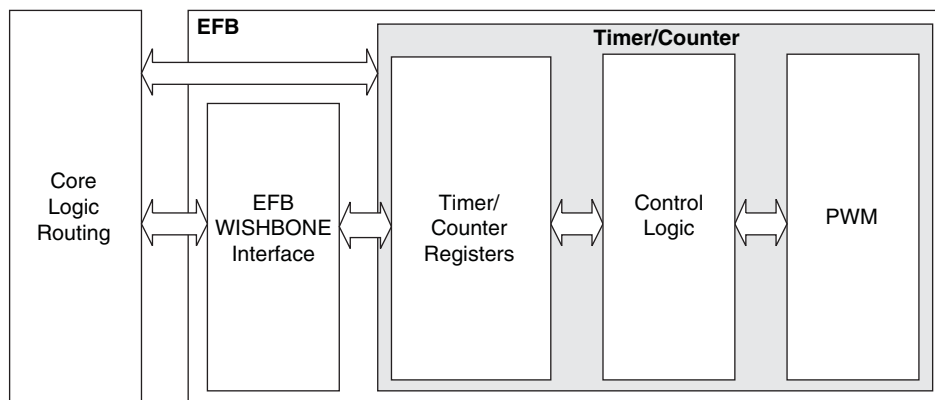
MachXO2-256 and MachXO2-640 devices contain single-ended ratioed input buffers and single-ended output buffers with complementary outputs on all the I/O banks. Note that the single-ended input buffers on these devices do not contain PCI clamps. In addition to the single-ended I/O buffers these two devices also have differential and referenced input buffers on all I/Os. The I/Os are arranged in pairs, the two pads in the pair are described as "T" and "C", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

## Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  - Watchdog timer
  - Clear timer on compare match
  - Fast PWM
  - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

**Figure 2-23. Timer/Counter Block Diagram**



**Table 2-17. Timer/Counter Signal Description**

Port	I/O	Description
tc_clk	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	O	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	O	Timer counter output signal

Input/Output Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$ Max. (V)	$V_{OH}$ Min. (V)	$I_{OL}$ Max. <sup>4</sup> (mA)	$I_{OH}$ Max. <sup>4</sup> (mA)
	Min. (V) <sup>3</sup>	Max. (V)	Min. (V)	Max. (V)				
LVC MOS10R25	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain

1. MachXO2 devices allow LVC MOS inputs to be placed in I/O banks where  $V_{CCIO}$  is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO2 devices do not meet the relevant JEDEC specification are documented in the table below.
2. MachXO2 devices allow for LVC MOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1202, [MachXO2 sysIO Usage Guide](#).
3. The dual function I<sup>2</sup>C pins SCL and SDA are limited to a  $V_{IL}$  min of -0.25 V or to -0.3 V with a duration of <10 ns.
4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive  $V_{CCIO}$  or GND pad connections, or between the last  $V_{CCIO}$  or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of  $n * 8$  mA. "n" is the number of I/O pads between the two consecutive bank  $V_{CCIO}$  or GND connections or between the last  $V_{CCIO}$  and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

Input Standard	$V_{CCIO}$ (V)	$V_{IL}$ Max. (V)
LVC MOS 33	1.5	0.685
LVC MOS 25	1.5	0.687
LVC MOS 18	1.5	0.655

## sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of MachXO2-640U, MachXO2-1200/U and higher density devices in the MachXO2 PLD family.

### LVDS

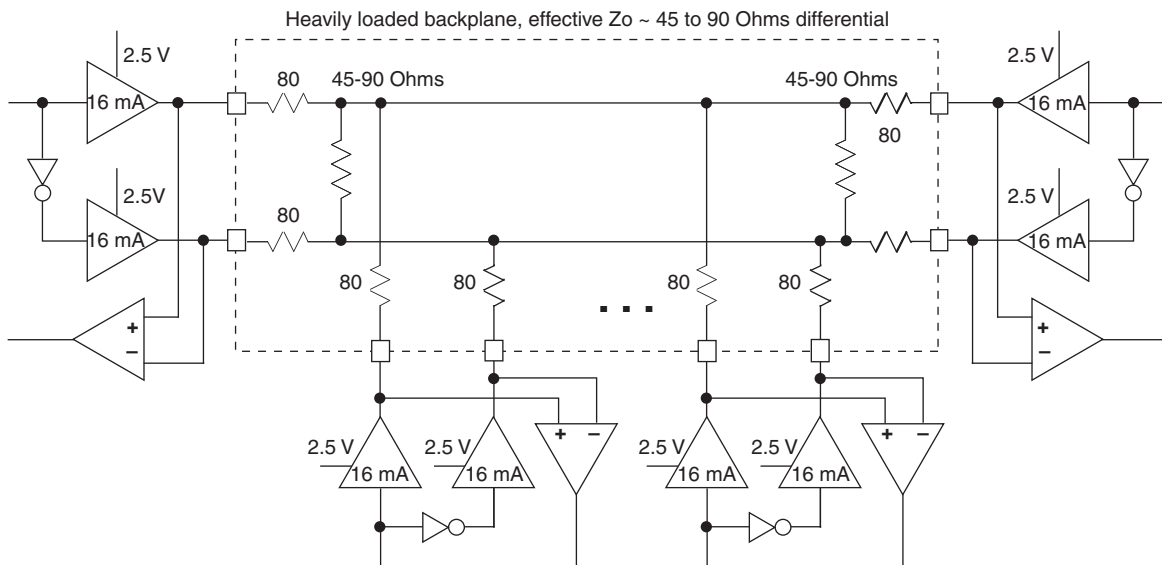
#### Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{INP}$ $V_{INM}$	Input Voltage	$V_{CCIO} = 3.3$ V	0	—	2.605	V
		$V_{CCIO} = 2.5$ V	0	—	2.05	V
$V_{THD}$	Differential Input Threshold		±100	—		mV
$V_{CM}$	Input Common Mode Voltage	$V_{CCIO} = 3.3$ V	0.05	—	2.6	V
		$V_{CCIO} = 2.5$ V	0.05	—	2.0	V
$I_{IN}$	Input current	Power on	—	—	±10	μA
$V_{OH}$	Output high voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100$ Ohm	—	1.375	—	V
$V_{OL}$	Output low voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100$ Ohm	0.90	1.025	—	V
$V_{OD}$	Output voltage differential	$(V_{OP} - V_{OM})$ , $R_T = 100$ Ohm	250	350	450	mV
$\Delta V_{OD}$	Change in $V_{OD}$ between high and low		—	—	50	mV
$V_{OS}$	Output voltage offset	$(V_{OP} + V_{OM})/2$ , $R_T = 100$ Ohm	1.125	1.20	1.395	V
$\Delta V_{OS}$	Change in $V_{OS}$ between H and L		—	—	50	mV
$I_{OSD}$	Output short circuit current	$V_{OD} = 0$ V driver outputs shorted	—	—	24	mA

### BLVDS

The MachXO2 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

**Figure 3-2. BLVDS Multi-point Output Example**



**Table 3-2. BLVDS DC Conditions<sup>1</sup>**

#### Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z <sub>OUT</sub>	Output impedance	20	20	Ohms
R <sub>S</sub>	Driver series resistance	80	80	Ohms
R <sub>TLEFT</sub>	Left end termination	45	90	Ohms
R <sub>TRIGHT</sub>	Right end termination	45	90	Ohms
V <sub>OH</sub>	Output high voltage	1.376	1.480	V
V <sub>OL</sub>	Output low voltage	1.124	1.020	V
V <sub>OD</sub>	Output differential voltage	0.253	0.459	V
V <sub>CM</sub>	Output common mode voltage	1.250	1.250	V
I <sub>DC</sub>	DC output current	11.236	10.204	mA

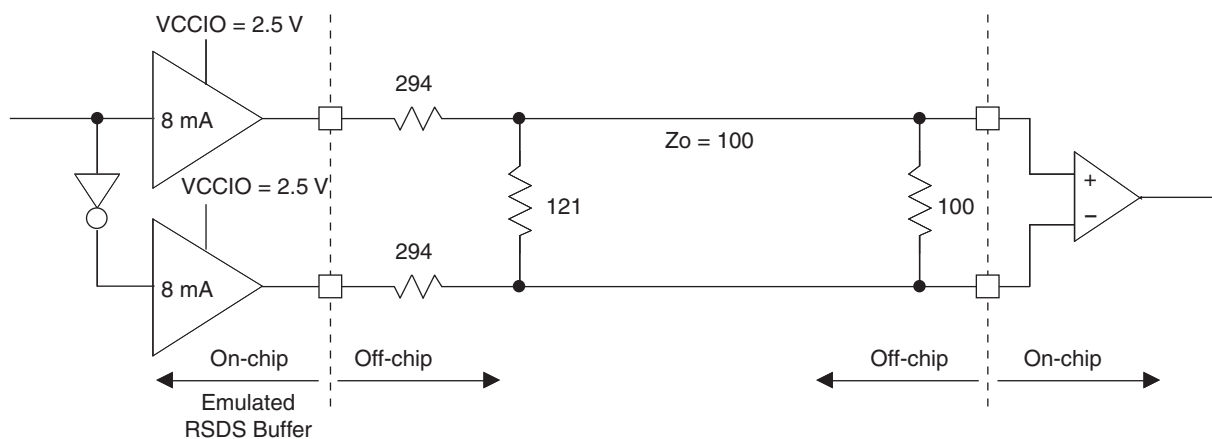
1. For input buffer, see LVDS table.



### RSDS

The MachXO2 family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

**Figure 3-4. RSDS (Reduced Swing Differential Standard)**



**Table 3-4. RSDS DC Conditions**

Parameter	Description	Typical	Units
$Z_{OUT}$	Output impedance	20	Ohms
$R_S$	Driver series resistor	294	Ohms
$R_P$	Driver parallel resistor	121	Ohms
$R_T$	Receiver termination	100	Ohms
$V_{OH}$	Output high voltage	1.35	V
$V_{OL}$	Output low voltage	1.15	V
$V_{OD}$	Output differential voltage	0.20	V
$V_{CM}$	Output common mode voltage	1.25	V
$Z_{BACK}$	Back impedance	101.5	Ohms
$I_{DC}$	DC output current	3.66	mA

### MachXO2 External Switching Characteristics – HC/HE Devices<sup>1, 2, 3, 4, 5, 6, 7</sup>

Over Recommended Operating Conditions

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f <sub>MAX_PRI</sub> <sup>8</sup>	Frequency for Primary Clock Tree	All MachXO2 devices	—	388	—	323	—	269	MHz
t <sub>W_PRI</sub>	Clock Pulse Width for Primary Clock	All MachXO2 devices	0.5	—	0.6	—	0.7	—	ns
t <sub>SKEW_PRI</sub>	Primary Clock Skew Within a Device	MachXO2-256HC-HE	—	912	—	939	—	975	ps
		MachXO2-640HC-HE	—	844	—	871	—	908	ps
		MachXO2-1200HC-HE	—	868	—	902	—	951	ps
		MachXO2-2000HC-HE	—	867	—	897	—	941	ps
		MachXO2-4000HC-HE	—	865	—	892	—	931	ps
		MachXO2-7000HC-HE	—	902	—	942	—	989	ps
Edge Clock									
f <sub>MAX_EDGE</sub> <sup>8</sup>	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	400	—	333	—	278	MHz
Pin-LUT-Pin Propagation Delay									
t <sub>PD</sub>	Best case propagation delay through one LUT-4	All MachXO2 devices	—	6.72	—	6.96	—	7.24	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t <sub>CO</sub>	Clock to Output – PIO Output Register	MachXO2-256HC-HE	—	7.13	—	7.30	—	7.57	ns
		MachXO2-640HC-HE	—	7.15	—	7.30	—	7.57	ns
		MachXO2-1200HC-HE	—	7.44	—	7.64	—	7.94	ns
		MachXO2-2000HC-HE	—	7.46	—	7.66	—	7.96	ns
		MachXO2-4000HC-HE	—	7.51	—	7.71	—	8.01	ns
		MachXO2-7000HC-HE	—	7.54	—	7.75	—	8.06	ns
t <sub>SU</sub>	Clock to Data Setup – PIO Input Register	MachXO2-256HC-HE	–0.06	—	–0.06	—	–0.06	—	ns
		MachXO2-640HC-HE	–0.06	—	–0.06	—	–0.06	—	ns
		MachXO2-1200HC-HE	–0.17	—	–0.17	—	–0.17	—	ns
		MachXO2-2000HC-HE	–0.20	—	–0.20	—	–0.20	—	ns
		MachXO2-4000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-7000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
t <sub>H</sub>	Clock to Data Hold – PIO Input Register	MachXO2-256HC-HE	1.75	—	1.95	—	2.16	—	ns
		MachXO2-640HC-HE	1.75	—	1.95	—	2.16	—	ns
		MachXO2-1200HC-HE	1.88	—	2.12	—	2.36	—	ns
		MachXO2-2000HC-HE	1.89	—	2.13	—	2.37	—	ns
		MachXO2-4000HC-HE	1.94	—	2.18	—	2.43	—	ns
		MachXO2-7000HC-HE	1.98	—	2.23	—	2.49	—	ns

Parameter	Description	Device	-6		-5		-4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR <sup>9, 12</sup>									
t <sub>DVADQ</sub>	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. <sup>13</sup>	—	0.369	—	0.395	—	0.421	UI
t <sub>DVEDQ</sub>	Input Data Hold After DQS Input		0.529	—	0.530	—	0.527	—	UI
t <sub>DQVBS</sub>	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t <sub>DQVAS</sub>	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f <sub>DATA</sub>	MEM LPDDR Serial Data Speed		—	280	—	250	—	208	Mbps
f <sub>SCLK</sub>	SCLK Frequency		—	140	—	125	—	104	MHz
f <sub>LPDDR</sub>	LPDDR Data Transfer Rate		0	280	0	250	0	208	Mbps
DDR <sup>9, 12</sup>									
t <sub>DVADQ</sub>	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. <sup>13</sup>	—	0.350	—	0.387	—	0.414	UI
t <sub>DVEDQ</sub>	Input Data Hold After DQS Input		0.545	—	0.538	—	0.532	—	UI
t <sub>DQVBS</sub>	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t <sub>DQVAS</sub>	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f <sub>DATA</sub>	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f <sub>SCLK</sub>	SCLK Frequency		—	150	—	125	—	104	MHz
f <sub>MEM_DDR</sub>	MEM DDR Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps
DDR2 <sup>9, 12</sup>									
t <sub>DVADQ</sub>	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. <sup>13</sup>	—	0.360	—	0.378	—	0.406	UI
t <sub>DVEDQ</sub>	Input Data Hold After DQS Input		0.555	—	0.549	—	0.542	—	UI
t <sub>DQVBS</sub>	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t <sub>DQVAS</sub>	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f <sub>DATA</sub>	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f <sub>SCLK</sub>	SCLK Frequency		—	150	—	125	—	104	MHz
f <sub>MEM_DDR2</sub>	MEM DDR2 Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps

- Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
- General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
- Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
- DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
- 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
- For Generic DDRX1 mode  $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$ .
- The  $t_{SU\_DEL}$  and  $t_{H\_DEL}$  values use the SCLK\_ZERHOLD default step size. Each step is 105 ps (-6), 113 ps (-5), 120 ps (-4).
- This number for general purpose usage. Duty cycle tolerance is +/- 10%.
- Duty cycle is +/-5% for system usage.
- The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
- High-speed DDR and LVDS not supported in SG32 (32 QFN) packages.
- Advance information for MachXO2 devices in 48 QFN packages.
- DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

### MachXO2 External Switching Characteristics – ZE Devices<sup>1, 2, 3, 4, 5, 6, 7</sup>

Over Recommended Operating Conditions

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f <sub>MAX_PRI</sub> <sup>8</sup>	Frequency for Primary Clock Tree	All MachXO2 devices	—	150	—	125	—	104	MHz
t <sub>W_PRI</sub>	Clock Pulse Width for Primary Clock	All MachXO2 devices	1.00	—	1.20	—	1.40	—	ns
t <sub>SKEW_PRI</sub>	Primary Clock Skew Within a Device	MachXO2-256ZE	—	1250	—	1272	—	1296	ps
		MachXO2-640ZE	—	1161	—	1183	—	1206	ps
		MachXO2-1200ZE	—	1213	—	1267	—	1322	ps
		MachXO2-2000ZE	—	1204	—	1250	—	1296	ps
		MachXO2-4000ZE	—	1195	—	1233	—	1269	ps
		MachXO2-7000ZE	—	1243	—	1268	—	1296	ps
Edge Clock									
f <sub>MAX_EDGE</sub> <sup>8</sup>	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	210	—	175	—	146	MHz
Pin-LUT-Pin Propagation Delay									
t <sub>PD</sub>	Best case propagation delay through one LUT-4	All MachXO2 devices	—	9.35	—	9.78	—	10.21	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t <sub>CO</sub>	Clock to Output – PIO Output Register	MachXO2-256ZE	—	10.46	—	10.86	—	11.25	ns
		MachXO2-640ZE	—	10.52	—	10.92	—	11.32	ns
		MachXO2-1200ZE	—	11.24	—	11.68	—	12.12	ns
		MachXO2-2000ZE	—	11.27	—	11.71	—	12.16	ns
		MachXO2-4000ZE	—	11.28	—	11.78	—	12.28	ns
		MachXO2-7000ZE	—	11.22	—	11.76	—	12.30	ns
t <sub>SU</sub>	Clock to Data Setup – PIO Input Register	MachXO2-256ZE	–0.21	—	–0.21	—	–0.21	—	ns
		MachXO2-640ZE	–0.22	—	–0.22	—	–0.22	—	ns
		MachXO2-1200ZE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-2000ZE	–0.27	—	–0.27	—	–0.27	—	ns
		MachXO2-4000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-7000ZE	–0.33	—	–0.33	—	–0.33	—	ns
t <sub>H</sub>	Clock to Data Hold – PIO Input Register	MachXO2-256ZE	3.96	—	4.25	—	4.65	—	ns
		MachXO2-640ZE	4.01	—	4.31	—	4.71	—	ns
		MachXO2-1200ZE	3.95	—	4.29	—	4.73	—	ns
		MachXO2-2000ZE	3.94	—	4.29	—	4.74	—	ns
		MachXO2-4000ZE	3.96	—	4.36	—	4.87	—	ns
		MachXO2-7000ZE	3.93	—	4.37	—	4.91	—	ns

Parameter	Description	Device	-3		-2		-1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR <sup>9, 12</sup>									
t <sub>DVADQ</sub>	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. <sup>13</sup>	—	0.349	—	0.381	—	0.396	UI
t <sub>DVEDQ</sub>	Input Data Hold After DQS Input		0.665	—	0.630	—	0.613	—	UI
t <sub>DQVBS</sub>	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t <sub>DQVAS</sub>	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f <sub>DATA</sub>	MEM LPDDR Serial Data Speed		—	120	—	110	—	96	Mbps
f <sub>SCLK</sub>	SCLK Frequency		—	60	—	55	—	48	MHz
f <sub>LPDDR</sub>	LPDDR Data Transfer Rate		0	120	0	110	0	96	Mbps
DDR <sup>9, 12</sup>									
t <sub>DVADQ</sub>	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. <sup>13</sup>	—	0.347	—	0.374	—	0.393	UI
t <sub>DVEDQ</sub>	Input Data Hold After DQS Input		0.665	—	0.637	—	0.616	—	UI
t <sub>DQVBS</sub>	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t <sub>DQVAS</sub>	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f <sub>DATA</sub>	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f <sub>SCLK</sub>	SCLK Frequency		—	70	—	58	—	49	MHz
f <sub>MEM_DDR</sub>	MEM DDR Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps
DDR2 <sup>9, 12</sup>									
t <sub>DVADQ</sub>	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. <sup>13</sup>	—	0.372	—	0.394	—	0.410	UI
t <sub>DVEDQ</sub>	Input Data Hold After DQS Input		0.690	—	0.658	—	0.618	—	UI
t <sub>DQVBS</sub>	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t <sub>DQVAS</sub>	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f <sub>DATA</sub>	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f <sub>SCLK</sub>	SCLK Frequency		—	70	—	58	—	49	MHz
f <sub>MEM_DDR2</sub>	MEM DDR2 Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps

- Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
- General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pF load, fast slew rate.
- Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
- DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
- 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
- For Generic DDRX1 mode  $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$ .
- The  $t_{SU\_DEL}$  and  $t_{H\_DEL}$  values use the SCLK\_ZERHOLD default step size. Each step is 167 ps (–3), 182 ps (–2), 195 ps (–1).
- This number for general purpose usage. Duty cycle tolerance is +/-10%.
- Duty cycle is +/- 5% for system usage.
- The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
- High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.
- Advance information for MachXO2 devices in 48 QFN packages.
- DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

## Flash Download Time<sup>1, 2</sup>

Symbol	Parameter	Device	Typ.	Units
$t_{\text{REFRESH}}$	POR to Device I/O Active	LCMXO2-256	0.6	ms
		LCMXO2-640	1.0	ms
		LCMXO2-640U	1.9	ms
		LCMXO2-1200	1.9	ms
		LCMXO2-1200U	1.4	ms
		LCMXO2-2000	1.4	ms
		LCMXO2-2000U	2.4	ms
		LCMXO2-4000	2.4	ms
		LCMXO2-7000	3.8	ms

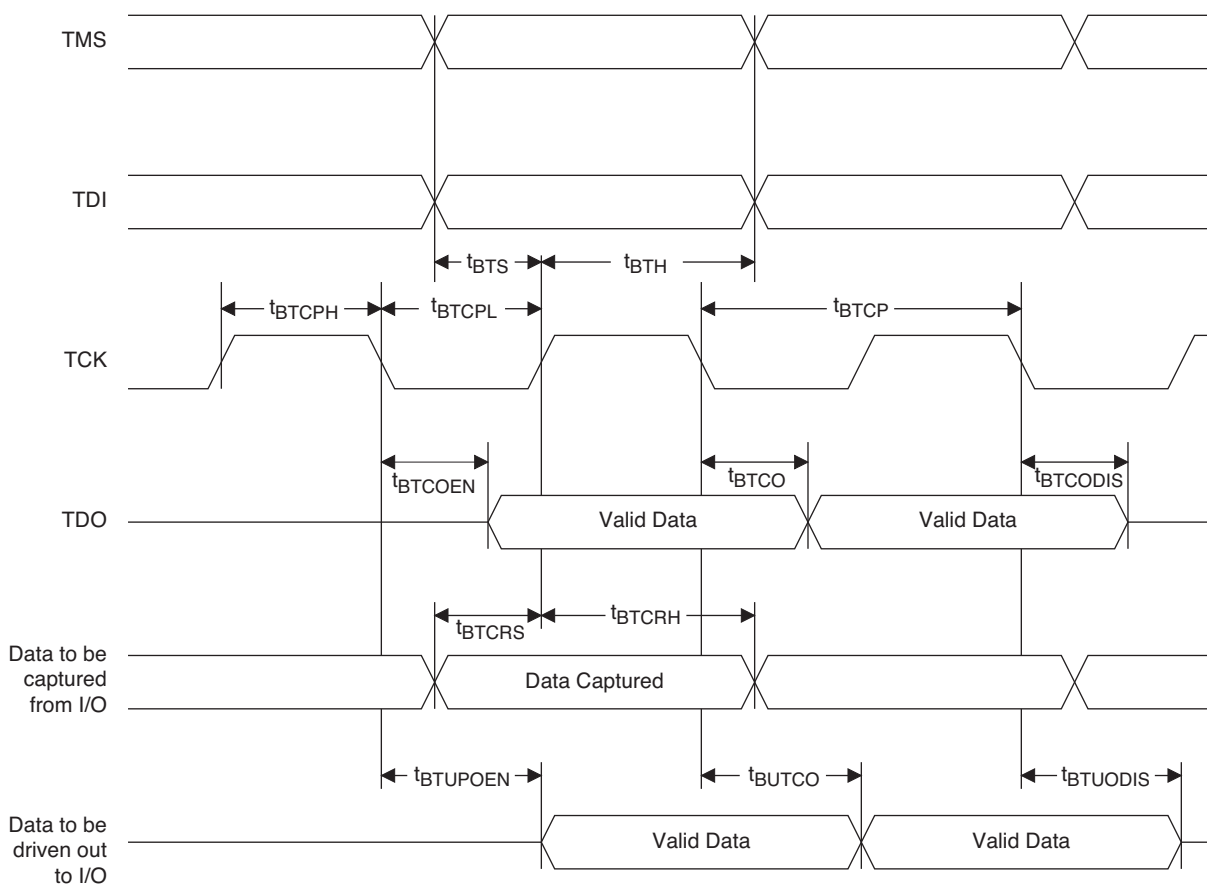
1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.

2. The Flash download time is measured starting from the maximum voltage of POR trip point.

## JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
$f_{\text{MAX}}$	TCK clock frequency	—	25	MHz
$t_{\text{BTCPH}}$	TCK [BSCAN] clock pulse width high	20	—	ns
$t_{\text{BTCPL}}$	TCK [BSCAN] clock pulse width low	20	—	ns
$t_{\text{BTS}}$	TCK [BSCAN] setup time	10	—	ns
$t_{\text{BTH}}$	TCK [BSCAN] hold time	8	—	ns
$t_{\text{BTCO}}$	TAP controller falling edge of clock to valid output	—	10	ns
$t_{\text{BTCODIS}}$	TAP controller falling edge of clock to valid disable	—	10	ns
$t_{\text{BTCOEN}}$	TAP controller falling edge of clock to valid enable	—	10	ns
$t_{\text{BTCRS}}$	BSCAN test capture register setup time	8	—	ns
$t_{\text{BTCRH}}$	BSCAN test capture register hold time	20	—	ns
$t_{\text{BUTCO}}$	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{\text{BTUODIS}}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{\text{BTUPOEN}}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

**Figure 3-12. JTAG Port Timing Waveforms**



### Signal Descriptions

Signal Name	I/O	Descriptions
<b>General Purpose</b>		
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	<p>[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).</p> <p>[Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.</p> <p>[A/B/C/D] indicates the PIO within the group to which the pad is connected.</p> <p>Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic.</p> <p>During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.</p>
NC	—	No connect.
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together. For QFN 48 package, the exposed die pad is the device ground.
VCC	—	VCC – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIOx	—	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.
<b>PLL and Clock Functions</b> (Used as user-programmable I/O pins when not used for PLL or clock pins)		
[LOC]_GPLL[T, C]_IN	—	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.
<b>Test and Programming</b> (Dual function pins used for test access port and during sysCONFIG™)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
JTAGENB	I	<p>Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then:</p> <p>If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O.</p> <p>If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.</p> <p>For more details, refer to TN1204, <a href="#">MachXO2 Programming and Configuration Usage Guide</a>.</p>
<b>Configuration</b> (Dual function pins used during sysCONFIG)		
PROGRAMN	I	Initiates configuration sequence when asserted low. During configuration, or when reserved as PROGRAMN in user mode, this pin always has an active pull-up.



### Pinout Information Summary

	MachXO2-256					MachXO2-640			MachXO2-640U
	32 QFN <sup>1</sup>	48 QFN <sup>3</sup>	64 ucBGA	100 TQFP	132 csBGA	48 QFN <sup>3</sup>	100 TQFP	132 csBGA	144 TQFP
<b>General Purpose I/O per Bank</b>									
Bank 0	8	10	9	13	13	10	18	19	27
Bank 1	2	10	12	14	14	10	20	20	26
Bank 2	9	10	11	14	14	10	20	20	28
Bank 3	2	10	12	14	14	10	20	20	26
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Single Ended I/O	21	40	44	55	55	40	78	79	107
<b>Differential I/O per Bank</b>									
Bank 0	4	5	5	7	7	5	9	10	14
Bank 1	1	5	6	7	7	5	10	10	13
Bank 2	4	5	5	7	7	5	10	10	14
Bank 3	1	5	6	7	7	5	10	10	13
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Differential I/O	10	20	22	28	28	20	39	40	54
<b>Dual Function I/O</b>									
	22	25	27	29	29	25	29	29	33
<b>High-speed Differential I/O</b>									
Bank 0	0	0	0	0	0	0	0	0	7
<b>Gearboxes</b>									
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	0	0	0	0	0	0	0	0	7
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	0	0	0	0	0	0	0	0	7
<b>DQS Groups</b>									
Bank 1	0	0	0	0	0	0	0	0	2
<b>VCCIO Pins</b>									
Bank 0	2	2	2	2	2	2	2	2	3
Bank 1	1	1	2	2	2	1	2	2	3
Bank 2	2	2	2	2	2	2	2	2	3
Bank 3	1	1	2	2	2	1	2	2	3
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
VCC	2	2	2	2	2	2	2	2	4
GND <sup>2</sup>	2	1	8	8	8	1	8	10	12
NC	0	0	1	26	58	0	3	32	8
Reserved for Configuration	1	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	32	49	64	100	132	49	100	132	144

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.
2. For 48 QFN package, exposed die pad is the device ground.
3. 48-pin QFN information is 'Advanced'.

	MachXO2-1200					MachXO2-1200U
	100 TQFP	132 csBGA	144 TQFP	25 WLCSP	32 QFN <sup>1</sup>	256 ftBGA
<b>General Purpose I/O per Bank</b>						
Bank 0	18	25	27	11	9	50
Bank 1	21	26	26	0	2	52
Bank 2	20	28	28	7	9	52
Bank 3	20	25	26	0	2	16
Bank 4	0	0	0	0	0	16
Bank 5	0	0	0	0	0	20
Total General Purpose Single Ended I/O	79	104	107	18	22	206
<b>Differential I/O per Bank</b>						
Bank 0	9	13	14	5	4	25
Bank 1	10	13	13	0	1	26
Bank 2	10	14	14	2	4	26
Bank 3	10	12	13	0	1	8
Bank 4	0	0	0	0	0	8
Bank 5	0	0	0	0	0	10
Total General Purpose Differential I/O	39	52	54	7	10	103
<b>Dual Function I/O</b>						
	31	33	33	18	22	33
<b>High-speed Differential I/O</b>						
Bank 0	4	7	7	0	0	14
<b>Gearboxes</b>						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	4	7	7	0	0	14
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	5	7	7	0	2	14
<b>DQS Groups</b>						
Bank 1	1	2	2	0	0	2
<b>VCCIO Pins</b>						
Bank 0	2	3	3	1	2	4
Bank 1	2	3	3	0	1	4
Bank 2	2	3	3	1	2	4
Bank 3	3	3	3	0	1	1
Bank 4	0	0	0	0	0	2
Bank 5	0	0	0	0	0	1
VCC	2	4	4	2	2	8
GND	8	10	12	2	2	24
NC	1	1	8	0	0	1
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	100	132	144	25	32	256

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.

### Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32C	256	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-256ZE-2SG32C	256	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-256ZE-3SG32C	256	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-256ZE-1UMG64C	256	1.2 V	–1	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-2UMG64C	256	1.2 V	–2	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-3UMG64C	256	1.2 V	–3	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-1TG100C	256	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-2TG100C	256	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-3TG100C	256	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-1MG132C	256	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-2MG132C	256	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-3MG132C	256	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100C	640	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-2TG100C	640	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-3TG100C	640	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-1MG132C	640	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-2MG132C	640	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-3MG132C	640	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1SG32C	1280	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-2SG32C	1280	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-3SG32C	1280	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-1TG100C	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100C	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100C	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132C	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132C	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132C	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144C	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144C	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144C	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

# MachXO2 Family Data Sheet

## Revision History

March 2017

Data Sheet DS1035

Date	Version	Section	Change Summary
March 2017	3.3	DC and Switching Characteristics	Updated the <a href="#">Absolute Maximum Ratings</a> section. Added standards.
			Updated the <a href="#">sysIO Recommended Operating Conditions</a> section. Added standards.
			Updated the <a href="#">sysIO Single-Ended DC Electrical Characteristics</a> section. Added standards.
			Updated the <a href="#">MachXO2 External Switching Characteristics – HC/HE Devices</a> section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the $D_{VB}$ and the $D_{VA}$ parameters were changed to $D_{IB}$ and $D_{IA}$ . The parameter descriptions were also modified.
			Updated the <a href="#">MachXO2 External Switching Characteristics – ZE Devices</a> section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the $D_{VB}$ and the $D_{VA}$ parameters were changed to $D_{IB}$ and $D_{IA}$ . The parameter descriptions were also modified.
			Updated the <a href="#">sysCONFIG Port Timing Specifications</a> section. Corrected the $t_{INITL}$ units from ns to $\mu$ s.
		Pinout Information	Updated the <a href="#">Signal Descriptions</a> section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals.
			Updated the <a href="#">Pinout Information Summary</a> section. Added footnote to MachXO2-1200 32 QFN.
		Ordering Information	Updated the <a href="#">MachXO2 Part Number Description</a> section. Corrected the MG184, BG256, FTG256 package information. Added “(0.8 mm Pitch)” to BG332.
			Updated the <a href="#">Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging</a> section. — Updated LCMXO2-1200ZE-1UWG25ITR50 footnote. — Corrected footnote numbering typo. — Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2-2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s.

Date	Version	Section	Change Summary
January 2013	02.0	Introduction	Updated the total number IOs to include JTAGENB.
		Architecture	Supported Output Standards table – Added 3.3 V <sub>CCIO</sub> (Typ.) to LVDS row.
			Changed SRAM CRC Error Detection to Soft Error Detection.
		DC and Switching Characteristics	Power Supply Ramp Rates table – Updated Units column for t <sub>RAMP</sub> symbol.
			Added new Maximum sysIO Buffer Performance table.
			sysCLOCK PLL Timing table – Updated Min. column values for f <sub>IN</sub> , f <sub>OUT</sub> , f <sub>OUT2</sub> and f <sub>PFD</sub> parameters. Added t <sub>SPO</sub> parameter. Updated footnote 6.
			MachXO2 Oscillator Output Frequency table – Updated symbol name for t <sub>STABLEOSC</sub> .
			DC Electrical Characteristics table – Updated conditions for I <sub>IL</sub> , I <sub>IH</sub> symbols.
			Corrected parameters tDQVBS and tDQVAS
			Corrected MachXO2 ZE parameters tDVADQ and tDVEDQ
		Pinout Information	Included the MachXO2-4000HE 184 csBGA package.
		Ordering Information	Updated part number.
April 2012	01.9	Architecture	Removed references to TN1200.
		Ordering Information	Updated the Device Status portion of the MachXO2 Part Number Description to include the 50 parts per reel for the WLCSP package.
			Added new part number and footnote 2 for LCMXO2-1200ZE-1UWG25ITR50.
			Updated footnote 1 for LCMXO2-1200ZE-1UWG25ITR.
		Supplemental Information	Removed references to TN1200.
March 2012	01.8	Introduction	Added 32 QFN packaging information to Features bullets and MachXO2 Family Selection Guide table.
		DC and Switching Characteristics	Changed 'STANDBY' to 'USERSTDBY' in Standby Mode timing diagram.
		Pinout Information	Removed footnote from Pin Information Summary tables.
			Added 32 QFN package to Pin Information Summary table.
		Ordering Information	Updated Part Number Description and Ordering Information tables for 32 QFN package.
			Updated topside mark diagram in the Ordering Information section.