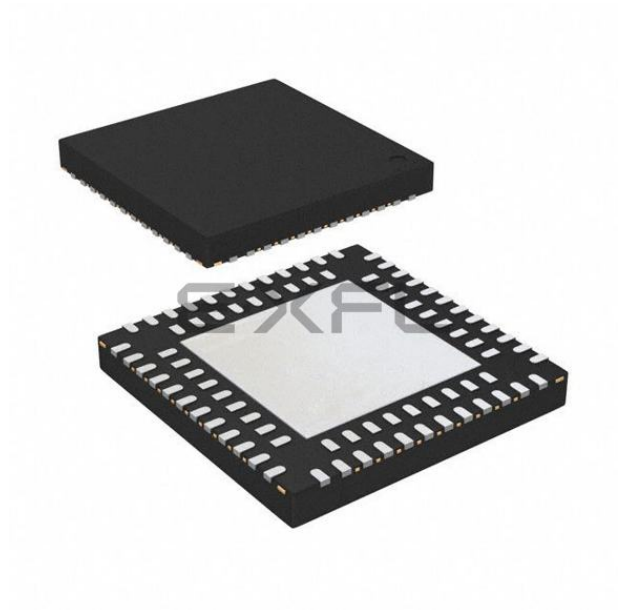
Lattice Semiconductor Corporation - LCMXO2-4000HC-5QN84C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

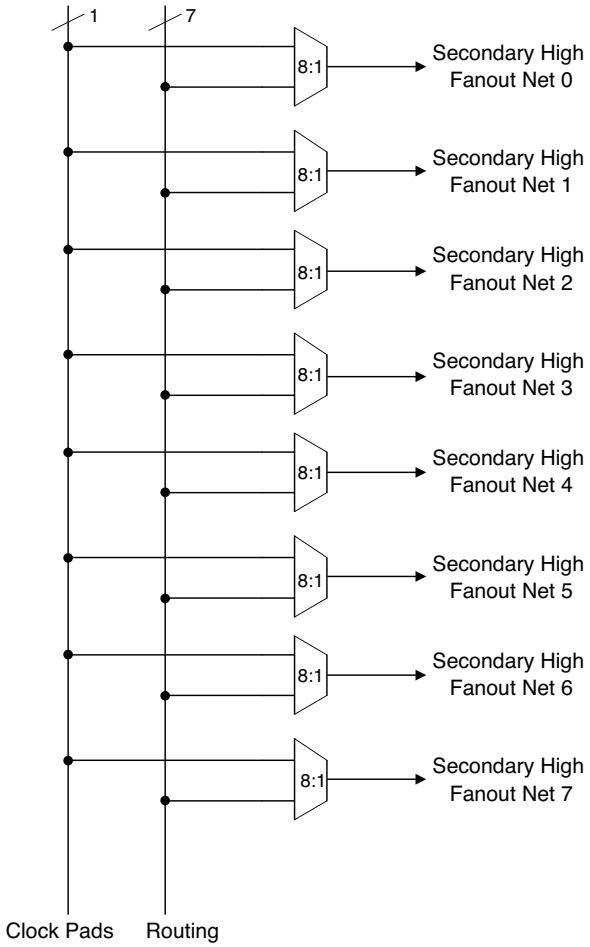
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	540
Number of Logic Elements/Cells	4320
Total RAM Bits	94208
Number of I/O	68
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	84-VFQFN Dual Rows, Exposed Pad
Supplier Device Package	84-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-4000hc-5qn84c

Figure 2-6. Secondary High Fanout Nets for MachXO2 Devices



sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The MachXO2-640U, MachXO2-1200/U and larger devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO2 sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO2 clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.

3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

Table 2-7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

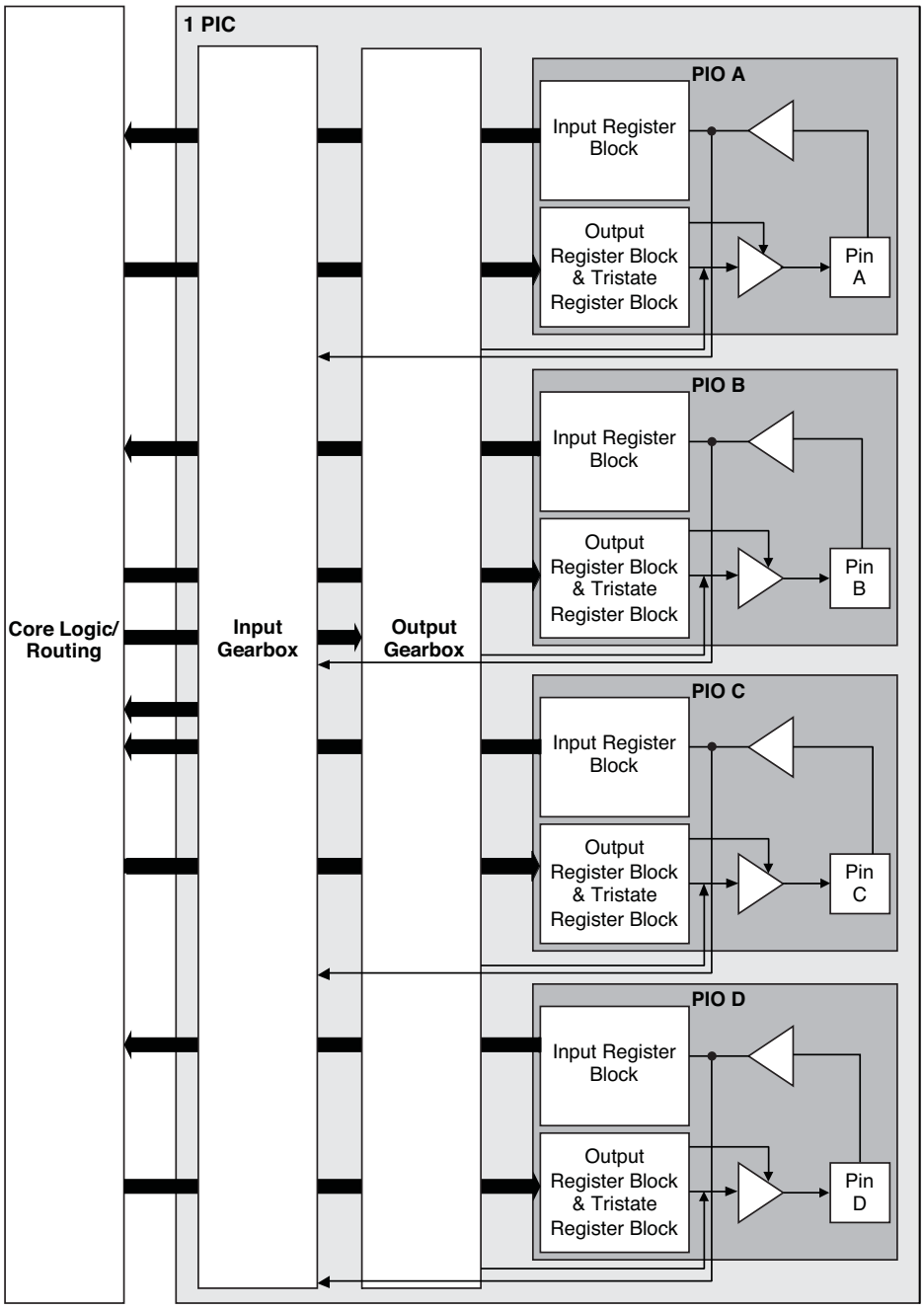
N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

Memory Core Reset

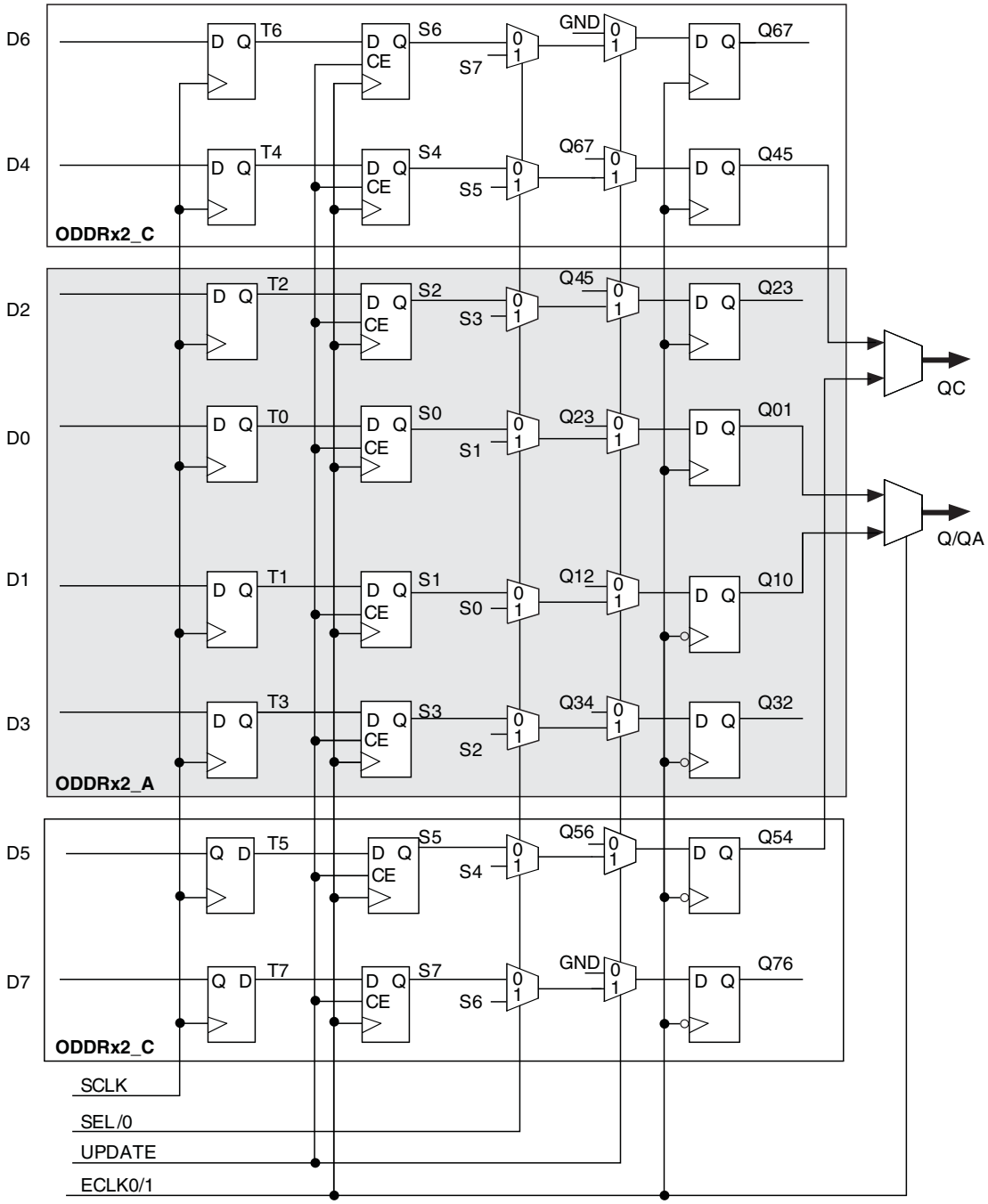
The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

Figure 2-11. Group of Four Programmable I/O Cells



Notes:
1. Input gearbox is available only in PIC on the bottom edge of MachXO2-640U, MachXO2-1200/U and larger devices.
2. Output gearbox is available only in PIC on the top edge of MachXO2-640U, MachXO2-1200/U and larger devices.

Figure 2-17. Output Gearbox



More information on the output gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.

Figure 2-18. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 Banks

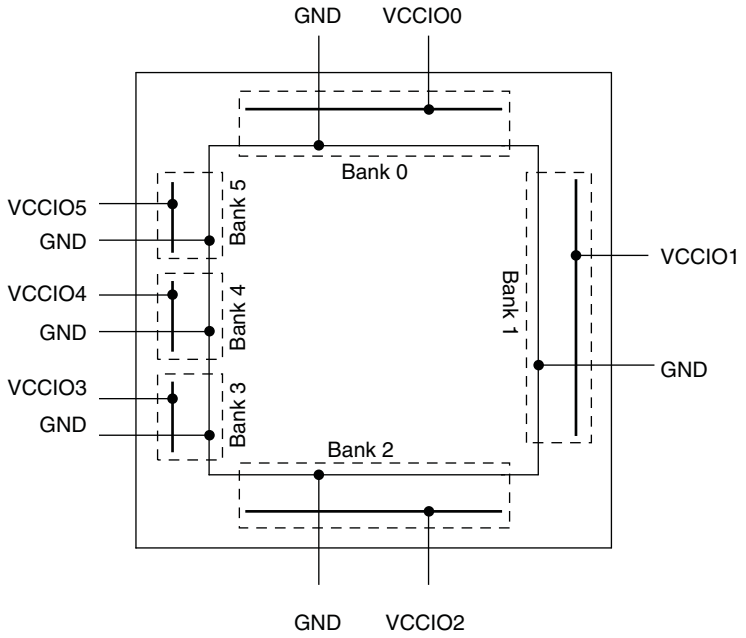
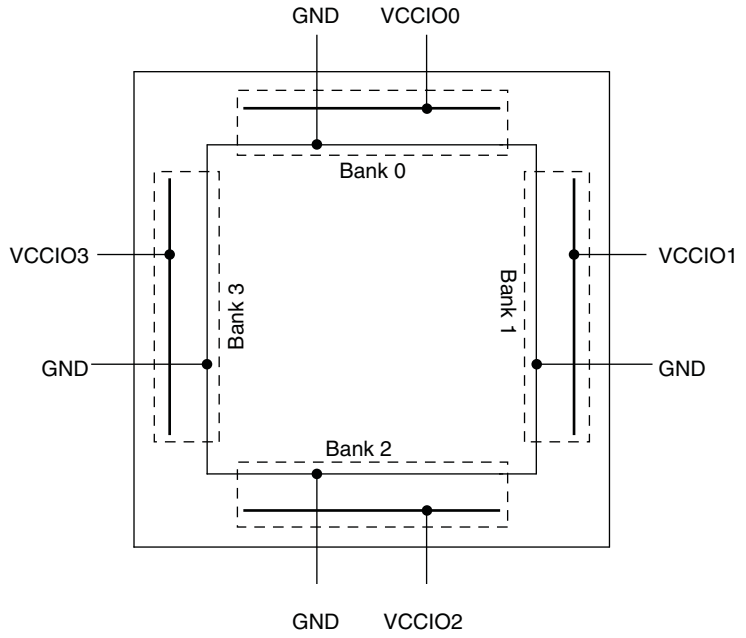


Figure 2-19. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks



For more details on these embedded functions, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

User Flash Memory (UFM)

MachXO2-640/U and higher density devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I^2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

Standby Mode and Power Saving Options

MachXO2 devices are available in three options for maximum flexibility: ZE, HC and HE devices. The ZE devices have ultra low static and dynamic power consumption. These devices use a 1.2 V core voltage that further reduces power consumption. The HC and HE devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the HE devices operate at 1.2 V V_{CC}.

MachXO2 devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO2 devices support an ultra low power Stand-by mode. While most of these features are available in all three device types, these features are mainly intended for use with MachXO2 ZE devices to manage power consumption.

In the stand-by mode the MachXO2 devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I^2C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO2 devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

Table 2-18. MachXO2 Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe V_{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1198, Power Estimation and Management for MachXO2 Devices.

Power On Reset

MachXO2 devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the V_{PORUP} level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices), V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators (HC devices), V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time ($t_{REFRESH}$) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min) they should not shut down the bandgap or POR circuit.

Static Supply Current – ZE Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO2-256ZE	18	µA
		LCMXO2-640ZE	28	µA
		LCMXO2-1200ZE	56	µA
		LCMXO2-2000ZE	80	µA
		LCMXO2-4000ZE	124	µA
		LCMXO2-7000ZE	189	µA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	1	µA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off. To estimate the impact of turning each of these items on, please refer to the following table or for more detail with your specific design use the Power Calculator tool.
3. Frequency = 0 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Static Power Consumption Contribution of Different Components – ZE Devices

The table below can be used for approximating static power consumption. For a more accurate power analysis for your design please use the Power Calculator tool.

Symbol	Parameter	Typ.	Units
I_{DCBG}	Bandgap DC power contribution	101	µA
I_{DCPOR}	POR DC power contribution	38	µA
$I_{DCIOBANKCONTROLLER}$	DC power contribution per I/O bank controller	143	µA

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HPLL}	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	0.41	—	0.48	—	0.55	—	ns
		MachXO2-2000HC-HE	0.42	—	0.49	—	0.56	—	ns
		MachXO2-4000HC-HE	0.43	—	0.50	—	0.58	—	ns
		MachXO2-7000HC-HE	0.46	—	0.54	—	0.62	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	2.88	—	3.19	—	3.72	—	ns
		MachXO2-2000HC-HE	2.87	—	3.18	—	3.70	—	ns
		MachXO2-4000HC-HE	2.96	—	3.28	—	3.81	—	ns
		MachXO2-7000HC-HE	3.05	—	3.35	—	3.87	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-2000HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-4000HC-HE	–0.87	—	–0.87	—	–0.87	—	ns
		MachXO2-7000HC-HE	–0.91	—	–0.91	—	–0.91	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.317	—	0.344	—	0.368	UI
t_{DVE}	Input Data Hold After CLK		0.742	—	0.702	—	0.668	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	All MachXO2 devices, all sides	0.566	—	0.560	—	0.538	—	ns
t_{HO}	Input Data Hold After CLK		0.778	—	0.879	—	1.090	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.316	—	0.342	—	0.364	UI
t_{DVE}	Input Data Hold After CLK		0.710	—	0.675	—	0.679	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.233	—	0.219	—	0.198	—	ns
t_{HO}	Input Data Hold After CLK		0.287	—	0.287	—	0.344	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz

Figure 3-5. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms

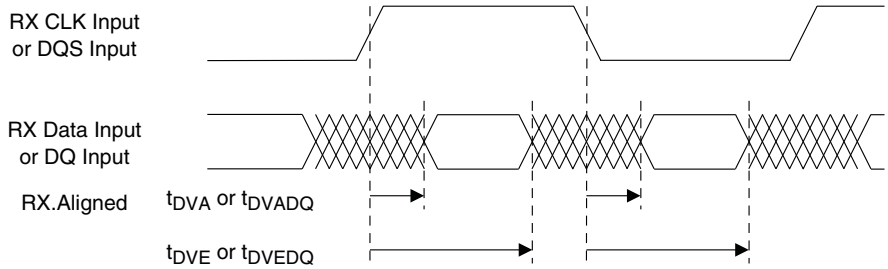


Figure 3-6. Receiver RX.CLK.Centered Waveforms

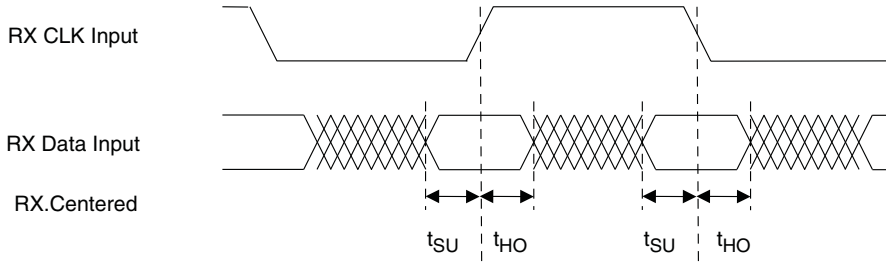


Figure 3-7. Transmitter TX.CLK.Aligned Waveforms

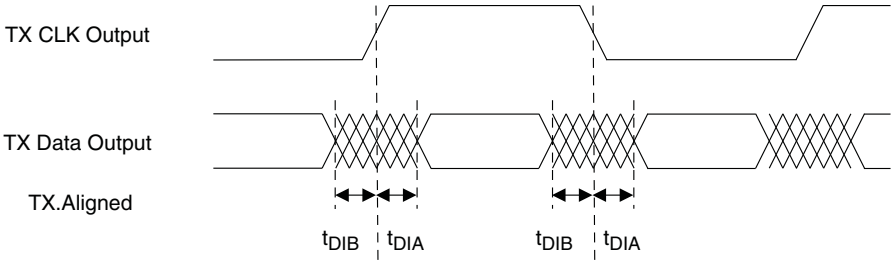
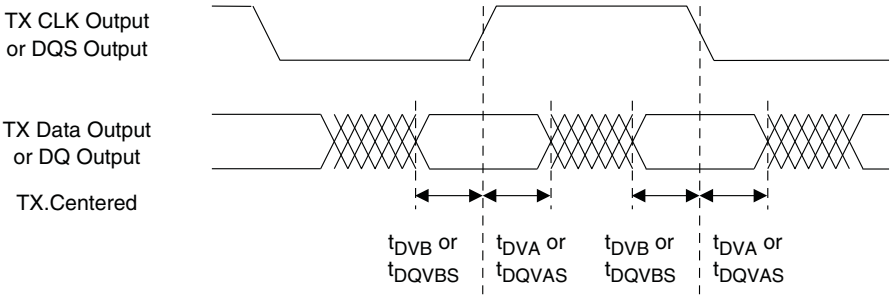


Figure 3-8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms



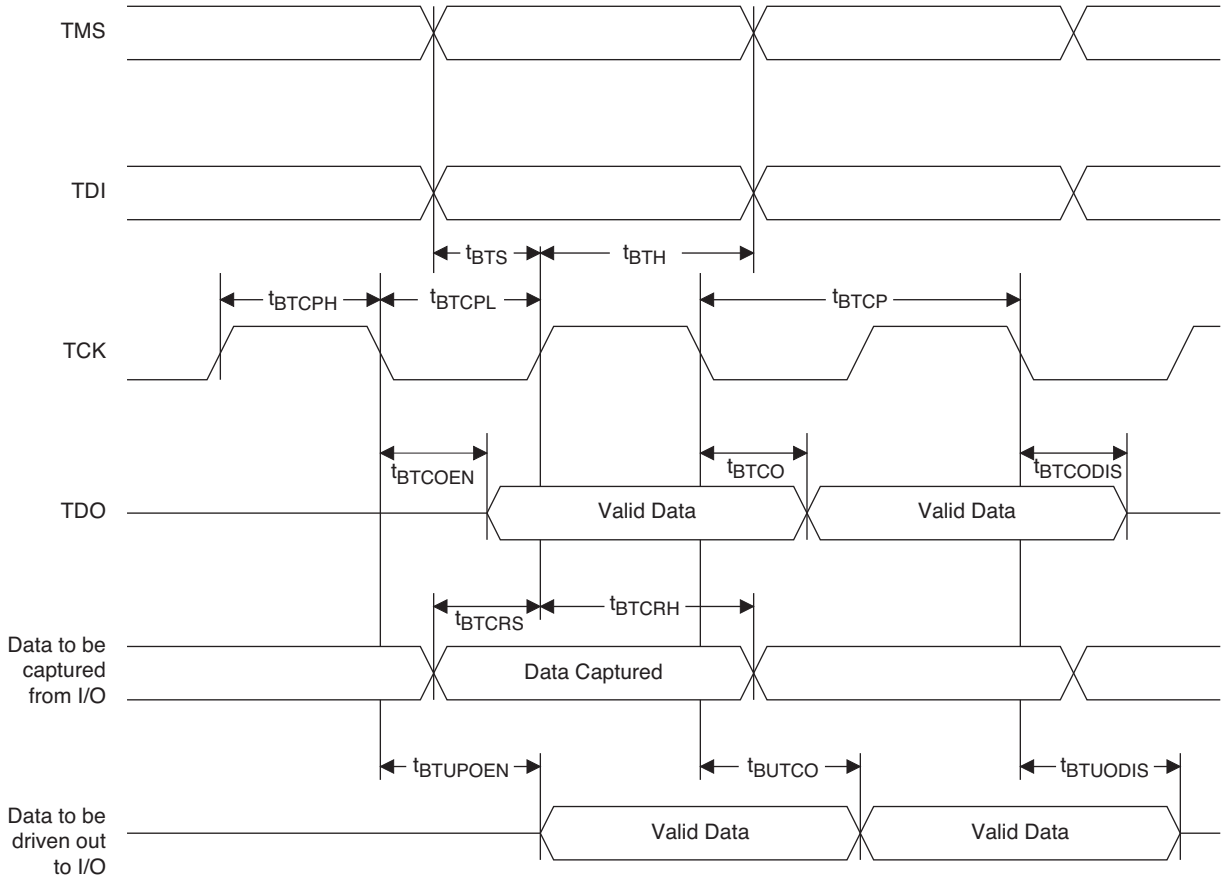
sysCLOCK PLL Timing (Continued)

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
t_{ROTATE_WD}	PHASESTEP Pulse Width		4	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide for more details.
5. At minimum $f_{PFD.}$ As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

Figure 3-12. JTAG Port Timing Waveforms



	MachXO2-4000							
	84 QFN	132 csBGA	144 TQFP	184 csBGA	256 caBGA	256 ftBGA	332 caBGA	484 fpBGA
General Purpose I/O per Bank								
Bank 0	27	25	27	37	50	50	68	70
Bank 1	10	26	29	37	52	52	68	68
Bank 2	22	28	29	39	52	52	70	72
Bank 3	0	7	9	10	16	16	24	24
Bank 4	9	8	10	12	16	16	16	16
Bank 5	0	10	10	15	20	20	28	28
Total General Purpose Single Ended I/O	68	104	114	150	206	206	274	278
Differential I/O per Bank								
Bank 0	13	13	14	18	25	25	34	35
Bank 1	4	13	14	18	26	26	34	34
Bank 2	11	14	14	19	26	26	35	36
Bank 3	0	3	4	4	8	8	12	12
Bank 4	4	4	5	6	8	8	8	8
Bank 5	0	5	5	7	10	10	14	14
Total General Purpose Differential I/O	32	52	56	72	103	103	137	139
Dual Function I/O	28	37	37	37	37	37	37	37
High-speed Differential I/O								
Bank 0	8	8	9	8	18	18	18	18
Gearboxes								
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	8	8	9	9	18	18	18	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	11	14	14	12	18	18	18	18
DQS Groups								
Bank 1	1	2	2	2	2	2	2	2
VCCIO Pins								
Bank 0	3	3	3	3	4	4	4	10
Bank 1	1	3	3	3	4	4	4	10
Bank 2	2	3	3	3	4	4	4	10
Bank 3	1	1	1	1	1	1	2	3
Bank 4	1	1	1	1	2	2	1	4
Bank 5	1	1	1	1	1	1	2	3
VCC	4	4	4	4	8	8	8	12
GND	4	10	12	16	24	24	27	48
NC	1	1	1	1	1	1	5	105
Reserved for configuration	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	84	132	144	184	256	256	332	484

For Further Information

For further information regarding logic signal connections for various packages please refer to the MachXO2 Device Pinout Files.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Users must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1198, Power Estimation and Management for MachXO2 Devices
- The Power Calculator tool is included with the Lattice design tools, or as a standalone download from www.latticesemi.com/software

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144C	6864	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-2TG144C	6864	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-3TG144C	6864	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-1BG256C	6864	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-2BG256C	6864	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-3BG256C	6864	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-1FTG256C	6864	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-2FTG256C	6864	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-3FTG256C	6864	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-1BG332C	6864	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-2BG332C	6864	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-3BG332C	6864	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-1FG484C	6864	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-2FG484C	6864	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-3FG484C	6864	1.2 V	–3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100CR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100CR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100CR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132CR1[1]	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132CR1[1]	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132CR1[1]	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144CR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144CR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144CR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200ZE-speed package CR1” are the same as the “LCMXO2-1200ZE-speed package C” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100C	2112	1.2 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-5TG100C	2112	1.2 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-6TG100C	2112	1.2 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-4TG144C	2112	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-5TG144C	2112	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-6TG144C	2112	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-4MG132C	2112	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-5MG132C	2112	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-6MG132C	2112	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-4BG256C	2112	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-5BG256C	2112	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-6BG256C	2112	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-4FTG256C	2112	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-5FTG256C	2112	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-6FTG256C	2112	1.2 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484C	2112	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-5FG484C	2112	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-6FG484C	2112	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4TG144C	4320	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-5TG144C	4320	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-6TG144C	4320	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-4MG132C	4320	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-5MG132C	4320	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-6MG132C	4320	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-4BG256C	4320	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4MG184C	4320	1.2 V	–4	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5MG184C	4320	1.2 V	–5	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-6MG184C	4320	1.2 V	–6	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5BG256C	4320	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-6BG256C	4320	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4FTG256C	4320	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-5FTG256C	4320	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-6FTG256C	4320	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-4BG332C	4320	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-5BG332C	4320	1.2 V	–5	Halogen-Free caBGA	332	COM

High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32I	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	IND
LCMXO2-256HC-5SG32I	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	IND
LCMXO2-256HC-6SG32I	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	IND
LCMXO2-256HC-4SG48I	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	IND
LCMXO2-256HC-5SG48I	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	IND
LCMXO2-256HC-6SG48I	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	IND
LCMXO2-256HC-4UMG64I	256	2.5 V / 3.3 V	–4	Halogen-Free ucBGA	64	IND
LCMXO2-256HC-5UMG64I	256	2.5 V / 3.3 V	–5	Halogen-Free ucBGA	64	IND
LCMXO2-256HC-6UMG64I	256	2.5 V / 3.3 V	–6	Halogen-Free ucBGA	64	IND
LCMXO2-256HC-4TG100I	256	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-256HC-5TG100I	256	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-256HC-6TG100I	256	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-256HC-4MG132I	256	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-256HC-5MG132I	256	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-256HC-6MG132I	256	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48I	640	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	IND
LCMXO2-640HC-5SG48I	640	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	IND
LCMXO2-640HC-6SG48I	640	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	IND
LCMXO2-640HC-4TG100I	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-640HC-5TG100I	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-640HC-6TG100I	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-640HC-4MG132I	640	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-640HC-5MG132I	640	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-640HC-6MG132I	640	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144I	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-640UHC-5TG144I	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-640UHC-6TG144I	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND

High Performance Industrial Grade Devices Without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100I	2112	1.2 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-5TG100I	2112	1.2 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-6TG100I	2112	1.2 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-4MG132I	2112	1.2 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-5MG132I	2112	1.2 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-6MG132I	2112	1.2 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-4TG144I	2112	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-5TG144I	2112	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-6TG144I	2112	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-4BG256I	2112	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-5BG256I	2112	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-6BG256I	2112	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-4FTG256I	2112	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-5FTG256I	2112	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-6FTG256I	2112	1.2 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484I	2112	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-5FG484I	2112	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-6FG484I	2112	1.2 V	–6	Halogen-Free fpBGA	484	IND

Date	Version	Section	Change Summary
May 2016	3.2	All	Moved designation for 84 QFN package information from 'Advanced' to 'Final'.
		Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added ‘Advanced’ 48 QFN package. — Revised footnote 6. — Added footnote 9.
		DC and Switching Characteristics	Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Added footnote 12.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Added footnote 12.
		Pinout Information	Updated the Signal Descriptions section. Added information on GND signal.
			Updated the Pinout Information Summary section. — Added ‘Advanced’ MachXO2-256 48 QFN values. — Added ‘Advanced’ MachXO2-640 48 QFN values. — Added footnote to GND. — Added footnotes 2 and 3.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added ‘Advanced’ SG48 package and revised footnote.
			Updated the Ordering Information section. — Added part numbers for ‘Advanced’ QFN 48 package.
March 2016	3.1	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 32 QFN value for XO2-1200. — Added 84 QFN (7 mm x 7 mm, 0.5 mm) package. — Modified package name to 100-pin TQFP. — Modified package name to 144-pin TQFP. — Added footnote.
		Architecture	Updated the Typical I/O Behavior During Power-up section. Removed reference to TN1202.
		DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications section. Revised $t_{DPPDONE}$ and $t_{DPPINIT}$ Max. values per PCN 03A-16, released March 2016.
		Pinout Information	Updated the Pinout Information Summary section. — Added MachXO2-1200 32 QFN values. — Added ‘Advanced’ MachXO2-4000 84 QFN values.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added ‘Advanced’ QN84 package and footnote.
			Updated the Ordering Information section. — Added part numbers for 1280 LUTs QFN 32 package. — Added part numbers for 4320 LUTs QFN 84 package.
March 2015	3.0	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Changed 64-ball ucBGA dimension.
		Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.

Date	Version	Section	Change Summary
May 2014	2.5	Architecture	Updated TransFR (Transparent Field Reconfiguration) section. Updated TransFR description for PLL use during background Flash programming.
February 2014	02.4	Introduction	Included the 49 WLCSP package in the MachXO2 Family Selection Guide table.
		Architecture	Added information to Standby Mode and Power Saving Options section.
		Pinout Information	Added the XO2-2000 49 WLCSP in the Pinout Information Summary table.
		Ordering Information	Added UW49 package in MachXO2 Part Number Description.
			Added and LCMXO2-2000ZE-1UWG49CTR in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging section.
			Added and LCMXO2-2000ZE-1UWG49ITR in Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section.
December 2013	02.3	Architecture	Updated information on CLKOS output divider in sysCLOCK Phase Locked Loops (PLLs) section.
		DC and Switching Characteristics	Updated Static Supply Current – ZE Devices table.
			Updated footnote 4 in sysIO Single-Ended DC Electrical Characteristics table; Updated V_{IL} Max. (V) data for LVCMOS 25 and LVCMOS 28.
			Updated V_{OS} test condition in sysIO Differential Electrical Characteristics - LVDS table.
September 2013	02.2	Architecture	Removed I^2C Clock-Stretching feature per PCN #10A-13.
			Removed information on PDPR memory in RAM Mode section.
			Updated Supported Input Standards table.
		DC and Switching Characteristics	Updated Power-On-Reset Voltage Levels table.
June 2013	02.1	Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.
			sysCLOCK Phase Locked Loops (PLLs) section – Added missing cross reference to sysCLOCK PLL Timing table.
		DC and Switching Characteristics	Added slew rate information to footnote 2 of the MachXO2 External Switching Characteristics – HC/HE Devices and the MachXO2 External Switching Characteristics – ZE Devices tables.
			Power-On-Reset Voltage Levels table – Added symbols.