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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	540
Number of Logic Elements/Cells	4320
Total RAM Bits	94208
Number of I/O	150
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	184-LFBGA, CSPBGA
Supplier Device Package	184-CSBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-4000he-4mg184i

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Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), preengineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I²C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external V_{CC} supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V_{CC} supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pulldown and bus-keeper features are controllable on a "per-pin" basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I²C port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE[™] modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.



ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

Routing

There are many resources provided in the MachXO2 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Each MachXO2 device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO2 architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO2-640U, MachXO2-1200/U and higher density devices have two edge clocks each on the top and bottom edges. Lower density devices have no edge clocks. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO2 devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO2 External Switching Characteristics table.

The primary clock signals for the MachXO2-256 and MachXO2-640 are generated from eight 17:1 muxes The available clock sources include eight I/O sources and 9 routing inputs. Primary clock signals for the MachXO2-640U, MachXO2-1200/U and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.



Figure 2-6. Secondary High Fanout Nets for MachXO2 Devices



sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The MachXO2-640U, MachXO2-1200/U and larger devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO2 sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO2 clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.



Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe V_{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1198, Power Estimation and Management for MachXO2 Devices.

Power On Reset

MachXO2 devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the V_{PORUP} level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices), V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators (HC devices), V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time (t_{REFRESH}) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tristate. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min) they should not shut down the bandgap or POR circuit.



Typical Building Block Function Performance – ZE Devices¹

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–3 Timing	Units
Basic Functions		
16-bit decoder	13.9	ns
4:1 MUX	10.9	ns
16:1 MUX	12.0	ns

Register-to-Register Performance

Function	–3 Timing	Units
Basic Functions		·
16:1 MUX	191	MHz
16-bit adder	134	MHz
16-bit counter	148	MHz
64-bit counter	77	MHz
Embedded Memory Functions	·	
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	90	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	214	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.



			_	-6 –5		_	-4		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
		MachXO2-1200HC-HE	0.41		0.48		0.55	—	ns
1	Clock to Data Hold – PIO Input	MachXO2-2000HC-HE	0.42		0.49		0.56	—	ns
THPLL	Register	MachXO2-4000HC-HE	0.43		0.50		0.58	—	ns
		MachXO2-7000HC-HE	0.46		0.54		0.62	—	ns
		MachXO2-1200HC-HE	2.88		3.19		3.72	—	ns
t	Clock to Data Setup – PIO	MachXO2-2000HC-HE	2.87		3.18		3.70	—	ns
^I SU_DELPLL	Delav	MachXO2-4000HC-HE	2.96		3.28		3.81	—	ns
	,	MachXO2-7000HC-HE	3.05		3.35		3.87	—	ns
		MachXO2-1200HC-HE	-0.83		-0.83		-0.83	—	ns
	Clock to Data Hold – PIO Input	MachXO2-2000HC-HE	-0.83		-0.83		-0.83	—	ns
^I H_DELPLL	Register with Input Data Delay	MachXO2-4000HC-HE	-0.87		-0.87		-0.87	—	ns
		MachXO2-7000HC-HE	-0.91	—	-0.91	—	-0.91	—	ns
Generic DDF	RX1 Inputs with Clock and Data	Aligned at Pin Using PC	LK Pin	for Cloc	k Input -	GDDR	(1_RX.S	CLK.Ali	gned ^{9, 12}
t _{DVA}	Input Data Valid After CLK			0.317	—	0.344	—	0.368	UI
t _{DVE}	Input Data Hold After CLK	All MachXO2 devices, all sides	0.742	—	0.702	—	0.668	—	UI
f _{DATA}	DDRX1 Input Data Speed		_	300	—	250	—	208	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency			150	—	125	—	104	MHz
Generic DDF	X1 Inputs with Clock and Data C	Centered at Pin Using PC	LK Pin f	or Clock	Input –	GDDRX	1_RX.SC	LK.Cen	tered ^{9, 12}
t _{SU}	Input Data Setup Before CLK		0.566		0.560		0.538	—	ns
t _{HO}	Input Data Hold After CLK	All MachXO2 devices,	0.778		0.879		1.090	—	ns
f _{DATA}	DDRX1 Input Data Speed	all sides		300		250		208	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency			150		125		104	MHz
Generic DDF	RX2 Inputs with Clock and Data	Aligned at Pin Using PC	LK Pin f	for Clock	k Input –	GDDR	(2_RX.E	CLK.Ali	gned ^{9, 12}
t _{DVA}	Input Data Valid After CLK		—	0.316		0.342		0.364	UI
t _{DVE}	Input Data Hold After CLK	MachXO2-640U,	0.710		0.675		0.679	—	UI
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	664	_	554	_	462	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency	bottom side only ¹¹		332		277		231	MHz
f _{SCLK}	SCLK Frequency			166		139	—	116	MHz
Generic DDF	X2 Inputs with Clock and Data C	Centered at Pin Using PC	LK Pin f	or Clock	Input –	GDDRX	2_RX.EC	LK.Cen	tered ^{9, 12}
t _{SU}	Input Data Setup Before CLK		0.233		0.219		0.198	—	ns
t _{HO}	Input Data Hold After CLK	MachXO2-640U	0.287	—	0.287	—	0.344	—	ns
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	664	_	554	_	462	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency	bottom side only ¹¹	—	332	—	277	—	231	MHz
f _{SCLK}	SCLK Frequency	1	—	166		139		116	MHz



			-	-6	_	5	_	-4	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
LPDDR ^{9, 12}	·	·			•	•			
t _{DVADQ}	Input Data Valid After DQS Input		_	0.369	_	0.395	_	0.421	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.529	_	0.530	_	0.527	_	UI
t _{DQVBS}	Output Data Invalid Before DQS Output	MachXO2-1200/U and	0.25	_	0.25		0.25	_	UI
t _{DQVAS}	Output Data Invalid After DQS Output	larger devices, right side only. ¹³	0.25	_	0.25	_	0.25	_	UI
f _{DATA}	MEM LPDDR Serial Data Speed		_	280	_	250	_	208	Mbps
f _{SCLK}	SCLK Frequency			140	—	125	—	104	MHz
f _{LPDDR}	LPDDR Data Transfer Rate		0	280	0	250	0	208	Mbps
DDR ^{9, 12}	•								
t _{DVADQ}	Input Data Valid After DQS Input		_	0.350	_	0.387	_	0.414	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.545	_	0.538		0.532	_	UI
t _{DQVBS}	Output Data Invalid Before DQS Output	MachXO2-1200/U and larger devices, right	0.25	_	0.25	_	0.25	_	UI
t _{DQVAS}	Output Data Invalid After DQS Output	side only. ¹³	0.25	_	0.25	_	0.25	_	UI
f _{DATA}	MEM DDR Serial Data Speed			300	—	250	—	208	Mbps
f _{SCLK}	SCLK Frequency			150	—	125	—	104	MHz
f _{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps
DDR2 ^{9, 12}									
t _{DVADQ}	Input Data Valid After DQS Input		_	0.360	_	0.378	_	0.406	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.555	_	0.549	_	0.542	_	UI
t _{DQVBS}	Output Data Invalid Before DQS Output	MachXO2-1200/U and	0.25	_	0.25	_	0.25	_	UI
t _{DQVAS}	Output Data Invalid After DQS Output	larger devices, right side only. ¹³	0.25	_	0.25	_	0.25	_	UI
f _{DATA}	MEM DDR Serial Data Speed	1	—	300	—	250	—	208	Mbps
f _{SCLK}	SCLK Frequency	1	—	150	—	125	—	104	MHz
f _{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.

3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).

4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.

5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).

6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$.

7. The $t_{SU_{DEL}}$ and $t_{H_{DEL}}$ values use the SCLK_ZERHOLD default step size. Each step is 105 ps (-6), 113 ps (-5), 120 ps (-4).

8. This number for general purpose usage. Duty cycle tolerance is +/- 10%.

9. Duty cycle is +/-5% for system usage.

10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.

11. High-speed DDR and LVDS not supported in SG32 (32 QFN) packages.

12. Advance information for MachXO2 devices in 48 QFN packages.

13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.



MachXO2 External Switching Characteristics – ZE Devices^{1, 2, 3, 4, 5, 6, 7}

			-	-3	-	-2	-	1	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Clocks			1						
Primary Cloo	cks								
f _{MAX_PRI} ⁸	Frequency for Primary Clock Tree	All MachXO2 devices	_	150	_	125	_	104	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	1.00	_	1.20	_	1.40	_	ns
		MachXO2-256ZE	_	1250	—	1272		1296	ps
		MachXO2-640ZE		1161		1183		1206	ps
	Primary Clock Skew Within a	MachXO2-1200ZE	_	1213		1267		1322	ps
^t SKEW_PRI	Device	MachXO2-2000ZE		1204		1250		1296	ps
		MachXO2-4000ZE		1195		1233		1269	ps
		MachXO2-7000ZE		1243		1268		1296	ps
Edge Clock									
f _{MAX_EDGE} ⁸	Frequency for Edge Clock	MachXO2-1200 and larger devices	_	210	_	175	_	146	MHz
Pin-LUT-Pin	Propagation Delay		1	1	1	1	1	1	
t _{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	_	9.35	_	9.78	_	10.21	ns
General I/O	Pin Parameters (Using Primary	Clock without PLL)	I	I	I	I	I		
		MachXO2-256ZE		10.46	—	10.86	—	11.25	ns
		MachXO2-640ZE	_	10.52	—	10.92		11.32	ns
	Clock to Output – PIO Output	MachXO2-1200ZE	_	11.24		11.68		12.12	ns
^t CO	Register	MachXO2-2000ZE	_	11.27		11.71		12.16	ns
		MachXO2-4000ZE	_	11.28		11.78		12.28	ns
		MachXO2-7000ZE		11.22		11.76		12.30	ns
		MachXO2-256ZE	-0.21		-0.21		-0.21		ns
		MachXO2-640ZE	-0.22		-0.22		-0.22	—	ns
	Clock to Data Setup – PIO	MachXO2-1200ZE	-0.25	—	-0.25	—	-0.25	_	ns
t _{SU}	Input Register	MachXO2-2000ZE	-0.27		-0.27		-0.27	_	ns
		MachXO2-4000ZE	-0.31		-0.31		-0.31	_	ns
		MachXO2-7000ZE	-0.33		-0.33		-0.33	_	ns
		MachXO2-256ZE	3.96	—	4.25	—	4.65	—	ns
		MachXO2-640ZE	4.01		4.31		4.71	_	ns
+	Clock to Data Hold – PIO Input	MachXO2-1200ZE	3.95		4.29	_	4.73	—	ns
Ч	Register	MachXO2-2000ZE	3.94		4.29		4.74	_	ns
		MachXO2-4000ZE	3.96		4.36		4.87	_	ns
		MachXO2-7000ZE	3.93	_	4.37	_	4.91		ns

Over Recommended Operating Conditions



			-	-3	-	-2	-	1	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Generic DDR4	Inputs with Clock and Data Cer	ntered at Pin Using PC	LK Pin fo	or Clock	Input –	GDDRX4	LRX.EC	LK.Cent	ered ^{9, 12}
t _{SU}	Input Data Setup Before ECLK		0.434		0.535		0.630	—	ns
t _{HO}	Input Data Hold After ECLK	MachXO2-640U,	0.385		0.395		0.463	—	ns
f _{DATA}	DDRX4 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	420	_	352	_	292	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency	bottom side only'		210		176	—	146	MHz
f _{SCLK}	SCLK Frequency		—	53		44	—	37	MHz
7:1 LVDS Inp	uts – GDDR71_RX.ECLK.7.1 ^{9, 1}	2							
t _{DVA}	Input Data Valid After ECLK		—	0.307		0.316	—	0.326	UI
t _{DVE}	Input Data Hold After ECLK		0.662		0.650		0.649	—	UI
f _{DATA}	DDR71 Serial Input Data Speed	MachXO2-640U, MachXO2-1200/U	—	420	_	352	_	292	Mbps
f _{DDR71}	DDR71 ECLK Frequency	and larger devices,		210		176	—	146	MHz
f _{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		_	60	_	50	_	42	MHz
Generic DDR	Outputs with Clock and Data A	ligned at Pin Using PC	LK Pin f	for Clock	k Input –	GDDRX	(1_TX.S	CLK.Aliç	gned ^{9, 12}
t _{DIA}	Output Data Invalid After CLK Output		—	0.850	—	0.910	—	0.970	ns
t _{DIB}	Output Data Invalid Before CLK Output	All MachXO2 devices, all sides		0.850	_	0.910	_	0.970	ns
f _{DATA}	DDRX1 Output Data Speed			140	—	116		98	Mbps
f _{DDRX1}	DDRX1 SCLK frequency			70		58		49	MHz
Generic DDR	Outputs with Clock and Data Ce	ntered at Pin Using PC	LK Pin f	or Clock	Input –	GDDRX	1_TX.SC	LK.Cen	tered ^{9, 12}
t _{DVB}	Output Data Valid Before CLK Output		2.720	_	3.380	_	4.140	_	ns
t _{DVA}	Output Data Valid After CLK Output	All MachXO2	2.720	_	3.380	_	4.140	_	ns
f _{DATA}	DDRX1 Output Data Speed	devices, all sides		140	—	116		98	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)			70	_	58	_	49	MHz
Generic DDR	X2 Outputs with Clock and Data	Aligned at Pin Using P	CLK Pin	for Cloc	k Input	- GDDR	X2_TX.E	CLK.Ali	gned ^{9, 12}
t _{DIA}	Output Data Invalid After CLK Output			0.270	_	0.300	_	0.330	ns
t _{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U	_	0.270	_	0.300	_	0.330	ns
f _{DATA}	DDRX2 Serial Output Data Speed	and larger devices, top side only		280	_	234	_	194	Mbps
f _{DDRX2}	DDRX2 ECLK frequency	1	—	140	—	117	—	97	MHz
f _{SCLK}	SCLK Frequency			70		59	_	49	MHz



			_	-3	-	2	_	-1	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
LPDDR ^{9, 12}			1						
t _{DVADQ}	Input Data Valid After DQS Input			0.349	_	0.381	_	0.396	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.665	_	0.630		0.613	_	UI
t _{DQVBS}	Output Data Invalid Before DQS Output	MachXO2-1200/U	0.25	_	0.25		0.25	_	UI
t _{DQVAS}	Output Data Invalid After DQS Output	and larger devices, right side only. ¹³	0.25	_	0.25	_	0.25	_	UI
f _{DATA}	MEM LPDDR Serial Data Speed		_	120	_	110	_	96	Mbps
f _{SCLK}	SCLK Frequency		—	60		55		48	MHz
f _{LPDDR}	LPDDR Data Transfer Rate		0	120	0	110	0	96	Mbps
DDR ^{9, 12}	•	•							
t _{DVADQ}	Input Data Valid After DQS Input			0.347	_	0.374	_	0.393	UI
t _{DVEDQ}	Input Data Hold After DQS Input	-	0.665	_	0.637		0.616	_	UI
t _{DQVBS}	Output Data Invalid Before DQS Output	MachXO2-1200/U	0.25	_	0.25		0.25	_	UI
t _{DQVAS}	Output Data Invalid After DQS Output	right side only. ¹³	0.25	_	0.25	_	0.25	_	UI
f _{DATA}	MEM DDR Serial Data Speed			140	_	116		98	Mbps
f _{SCLK}	SCLK Frequency			70		58	—	49	MHz
f _{MEM DDR}	MEM DDR Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps
DDR2 ^{9, 12}	•		1	1	1	1	1	1	
t _{DVADQ}	Input Data Valid After DQS Input		_	0.372	_	0.394	_	0.410	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.690	_	0.658	_	0.618	_	UI
t _{DQVBS}	Output Data Invalid Before DQS Output	MachXO2-1200/U	0.25	_	0.25	_	0.25	_	UI
t _{DQVAS}	Output Data Invalid After DQS Output	and larger devices, right side only. ¹³	0.25	_	0.25	_	0.25	_	UI
f _{DATA}	MEM DDR Serial Data Speed	1	—	140	—	116		98	Mbps
f _{SCLK}	SCLK Frequency	1	<u> </u>	70	—	58		49	MHz
f _{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pf load, fast slew rate.

3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).

4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.

5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).

6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$.

7. The $t_{SU_{DEL}}$ and $t_{H_{DEL}}$ values use the SCLK_ZERHOLD default step size. Each step is 167 ps (-3), 182 ps (-2), 195 ps (-1).

8. This number for general purpose usage. Duty cycle tolerance is +/-10%.

9. Duty cycle is +/-5% for system usage.

10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.

11. High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.

12. Advance information for MachXO2 devices in 48 QFN packages.

13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.



Figure 3-9. GDDR71 Video Timing Waveforms



Figure 3-10. Receiver GDDR71_RX. Waveforms



Figure 3-11. Transmitter GDDR71_TX. Waveforms





MachXO2 Family Data Sheet Ordering Information

March 2017

Data Sheet DS1035

MachXO2 Part Number Description



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High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32C	256	2.5 V / 3.3 V	-4	Halogen-Free QFN	32	COM
LCMXO2-256HC-5SG32C	256	2.5 V / 3.3 V	-5	Halogen-Free QFN	32	COM
LCMXO2-256HC-6SG32C	256	2.5 V / 3.3 V	-6	Halogen-Free QFN	32	COM
LCMXO2-256HC-4SG48C	256	2.5 V / 3.3 V	-4	Halogen-Free QFN	48	COM
LCMXO2-256HC-5SG48C	256	2.5 V / 3.3 V	-5	Halogen-Free QFN	48	COM
LCMXO2-256HC-6SG48C	256	2.5 V / 3.3 V	-6	Halogen-Free QFN	48	COM
LCMXO2-256HC-4UMG64C	256	2.5 V / 3.3 V	-4	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-5UMG64C	256	2.5 V / 3.3 V	-5	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-6UMG64C	256	2.5 V / 3.3 V	-6	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-4TG100C	256	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-256HC-5TG100C	256	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-256HC-6TG100C	256	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-256HC-4MG132C	256	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-256HC-5MG132C	256	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-256HC-6MG132C	256	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48C	640	2.5 V / 3.3 V	-4	Halogen-Free QFN	48	COM
LCMXO2-640HC-5SG48C	640	2.5 V / 3.3 V	-5	Halogen-Free QFN	48	COM
LCMXO2-640HC-6SG48C	640	2.5 V / 3.3 V	-6	δ Halogen-Free QFN		COM
LCMXO2-640HC-4TG100C	640	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-640HC-5TG100C	640	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-640HC-6TG100C	640	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-640HC-4MG132C	640	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-640HC-5MG132C	640	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-640HC-6MG132C	640	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144C	640	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-5TG144C	640	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-6TG144C	640	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	COM



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-6BG332C	4320	1.2 V	-6	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-4FG484C	4320	1.2 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-5FG484C	4320	1.2 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-6FG484C	4320	1.2 V	-6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144C	6864	1.2 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-5TG144C	6864	1.2 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-6TG144C	6864	1.2 V	-6	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-4BG256C	6864	1.2 V	-4	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-5BG256C	6864	1.2 V	-5	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-6BG256C	6864	1.2 V	-6	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-4FTG256C	6864	1.2 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-5FTG256C	6864	1.2 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-6FTG256C	6864	1.2 V	-6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-4BG332C	6864	1.2 V	-4	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-5BG332C	6864	1.2 V	-5	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-6BG332C	6864	1.2 V	-6	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-4FG484C	6864	1.2 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-5FG484C	6864	1.2 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-6FG484C	6864	1.2 V	-6	Halogen-Free fpBGA	484	COM



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100IR11	1280	1.2 V	-1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100IR11	1280	1.2 V	-2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100IR11	1280	1.2 V	-3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132IR1 ¹	1280	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132IR1 ¹	1280	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132IR11	1280	1.2 V	-3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144IR11	1280	1.2 V	-1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144IR11	1280	1.2 V	-2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144IR11	1280	1.2 V	-3	Halogen-Free TQFP	144	IND

1. Specifications for the "LCMXO2-1200ZE-speed package IR1" are the same as the "LCMXO2-1200ZE-speed package I" devices respectively, except as specified in the R1 Device Specifications section of this data sheet.



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32I	1280	2.5 V / 3.3 V	-4	Halogen-Free QFN	32	IND
LCMXO2-1200HC-5SG32I	1280	2.5 V / 3.3 V	-5	Halogen-Free QFN	32	IND
LCMXO2-1200HC-6SG32I	1280	2.5 V / 3.3 V	-6	Halogen-Free QFN	32	IND
LCMXO2-1200HC-4TG100I	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100I	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100I	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132I	1280	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132I	1280	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132I	1280	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144I	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144I	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144I	1280	2.5 V/ 3.3 V	-6	Halogen-Free TQFP	144	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256I	1280	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-5FTG256I	1280	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-6FTG256I	1280	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100I	2112	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-5TG100I	2112	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-6TG100I	2112	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-4MG132I	2112	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-5MG132I	2112	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-6MG132I	2112	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-4TG144I	2112	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-5TG144I	2112	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-6TG144I	2112	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-4BG256I	2112	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-5BG256I	2112	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-6BG256I	2112	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-4FTG256I	2112	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-5FTG256I	2112	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-6FTG256I	2112	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484I	2112	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-5FG484I	2112	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-6FG484I	2112	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	IND



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84I	4320	2.5 V / 3.3 V	-4	Halogen-Free QFN	84	IND
LCMXO2-4000HC-5QN84I	4320	2.5 V / 3.3 V	-5	Halogen-Free QFN	84	IND
LCMXO2-4000HC-6QN84I	4320	2.5 V / 3.3 V	-6	Halogen-Free QFN	84	IND
LCMXO2-4000HC-4TG144I	4320	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-5TG144I	4320	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-6TG144I	4320	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-4MG132I	4320	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-5MG132I	4320	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-6MG132I	4320	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-4BG256I	4320	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-5BG256I	4320	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-6BG256I	4320	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-4FTG256I	4320	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-5FTG256I	4320	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-6FTG256I	4320	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-4BG332I	4320	2.5 V / 3.3 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-5BG332I	4320	2.5 V / 3.3 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-6BG332I	4320	2.5 V / 3.3 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-4FG484I	4320	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-5FG484I	4320	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-6FG484I	4320	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144I	6864	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-5TG144I	6864	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-6TG144I	6864	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-4BG256I	6864	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-5BG256I	6864	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-6BG256I	6864	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-4FTG256I	6864	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-5FTG256I	6864	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-6FTG256I	6864	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-4BG332I	6864	2.5 V / 3.3 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-5BG332I	6864	2.5 V / 3.3 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-6BG332I	6864	2.5 V / 3.3 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-4FG400I	6864	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-5FG400I	6864	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-6FG400I	6864	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-4FG484I	6864	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-5FG484I	6864	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-6FG484I	6864	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	IND



R1 Device Specifications

The LCMXO2-1200ZE/HC "R1" devices have the same specifications as their Standard (non-R1) counterparts except as listed below. For more details on the R1 to Standard migration refer to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard Non-R1) Devices.

- The User Flash Memory (UFM) cannot be programmed through the internal WISHBONE interface. It can still be programmed through the JTAG/SPI/I²C ports.
- The on-chip differential input termination resistor value is higher than intended. It is approximately 200Ω as opposed to the intended 100Ω. It is recommended to use external termination resistors for differential inputs. The on-chip termination resistors can be disabled through Lattice design software.
- Soft Error Detection logic may not produce the correct result when it is run for the first time after configuration. To use this feature, discard the result from the first operation. Subsequent operations will produce the correct result.
- Under certain conditions, IIH exceeds data sheet specifications. The following table provides more details:

Condition	Clamp	Pad Rising IIH Max.	Pad Falling IIH Min.	Steady State Pad High IIH	Steady State Pad Low IIL
VPAD > VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD = VCCIO	ON	10 µA	–10 μA	10 µA	10 µA
VPAD = VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD < VCCIO	OFF	10 µA	–10 μA	10 µA	10 µA

- The user SPI interface does not operate correctly in some situations. During master read access and slave write access, the last byte received does not generate the RRDY interrupt.
- In GDDRX2, GDDRX4 and GDDR71 modes, ECLKSYNC may have a glitch in the output under certain conditions, leading to possible loss of synchronization.
- When using the hard I²C IP core, the I²C status registers I2C_1_SR and I2C_2_SR may not update correctly.
- PLL Lock signal will glitch high when coming out of standby. This glitch lasts for about 10 μsec before returning low.
- Dual boot only available on HC devices, requires tying VCC and VCCIO2 to the same 3.3 V or 2.5 V supply.



MachXO2 Family Data Sheet Revision History

March 2017

Data Sheet DS1035

Date	Version	Section	Change Summary	
March 2017	3.3	DC and Switching Characteristics	Updated the Absolute Maximum Ratings section. Added standards.	
			Updated the sysIO Recommended Operating Conditions section. Added standards.	
			Updated the sysIO Single-Ended D tion. Added standards. Updated the MachXO2 External Sy Devices section. Under 7:1 LVDS Outputs – GDDR7 D _{VA} parameters were changed to D descriptions were also modified.	Updated the sysIO Single-Ended DC Electrical Characteristics sec- tion. Added standards.
				Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA} . The parameter descriptions were also modified.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA} . The parameter descriptions were also modified.	
			Updated the sysCONFIG Port Timing Specifications section. Corrected the t_{INITL} units from ns to μ s.	
		Pinout Information	Updated the Signal Descriptions section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals.	
			Updated the Pinout Information Summary section. Added footnote to MachXO2-1200 32 QFN.	
		Ordering Information	Updated the MachXO2 Part Number Description section. Corrected the MG184, BG256, FTG256 package information. Added "(0.8 mm Pitch)" to BG332.	
			Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. — Updated LCMXO2-1200ZE-1UWG25ITR50 footnote. — Corrected footnote numbering typo. — Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2- 2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s.	

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Date	Version	Section	Change Summary
May 2016	3.2	All	Moved designation for 84 QFN package information from 'Advanced' to 'Final'.
		Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 'Advanced' 48 QFN package. — Revised footnote 6. — Added footnote 9.
		DC and Switching Characteristics	Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Added footnote 12.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Added footnote 12.
		Pinout Information	Updated the Signal Descriptions section. Added information on GND signal.
			Updated the Pinout Information Summary section. — Added 'Advanced' MachXO2-256 48 QFN values. — Added 'Advanced' MachXO2-640 48 QFN values. — Added footnote to GND. — Added footnotes 2 and 3.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added 'Advanced' SG48 package and revised footnote.
			Updated the Ordering Information section. — Added part numbers for 'Advanced' QFN 48 package.
March 2016	3.1	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 32 QFN value for XO2-1200. — Added 84 QFN (7 mm x 7 mm, 0.5 mm) package. — Modified package name to 100-pin TQFP. — Modified package name to 144-pin TQFP. — Added footnote.
		Architecture	Updated the Typical I/O Behavior During Power-up section. Removed reference to TN1202.
		DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications section. Revised t _{DPPDONE} and t _{DPPINIT} Max. values per PCN 03A-16, released March 2016.
		Pinout Information	Updated the Pinout Information Summary section. — Added MachXO2-1200 32 QFN values. — Added 'Advanced' MachXO2-4000 84 QFN values.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added 'Advanced' QN84 package and footnote.
			Updated the Ordering Information section. — Added part numbers for 1280 LUTs QFN 32 package. — Added part numbers for 4320 LUTs QFN 84 package.
March 2015	3.0	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Changed 64-ball ucBGA dimension.
		Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.