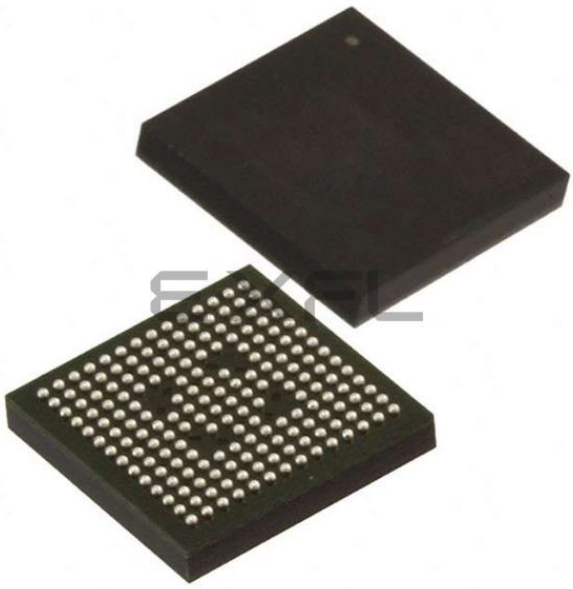
# Lattice Semiconductor Corporation - LCMXO2-4000HE-5MG184I Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 540 |
| Number of Logic Elements/Cells | 4320 |
| Total RAM Bits | 94208 |
| Number of I/O | 150 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 184-LFBGA, CSPBGA |
| Supplier Device Package | 184-CSBGA (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-4000he-5mg184i |

# Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, $I^2C$ controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external $V_{CC}$ supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external $V_{CC}$ supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis.

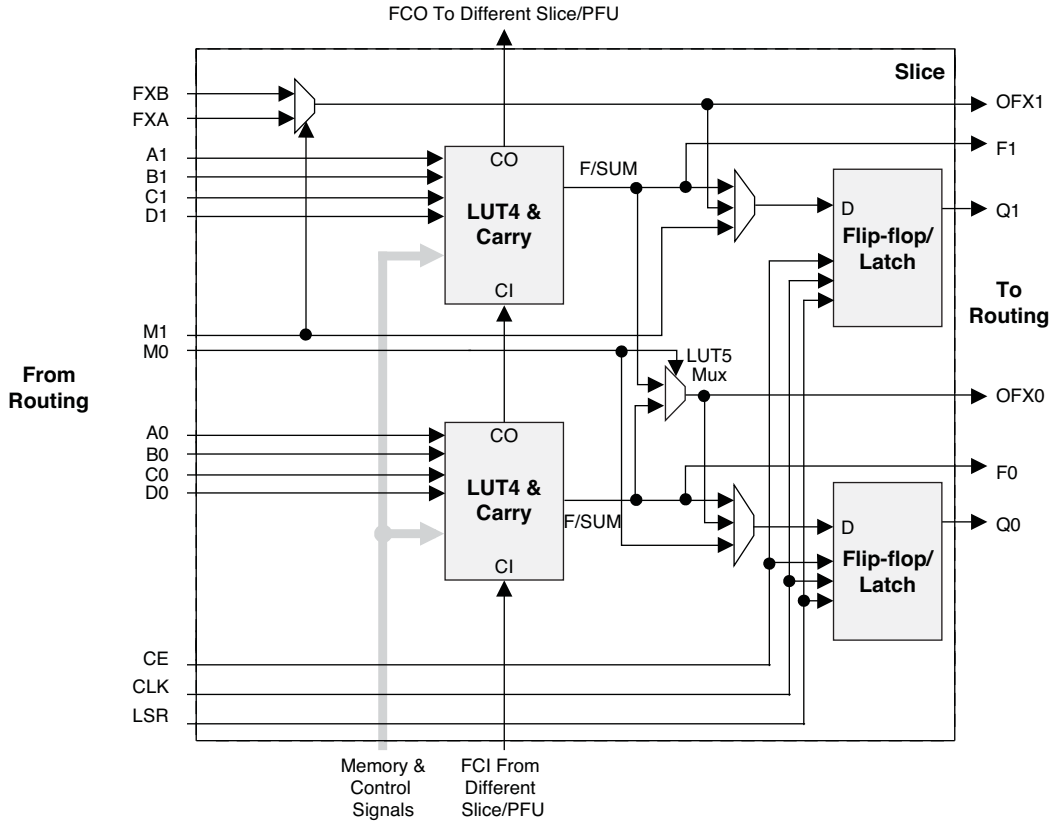
A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the $I^2C$ port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

*Figure 2-4. Slice Diagram*




For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

*Table 2-2. Slice Signal Descriptions*

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0/M1 | Multi-purpose input |
| Input | Control signal | CE | Clock enable |
| Input | Control signal | LSR | Local set/reset |
| Input | Control signal | CLK | System clock |
| Input | Inter-PFU signal | FCIN | Fast carry in[1] |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register outputs |
| Output | Data signals | OFX0 | Output of a LUT5 MUX |
| Output | Data signals | OFX1 | Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice |
| Output | Inter-PFU signal | FCO | Fast carry out[1] |

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

## Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

**Logic Mode**
In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

**Ripple Mode**
Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  — A greater-than-or-equal-to B
  — A not-equal-to B
  — A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

## RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO2 devices support distributed memory initialization.

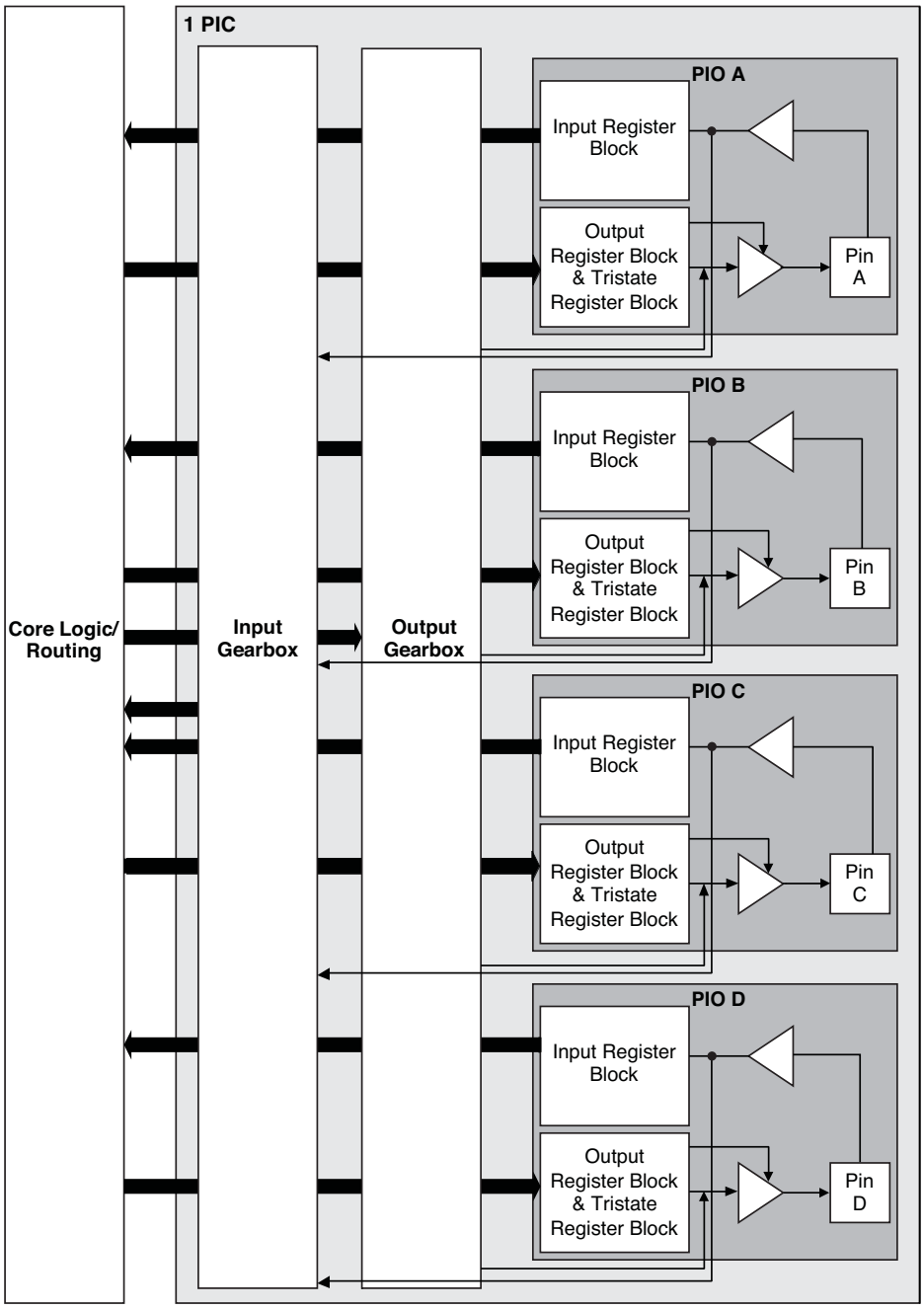
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO2 devices, please see TN1201, Memory Usage Guide for MachXO2 Devices.

***Table 2-3. Number of Slices Required For Implementing Distributed RAM***

| | SPR 16x4 | PDPR 16x4 |
|---|---|---|
| Number of slices | 3 | 3 |

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

*Figure 2-11. Group of Four Programmable I/O Cells*




Notes:
1. Input gearbox is available only in PIC on the bottom edge of MachXO2-640U, MachXO2-1200/U and larger devices.
2. Output gearbox is available only in PIC on the top edge of MachXO2-640U, MachXO2-1200/U and larger devices.

MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 devices contain three types of sysIO buffer pairs.

1. **Left and Right sysIO Buffer Pairs**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential and referenced input buffers.

2. **Bottom sysIO Buffer Pairs**
   The sysIO buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential and referenced input buffers. Only the I/Os on the bottom banks have programmable PCI clamps and differential input termination. The PCI clamp is enabled after $V_{CC}$ and $V_{CCIO}$ are at valid operating levels and the device has been configured.

3. **Top sysIO Buffer Pairs**
   The sysIO buffer pairs in the top bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential and referenced I/O buffers. Half of the sysIO buffer pairs on the top edge have true differential outputs. The sysIO buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver. The referenced input buffer can also be configured as a differential input buffer.

## Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when $V_{CC}$ and $V_{CCIO0}$ have reached $V_{PORUP}$ level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-down to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to $V_{CCIO}$ as the default functionality). The I/O pins will maintain the blank configuration until $V_{CC}$ and $V_{CCIO}$ (for I/O banks containing configuration I/Os) have reached $V_{PORUP}$ levels at which time the I/Os will take on the user-configured settings only after a proper download/configuration.

## Supported Standards

The MachXO2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL, and PCI. The buffer supports the LVTTL, PCI, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO2-640U, MachXO2-1200/U and higher devices support on-chip LVDS output buffers on approximately 50% of the I/Os on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO2 devices. PCI support is provided in the bottom bank of theMachXO2-640U, MachXO2-1200/U and higher density devices. Table 2-11 summarizes the I/O characteristics of the MachXO2 PLDs.

Tables 2-11 and 2-12 show the I/O standards (together with their supply and reference voltages) supported by the MachXO2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1202, MachXO2 sysIO Usage Guide.

For more details on these embedded functions, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

## User Flash Memory (UFM)

MachXO2-640/U and higher density devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, $I^2C$ and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

## Standby Mode and Power Saving Options

MachXO2 devices are available in three options for maximum flexibility: ZE, HC and HE devices. The ZE devices have ultra low static and dynamic power consumption. These devices use a 1.2 V core voltage that further reduces power consumption. The HC and HE devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V $V_{CC}$ and 3.3 V $V_{CC}$ while the HE devices operate at 1.2 V $V_{CC}$.

MachXO2 devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO2 devices support an ultra low power Stand-by mode. While most of these features are available in all three device types, these features are mainly intended for use with MachXO2 ZE devices to manage power consumption.

In the stand-by mode the MachXO2 devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate $I^2C$ or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO2 devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

# MachXO2 Family Data Sheet DC and Switching Characteristics

March 2017 Data Sheet DS1035

## Absolute Maximum Ratings[1, 2, 3]

| | MachXO2 ZE/HE (1.2 V) | MachXO2 HC (2.5 V / 3.3 V) |
|---|---|---|
| Supply Voltage $V_{CC}$ | –0.5 V to 1.32 V | –0.5 V to 3.75 V |
| Output Supply Voltage $V_{CCIO}$ | –0.5 V to 3.75 V | –0.5 V to 3.75 V |
| I/O Tri-state Voltage Applied[4, 5] | –0.5 V to 3.75 V | –0.5 V to 3.75 V |
| Dedicated Input Voltage Applied[4] | –0.5 V to 3.75 V | –0.5 V to 3.75 V |
| Storage Temperature (Ambient) | –55 °C to 125 °C | –55 °C to 125 °C |
| Junction Temperature ($T_J$) | –40 °C to 125 °C | –40 °C to 125 °C |

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to ($V_{IHMAX}$ + 2) volts is permitted for a duration of <20 ns.
5. The dual function $I^2C$ pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.

## Recommended Operating Conditions[1]

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{CC}$[1] | Core Supply Voltage for 1.2 V Devices | 1.14 | 1.26 | V |
| | Core Supply Voltage for 2.5 V / 3.3 V Devices | 2.375 | 3.6 | V |
| $V_{CCIO}$[1, 2, 3] | I/O Driver Supply Voltage | 1.14 | 3.6 | V |
| $t_{JCOM}$ | Junction Temperature Commercial Operation | 0 | 85 | °C |
| $t_{JIND}$ | Junction Temperature Industrial Operation | –40 | 100 | °C |

1. Like power supplies must be tied together. For example, if $V_{CCIO}$ and $V_{CC}$ are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. $V_{CCIO}$ pins of unused I/O banks should be connected to the $V_{CC}$ power supply on boards.

## Power Supply Ramp Rates[1]

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{RAMP}$ | Power supply ramp rates for all power supplies. | 0.01 | — | 100 | V/ms |

1. Assumes monotonic ramp rates.

# MachXO2 External Switching Characteristics – ZE Devices[1, 2, 3, 4, 5, 6, 7]

**Over Recommended Operating Conditions**

| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Clocks** | | | | | | | | | |
| **Primary Clocks** | | | | | | | | | |
| $f_{MAX\_PRI}$[8] | Frequency for Primary Clock Tree | All MachXO2 devices | — | 150 | — | 125 | — | 104 | MHz |
| $t_{W\_PRI}$ | Clock Pulse Width for Primary Clock | All MachXO2 devices | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| $t_{SKEW\_PRI}$ | Primary Clock Skew Within a Device | MachXO2-256ZE | — | 1250 | — | 1272 | — | 1296 | ps |
| | | MachXO2-640ZE | — | 1161 | — | 1183 | — | 1206 | ps |
| | | MachXO2-1200ZE | — | 1213 | — | 1267 | — | 1322 | ps |
| | | MachXO2-2000ZE | — | 1204 | — | 1250 | — | 1296 | ps |
| | | MachXO2-4000ZE | — | 1195 | — | 1233 | — | 1269 | ps |
| | | MachXO2-7000ZE | — | 1243 | — | 1268 | — | 1296 | ps |
| **Edge Clock** | | | | | | | | | |
| $f_{MAX\_EDGE}$[8] | Frequency for Edge Clock | MachXO2-1200 and larger devices | — | 210 | — | 175 | — | 146 | MHz |
| **Pin-LUT-Pin Propagation Delay** | | | | | | | | | |
| $t_{PD}$ | Best case propagation delay through one LUT-4 | All MachXO2 devices | — | 9.35 | — | 9.78 | — | 10.21 | ns |
| **General I/O Pin Parameters (Using Primary Clock without PLL)** | | | | | | | | | |
| $t_{CO}$ | Clock to Output – PIO Output Register | MachXO2-256ZE | — | 10.46 | — | 10.86 | — | 11.25 | ns |
| | | MachXO2-640ZE | — | 10.52 | — | 10.92 | — | 11.32 | ns |
| | | MachXO2-1200ZE | — | 11.24 | — | 11.68 | — | 12.12 | ns |
| | | MachXO2-2000ZE | — | 11.27 | — | 11.71 | — | 12.16 | ns |
| | | MachXO2-4000ZE | — | 11.28 | — | 11.78 | — | 12.28 | ns |
| | | MachXO2-7000ZE | — | 11.22 | — | 11.76 | — | 12.30 | ns |
| $t_{SU}$ | Clock to Data Setup – PIO Input Register | MachXO2-256ZE | –0.21 | — | –0.21 | — | –0.21 | — | ns |
| | | MachXO2-640ZE | –0.22 | — | –0.22 | — | –0.22 | — | ns |
| | | MachXO2-1200ZE | –0.25 | — | –0.25 | — | –0.25 | — | ns |
| | | MachXO2-2000ZE | –0.27 | — | –0.27 | — | –0.27 | — | ns |
| | | MachXO2-4000ZE | –0.31 | — | –0.31 | — | –0.31 | — | ns |
| | | MachXO2-7000ZE | –0.33 | — | –0.33 | — | –0.33 | — | ns |
| $t_{H}$ | Clock to Data Hold – PIO Input Register | MachXO2-256ZE | 3.96 | — | 4.25 | — | 4.65 | — | ns |
| | | MachXO2-640ZE | 4.01 | — | 4.31 | — | 4.71 | — | ns |
| | | MachXO2-1200ZE | 3.95 | — | 4.29 | — | 4.73 | — | ns |
| | | MachXO2-2000ZE | 3.94 | — | 4.29 | — | 4.74 | — | ns |
| | | MachXO2-4000ZE | 3.96 | — | 4.36 | — | 4.87 | — | ns |
| | | MachXO2-7000ZE | 3.93 | — | 4.37 | — | 4.91 | — | ns |

| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **LPDDR**[9, 12] | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only.[13] | — | 0.349 | — | 0.381 | — | 0.396 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.665 | — | 0.630 | — | 0.613 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM LPDDR Serial Data Speed | | — | 120 | — | 110 | — | 96 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 60 | — | 55 | — | 48 | MHz |
| $f_{LPDDR}$ | LPDDR Data Transfer Rate | | 0 | 120 | 0 | 110 | 0 | 96 | Mbps |
| **DDR**[9, 12] | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only.[13] | — | 0.347 | — | 0.374 | — | 0.393 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.665 | — | 0.637 | — | 0.616 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM DDR Serial Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 58 | — | 49 | MHz |
| $f_{MEM\_DDR}$ | MEM DDR Data Transfer Rate | | N/A | 140 | N/A | 116 | N/A | 98 | Mbps |
| **DDR2**[9, 12] | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only.[13] | — | 0.372 | — | 0.394 | — | 0.410 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.690 | — | 0.658 | — | 0.618 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM DDR Serial Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 58 | — | 49 | MHz |
| $f_{MEM\_DDR2}$ | MEM DDR2 Data Transfer Rate | | N/A | 140 | N/A | 116 | N/A | 98 | Mbps |

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
7. The $t_{SU\_DEL}$ and $t_{H\_DEL}$ values use the SCLK_ZERHOLD default step size. Each step is 167 ps (–3), 182 ps (–2), 195 ps (–1).
8. This number for general purpose usage. Duty cycle tolerance is +/–10%.
9. Duty cycle is +/– 5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

## sysCLOCK PLL Timing

**Over Recommended Operating Conditions**

| Parameter | Descriptions | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $f_{IN}$ | Input Clock Frequency (CLKI, CLKFB) | | 7 | 400 | MHz |
| $f_{OUT}$ | Output Clock Frequency (CLKOP, CLKOS, CLKOS2) | | 1.5625 | 400 | MHz |
| $f_{OUT2}$ | Output Frequency (CLKOS3 cascaded from CLKOS2) | | 0.0122 | 400 | MHz |
| $f_{VCO}$ | PLL VCO Frequency | | 200 | 800 | MHz |
| $f_{PFD}$ | Phase Detector Input Frequency | | 7 | 400 | MHz |
| **AC Characteristics** | | | | | |
| $t_{DT}$ | Output Clock Duty Cycle | Without duty trim selected[3] | 45 | 55 | % |
| $t_{DT\_TRIM}$[7] | Edge Duty Trim Accuracy | | –75 | 75 | % |
| $t_{PH}$[4] | Output Phase Accuracy | | –6 | 6 | % |
| $t_{OPJIT}$[1, 8] | Output Clock Period Jitter | $f_{OUT}$ > 100 MHz | — | 150 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.007 | UIPP |
| | Output Clock Cycle-to-cycle Jitter | $f_{OUT}$ > 100 MHz | — | 180 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.009 | UIPP |
| | Output Clock Phase Jitter | $f_{PFD}$ > 100 MHz | — | 160 | ps p-p |
| | | $f_{PFD}$ < 100 MHz | — | 0.011 | UIPP |
| | Output Clock Period Jitter (Fractional-N) | $f_{OUT}$ > 100 MHz | — | 230 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.12 | UIPP |
| | Output Clock Cycle-to-cycle Jitter (Fractional-N) | $f_{OUT}$ > 100 MHz | — | 230 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.12 | UIPP |
| $t_{SPO}$ | Static Phase Offset | Divider ratio = integer | –120 | 120 | ps |
| $t_W$ | Output Clock Pulse Width | At 90% or 10%[3] | 0.9 | — | ns |
| $t_{LOCK}$[2, 5] | PLL Lock-in Time | | — | 15 | ms |
| $t_{UNLOCK}$ | PLL Unlock Time | | — | 50 | ns |
| $t_{IPJIT}$[6] | Input Clock Period Jitter | $f_{PFD} \geq 20$ MHz | — | 1,000 | ps p-p |
| | | $f_{PFD}$ < 20 MHz | — | 0.02 | UIPP |
| $t_{HI}$ | Input Clock High Time | 90% to 90% | 0.5 | — | ns |
| $t_{LO}$ | Input Clock Low Time | 10% to 10% | 0.5 | — | ns |
| $t_{STABLE}$[5] | STANDBY High to PLL Stable | | — | 15 | ms |
| $t_{RST}$ | RST/RESETM Pulse Width | | 1 | — | ns |
| $t_{RSTREC}$ | RST Recovery Time | | 1 | — | ns |
| $t_{RST\_DIV}$ | RESETC/D Pulse Width | | 10 | — | ns |
| $t_{RSTREC\_DIV}$ | RESETC/D Recovery Time | | 1 | — | ns |
| $t_{ROTATE-SETUP}$ | PHASESTEP Setup Time | | 10 | — | ns |

## I²C Port Timing Specifications[1, 2]

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $f_{MAX}$ | Maximum SCL clock frequency | — | 400 | kHz |

1. MachXO2 supports the following modes:
   • Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
   • Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
2. Refer to the I²C specification for timing requirements.

## SPI Port Timing Specifications[1]

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $f_{MAX}$ | Maximum SCK clock frequency | — | 45 | MHz |

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

## Switching Test Conditions

Figure 3-13 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-5.

***Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards***

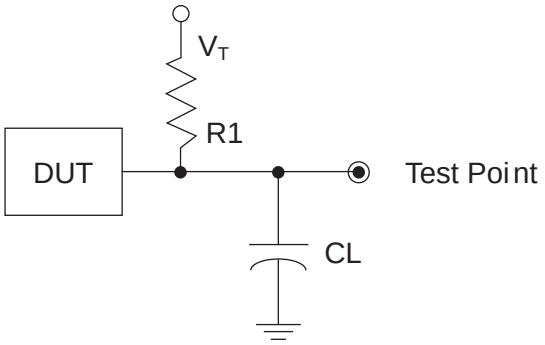



***Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces***

| Test Condition | R1 | CL | Timing Ref. | VT |
|---|---|---|---|---|
| LVTTL and LVCMOS settings (L -> H, H -> L) | ∞ | 0pF | LVTTL, LVCMOS 3.3 = 1.5 V | — |
| | | | LVCMOS 2.5 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.8 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.5 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.2 = $V_{CCIO}/2$ | — |
| LVTTL and LVCMOS 3.3 (Z -> H) | 188 | 0pF | 1.5 V | $V_{OL}$ |
| LVTTL and LVCMOS 3.3 (Z -> L) | | | 1.5 V | $V_{OH}$ |
| Other LVCMOS (Z -> H) | | | $V_{CCIO}/2$ | $V_{OL}$ |
| Other LVCMOS (Z -> L) | | | $V_{CCIO}/2$ | $V_{OH}$ |
| LVTTL + LVCMOS (H -> Z) | | | $V_{OH}$ – 0.15 V | $V_{OL}$ |
| LVTTL + LVCMOS (L -> Z) | | | $V_{OL}$ – 0.15 V | $V_{OH}$ |

*Note: Output test conditions for all other interfaces are determined by the respective standards.*

## Pinout Information Summary

| | MachXO2-256 | | | | | MachXO2-640 | | | MachXO2-640U |
|---|---|---|---|---|---|---|---|---|---|
| | 32 QFN[1] | 48 QFN[3] | 64 ucBGA | 100 TQFP | 132 csBGA | 48 QFN[3] | 100 TQFP | 132 csBGA | 144 TQFP |
| **General Purpose I/O per Bank** | | | | | | | | | |
| Bank 0 | 8 | 10 | 9 | 13 | 13 | 10 | 18 | 19 | 27 |
| Bank 1 | 2 | 10 | 12 | 14 | 14 | 10 | 20 | 20 | 26 |
| Bank 2 | 9 | 10 | 11 | 14 | 14 | 10 | 20 | 20 | 28 |
| Bank 3 | 2 | 10 | 12 | 14 | 14 | 10 | 20 | 20 | 26 |
| Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total General Purpose Single Ended I/O | 21 | 40 | 44 | 55 | 55 | 40 | 78 | 79 | 107 |
| | | | | | | | | | |
| **Differential I/O per Bank** | | | | | | | | | |
| Bank 0 | 4 | 5 | 5 | 7 | 7 | 5 | 9 | 10 | 14 |
| Bank 1 | 1 | 5 | 6 | 7 | 7 | 5 | 10 | 10 | 13 |
| Bank 2 | 4 | 5 | 5 | 7 | 7 | 5 | 10 | 10 | 14 |
| Bank 3 | 1 | 5 | 6 | 7 | 7 | 5 | 10 | 10 | 13 |
| Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total General Purpose Differential I/O | 10 | 20 | 22 | 28 | 28 | 20 | 39 | 40 | 54 |
| | | | | | | | | | |
| **Dual Function I/O** | 22 | 25 | 27 | 29 | 29 | 25 | 29 | 29 | 33 |
| **High-speed Differential I/O** | | | | | | | | | |
| Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 7 |
| **Gearboxes** | | | | | | | | | |
| Number of 7:1 or 8:1 Output Gearbox Available (Bank 0) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 7 |
| Number of 7:1 or 8:1 Input Gearbox Available (Bank 2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 7 |
| **DQS Groups** | | | | | | | | | |
| Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 |
| | | | | | | | | | |
| **VCCIO Pins** | | | | | | | | | |
| Bank 0 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 3 |
| Bank 1 | 1 | 1 | 2 | 2 | 2 | 1 | 2 | 2 | 3 |
| Bank 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 3 |
| Bank 3 | 1 | 1 | 2 | 2 | 2 | 1 | 2 | 2 | 3 |
| Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | | |
| VCC | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 4 |
| GND[2] | 2 | 1 | 8 | 8 | 8 | 1 | 8 | 10 | 12 |
| NC | 0 | 0 | 1 | 26 | 58 | 0 | 3 | 32 | 8 |
| Reserved for Configuration | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Total Count of Bonded Pins | 32 | 49 | 64 | 100 | 132 | 49 | 100 | 132 | 144 |

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.
2. For 48 QFN package, exposed die pad is the device ground.
3. 48-pin QFN information is 'Advanced'.

## Ordering Information

MachXO2 devices have top-side markings, for commercial and industrial grades, as shown below:



*Notes:*

*1. Markings are abbreviated for small packages.*

*2. See PCN 05A-12 for information regarding a change to the top-side mark logo.*

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000ZE-1TG144C | 6864 | 1.2 V | –1 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000ZE-2TG144C | 6864 | 1.2 V | –2 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000ZE-3TG144C | 6864 | 1.2 V | –3 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000ZE-1BG256C | 6864 | 1.2 V | –1 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000ZE-2BG256C | 6864 | 1.2 V | –2 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000ZE-3BG256C | 6864 | 1.2 V | –3 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000ZE-1FTG256C | 6864 | 1.2 V | –1 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000ZE-2FTG256C | 6864 | 1.2 V | –2 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000ZE-3FTG256C | 6864 | 1.2 V | –3 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000ZE-1BG332C | 6864 | 1.2 V | –1 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000ZE-2BG332C | 6864 | 1.2 V | –2 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000ZE-3BG332C | 6864 | 1.2 V | –3 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000ZE-1FG484C | 6864 | 1.2 V | –1 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000ZE-2FG484C | 6864 | 1.2 V | –2 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000ZE-3FG484C | 6864 | 1.2 V | –3 | Halogen-Free fpBGA | 484 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-1200ZE-1TG100CR1[1] | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200ZE-2TG100CR1[1] | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200ZE-3TG100CR1[1] | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200ZE-1MG132CR1[1] | 1280 | 1.2 V | –1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-2MG132CR1[1] | 1280 | 1.2 V | –2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-3MG132CR1[1] | 1280 | 1.2 V | –3 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-1TG144CR1[1] | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200ZE-2TG144CR1[1] | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200ZE-3TG144CR1[1] | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 144 | COM |

1. Specifications for the “LCMXO2-1200ZE-speed package CR1” are the same as the “LCMXO2-1200ZE-speed package C” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-1200HC-4SG32C | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200HC-5SG32C | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200HC-6SG32C | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200HC-4TG100C | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200HC-5TG100C | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200HC-6TG100C | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200HC-4MG132C | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200HC-5MG132C | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200HC-6MG132C | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200HC-4TG144C | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200HC-5TG144C | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200HC-6TG144C | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-1200UHC-4FTG256C | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-1200UHC-5FTG256C | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-1200UHC-6FTG256C | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000HC-4TG100C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000HC-5TG100C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000HC-6TG100C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000HC-4MG132C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000HC-5MG132C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000HC-6MG132C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000HC-4TG144C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000HC-5TG144C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000HC-6TG144C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000HC-4BG256C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000HC-5BG256C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000HC-6BG256C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000HC-4FTG256C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000HC-5FTG256C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000HC-6FTG256C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000UHC-4FG484C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-2000UHC-5FG484C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-2000UHC-6FG484C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000HC-4QN84C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000HC-5QN84C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000HC-6QN84C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000HC-4MG132C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HC-5MG132C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HC-6MG132C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HC-4TG144C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HC-5TG144C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HC-6TG144C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HC-4BG256C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HC-5BG256C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HC-6BG256C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HC-4FTG256C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HC-5FTG256C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HC-6FTG256C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HC-4BG332C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HC-5BG332C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HC-6BG332C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HC-4FG484C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HC-5FG484C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HC-6FG484C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | COM |

## Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-256ZE-1SG32I | 256 | 1.2 V | –1 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256ZE-2SG32I | 256 | 1.2 V | –2 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256ZE-3SG32I | 256 | 1.2 V | –3 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256ZE-1UMG64I | 256 | 1.2 V | –1 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256ZE-2UMG64I | 256 | 1.2 V | –2 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256ZE-3UMG64I | 256 | 1.2 V | –3 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256ZE-1TG100I | 256 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256ZE-2TG100I | 256 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256ZE-3TG100I | 256 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256ZE-1MG132I | 256 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256ZE-2MG132I | 256 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256ZE-3MG132I | 256 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640ZE-1TG100I | 640 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640ZE-2TG100I | 640 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640ZE-3TG100I | 640 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640ZE-1MG132I | 640 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640ZE-2MG132I | 640 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640ZE-3MG132I | 640 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-1200ZE-1UWG25ITR[1] | 1280 | 1.2 V | –1 | Halogen-Free WLCSP | 25 | IND |
| LCMXO2-1200ZE-1UWG25ITR50[3] | 1280 | 1.2 V | –1 | Halogen-Free WLCSP | 25 | IND |
| LCMXO2-1200ZE-1UWG25ITR1K[2] | 1280 | 1.2 V | –1 | Halogen-Free WLCSP | 25 | IND |
| LCMXO2-1200ZE-1SG32I | 1280 | 1.2 V | –1 | Halogen-Free QFN | 32 | IND |
| LCMXO2-1200ZE-2SG32I | 1280 | 1.2 V | –2 | Halogen-Free QFN | 32 | IND |
| LCMXO2-1200ZE-3SG32I | 1280 | 1.2 V | –3 | Halogen-Free QFN | 32 | IND |
| LCMXO2-1200ZE-1TG100I | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-2TG100I | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-3TG100I | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-1MG132I | 1280 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-2MG132I | 1280 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-3MG132I | 1280 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-1TG144I | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200ZE-2TG144I | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200ZE-3TG144I | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 144 | IND |

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

## High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-256HC-4SG32I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256HC-5SG32I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256HC-6SG32I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256HC-4SG48I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 48 | IND |
| LCMXO2-256HC-5SG48I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 48 | IND |
| LCMXO2-256HC-6SG48I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 48 | IND |
| LCMXO2-256HC-4UMG64I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256HC-5UMG64I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256HC-6UMG64I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256HC-4TG100I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256HC-5TG100I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256HC-6TG100I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256HC-4MG132I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256HC-5MG132I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256HC-6MG132I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640HC-4SG48I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 48 | IND |
| LCMXO2-640HC-5SG48I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 48 | IND |
| LCMXO2-640HC-6SG48I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 48 | IND |
| LCMXO2-640HC-4TG100I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640HC-5TG100I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640HC-6TG100I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640HC-4MG132I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640HC-5MG132I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640HC-6MG132I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640UHC-4TG144I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-640UHC-5TG144I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-640UHC-6TG144I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| January 2013 | 02.0 | Introduction | Updated the total number IOs to include JTAGENB. |
| | | Architecture | Supported Output Standards table – Added 3.3 $V_{CCIO}$ (Typ.) to LVDS row. |
| | | | Changed SRAM CRC Error Detection to Soft Error Detection. |
| | | DC and Switching Characteristics | Power Supply Ramp Rates table – Updated Units column for $t_{RAMP}$ symbol. |
| | | | Added new Maximum sysIO Buffer Performance table. |
| | | | sysCLOCK PLL Timing table – Updated Min. column values for $f_{IN}$, $f_{OUT}$, $f_{OUT2}$ and $f_{PFD}$ parameters. Added $t_{SPO}$ parameter. Updated footnote 6. |
| | | | MachXO2 Oscillator Output Frequency table – Updated symbol name for $t_{STABLEOSC.}$ |
| | | | DC Electrical Characteristics table – Updated conditions for $I_{IL,}$ $I_{IH}$ symbols. |
| | | | Corrected parameters tDQVBS and tDQVAS |
| | | | Corrected MachXO2 ZE parameters tDVADQ and tDVEDQ |
| | | Pinout Information | Included the MachXO2-4000HE 184 csBGA package. |
| | | Ordering Information | Updated part number. |
| April 2012 | 01.9 | Architecture | Removed references to TN1200. |
| | | Ordering Information | Updated the Device Status portion of the MachXO2 Part Number Description to include the 50 parts per reel for the WLCSP package. |
| | | | Added new part number and footnote 2 for LCMXO2-1200ZE-1UWG25ITR50. |
| | | | Updated footnote 1 for LCMXO2-1200ZE-1UWG25ITR. |
| | | Supplemental Information | Removed references to TN1200. |
| March 2012 | 01.8 | Introduction | Added 32 QFN packaging information to Features bullets and MachXO2 Family Selection Guide table. |
| | | DC and Switching Characteristics | Changed ‘STANDBY’ to ‘USERSTDBY’ in Standby Mode timing diagram. |
| | | Pinout Information | Removed footnote from Pin Information Summary tables. |
| | | | Added 32 QFN package to Pin Information Summary table. |
| | | Ordering Information | Updated Part Number Description and Ordering Information tables for 32 QFN package. |
| | | | Updated topside mark diagram in the Ordering Information section. |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| February 2012 | 01.7 | All | Updated document with new corporate logo. |
| | 01.6 | — | Data sheet status changed from preliminary to final. |
| | | Introduction | MachXO2 Family Selection Guide table – Removed references to 49-ball WLCSP. |
| | | DC and Switching Characteristics | Updated Flash Download Time table. |
| | | | Modified Storage Temperature in the Absolute Maximum Ratings section. |
| | | | Updated $I_{DK}$ max in Hot Socket Specifications table. |
| | | | Modified Static Supply Current tables for ZE and HC/HE devices. |
| | | | Updated Power Supply Ramp Rates table. |
| | | | Updated Programming and Erase Supply Current tables. |
| | | | Updated data in the External Switching Characteristics table. |
| | | | Corrected Absolute Maximum Ratings for Dedicated Input Voltage Applied for LCMXO2 HC. |
| | | | DC Electrical Characteristics table – Minor corrections to conditions for $I_{IL}$, $I_{IH}$. |
| | | Pinout Information | Removed references to 49-ball WLCSP. |
| | | | Signal Descriptions table – Updated description for GND, VCC, and VCCIOx. |
| | | | Updated Pin Information Summary table – Number of VCCIOs, GNDs, VCCs, and Total Count of Bonded Pins for MachXO2-256, 640, and 640U and Dual Function I/O for MachXO2-4000 332caBGA. |
| | | Ordering Information | Removed references to 49-ball WLCSP |
| August 2011 | 01.5 | DC and Switching Characteristics | Updated ESD information. |
| | | Ordering Information | Updated footnote for ordering WLCSP devices. |
| | 01.4 | Architecture | Updated information in Clock/Control Distribution Network and sysCLOCK Phase Locked Loops (PLLs). |
| | | DC and Switching Characteristics | Updated $I_{IL}$ and $I_{IH}$ conditions in the DC Electrical Characteristics table. |
| | | Pinout Information | Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables. |
| | | | Updated Pin Information Summary table: Dual Function I/O, DQS Groups Bank 1, Total General Purpose Single-Ended I/O, Differential I/O Per Bank, Total Count of Bonded Pins, Gearboxes.<br><br>Added column of data for MachXO2-2000 49 WLCSP. |
| | | Ordering Information | Updated R1 Device Specifications text section with information on migration from MachXO2-1200-R1 to Standard (non-R1) devices. |
| | | | Corrected Supply Voltage typo for part numbers: LCMX02-2000UHE-4FG484I, LCMX02-2000UHE-5FG484I, LCMX02-2000UHE-6FG484I. |
| | | | Added footnote for WLCSP package parts. |
| | | Supplemental Information | Removed reference to Stand-alone Power Calculator for MachXO2 Devices. Added reference to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices. |