E · Contraction - <u>LCMXO2-4000HE-6FTG256I Datasheet</u>



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	540
Number of Logic Elements/Cells	4320
Total RAM Bits	94208
Number of I/O	206
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-4000he-6ftg256i

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MachXO2 Family Data Sheet Introduction

May 2016

Features

- Flexible Logic Architecture
 - Six devices with 256 to 6864 LUT4s and 18 to 334 I/Os
- Ultra Low Power Devices
 - Advanced 65 nm low power process
 - As low as 22 μ W standby power
 - Programmable low swing differential I/Os
 - · Stand-by mode and other power saving options

Embedded and Distributed Memory

- Up to 240 kbits sysMEM™ Embedded Block RAM
- Up to 54 kbits Distributed RAM
- Dedicated FIFO control logic
- On-Chip User Flash Memory
 - Up to 256 kbits of User Flash Memory
 - 100,000 write cycles
 - Accessible through WISHBONE, SPI, I²C and JTAG interfaces
 - Can be used as soft processor PROM or as Flash memory

Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/Os
- Generic DDR, DDRX2, DDRX4
- Dedicated DDR/DDR2/LPDDR memory with DQS support

■ High Performance, Flexible I/O Buffer

- Programmable sysIO[™] buffer supports wide range of interfaces:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2
 - LVTTL
 - PCI
 - LVDS, Bus-LVDS, MLVDS, RSDS, LVPECL
 - SSTL 25/18
 - HSTL 18
 - Schmitt trigger inputs, up to 0.5 V hysteresis
- I/Os support hot socketing
- On-chip differential termination
- · Programmable pull-up or pull-down mode

- Flexible On-Chip Clocking
 - · Eight primary clocks
 - Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
 - Up to two analog PLLs per device with fractional-n frequency synthesis
 - Wide input frequency range (7 MHz to 400 MHz)

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- Non-volatile, Infinitely Reconfigurable
 - Instant-on powers up in microseconds
 - Single-chip, secure solution
 - Programmable through JTAG, SPI or I²C
 - Supports background programming of non-volatile memory
 - Optional dual boot with external SPI memory
- TransFR[™] Reconfiguration
 - In-field logic update while system operates

Enhanced System Level Support

- On-chip hardened functions: SPI, I²C, timer/ counter
- On-chip oscillator with 5.5% accuracy
- Unique TraceID for system tracking
- One Time Programmable (OTP) mode
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming
- Broad Range of Package Options
 - TQFP, WLCSP, ucBGA, csBGA, caBGA, ftBGA, fpBGA, QFN package options
 - Small footprint package options
 As small as 2.5 mm x 2.5 mm
 - · Density migration supported
 - · Advanced halogen-free packaging



Table 1-1. MachXO2™ Family Selection Guide

		XO2-256	XO2-640	XO2-640U ¹	XO2-1200	XO2-1200U ¹	XO2-2000	XO2-2000U1	XO2-4000	XO2-7000
LUTs		256	640	640	1280	1280	2112	2112	4320	6864
Distributed RAM (kt	oits)	2	5	5	10	10	16	16	34	54
EBR SRAM (kbits)		0	18	64	64	74	74	92	92	240
Number of EBR SR kbits/block)	AM Blocks (9	0	2	7	7	8	8	10	10	26
UFM (kbits)		0	24	64	64	80	80	96	96	256
Device Options:	HC ²	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	HE ³						Yes	Yes	Yes	Yes
	ZE ⁴	Yes	Yes		Yes		Yes		Yes	Yes
Number of PLLs		0	0	1	1	1	1	2	2	2
Hardened	I2C	2	2	2	2	2	2	2	2	2
Functions:	SPI	1	1	1	1	1	1	1	1	1
	Timer/Coun- ter	1	1	1	1	1	1	1	1	1
Packages	1					ю				
25-ball WLCSP⁵ (2.5 mm x 2.5 mm,	0.4 mm)				18					
32 QFN ⁶ (5 mm x 5 mm, 0.5	mm)	21			21					
48 QFN ^{8, 9} (7 mm x 7 mm, 0.5	mm)	40	40							
49-ball WLCSP ⁵ (3.2 mm x 3.2 mm,	0.4 mm)						38			
64-ball ucBGA (4 mm x 4 mm, 0.4	mm)	44								
84 QFN ⁷ (7 mm x 7 mm, 0.5	mm)								68	
100-pin TQFP (14 mm x 14 mm)		55	78		79		79			
132-ball csBGA (8 mm x 8 mm, 0.5	mm)	55	79		104		104		104	
144-pin TQFP (20 mm x 20 mm)				107	107		111		114	114
184-ball csBGA ⁷ (8 mm x 8 mm, 0.5	mm)								150	
256-ball caBGA (14 mm x 14 mm, 0	.8 mm)						206		206	206
256-ball ftBGA (17 mm x 17 mm, 1	.0 mm)					206	206		206	206
332-ball caBGA (17 mm x 17 mm, 0	.8 mm)								274	278
484-ball ftBGA (23 mm x 23 mm, 1	.0 mm)							278	278	334

1. Ultra high I/O device.

2. High performance with regulator – VCC = 2.5 V, 3.3 V

3. High performance without regulator $-V_{CC} = 1.2 V$ 4. Low power without regulator $-V_{CC} = 1.2 V$ 5. WLCSP package only available for ZE devices.

6. 32 QFN package only available for HC and ZE devices.

7. 184 csBGA package only available for HE devices.

8. 48-pin QFN information is 'Advanced'.

9. 48 QFN package only available for HC devices.



MachXO2 Family Data Sheet Architecture

March 2016

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Architecture Overview

The MachXO2 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have sysCLOCK[™] PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.





Note: MachXO2-256, and MachXO2-640/U are similar to MachXO2-1200. MachXO2-256 has a lower LUT count and no PLL or EBR blocks. MachXO2-640 has no PLL, a lower LUT count and two EBR blocks. MachXO2-640U has a lower LUT count, one PLL and seven EBR blocks.

Figure 2-2. Top View of the MachXO2-4000 Device



Note: MachXO2-1200U, MachXO2-2000/U and MachXO2-7000 are similar to MachXO2-4000. MachXO2-1200U and MachXO2-2000 have a lower LUT count, one PLL, and eight EBR blocks. MachXO2-2000U has a lower LUT count, two PLLs, and 10 EBR blocks. MachXO2-7000 has a higher LUT count, two PLLs, and 26 EBR blocks.

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The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag "hard" control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysl/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2-640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO2 devices provide commonly used hardened functions such as SPI controller, I²C controller and timer/ counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I²C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

PFU Blocks

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.



Table 2-4. PLL Signal Descriptions (Continued)

Port Name	I/O	Description
CLKOP	0	Primary PLL output clock (with phase shift adjustment)
CLKOS	0	Secondary PLL output clock (with phase shift adjust)
CLKOS2	0	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	0	Secondary PLL output clock3 (with phase shift adjust)
LOCK	0	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feed- back signals.
DPHSRC	0	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset - includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	0	PLL data bus data output
PLLACK	0	PLL data bus acknowledge signal

sysMEM Embedded Block RAM Memory

The MachXO2-640/U and larger devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.



Figure 2-8. sysMEM Memory Primitives



Table 2-6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE ¹	Output Clock Enable	Active High
RST	Reset	Active High
BE ¹	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	
DI	Data In	_
DO	Data Out	_
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	_
FF	FIFO RAM Full Flag	_
AEF	FIFO RAM Almost Empty Flag	_
EF	FIFO RAM Empty Flag	_
RPRST	FIFO RAM Read Pointer Reset	_

1. Optional signals.

2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.

3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.

4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).

5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.



Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO2 devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO2 devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

The MachXO2-640U, MachXO2-1200/U and higher density devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these higher density devices have on-chip differential termination and also provide PCI support.



MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 devices contain three types of sysIO buffer pairs.

1. Left and Right sysIO Buffer Pairs

The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential and referenced input buffers.

2. Bottom sysIO Buffer Pairs

The sysIO buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential and referenced input buffers. Only the I/Os on the bottom banks have programmable PCI clamps and differential input termination. The PCI clamp is enabled after V_{CC} and V_{CCIO} are at valid operating levels and the device has been configured.

3. Top sysIO Buffer Pairs

The sysIO buffer pairs in the top bank of the device consist of two single-ended output drivers and two singleended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential and referenced I/O buffers. Half of the sysIO buffer pairs on the top edge have true differential outputs. The sysIO buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver. The referenced input buffer can also be configured as a differential input buffer.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCIO0} have reached V_{PORUP} level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pulldown to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to V_{CCIO} as the default functionality). The I/O pins will maintain the blank configuration until V_{CC} and V_{CCIO} (for I/O banks containing configuration I/Os) have reached V_{PORUP} levels at which time the I/Os will take on the user-configured settings only after a proper download/configuration.

Supported Standards

The MachXO2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL, and PCI. The buffer supports the LVTTL, PCI, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO2-640U, MachXO2-1200/U and higher devices support on-chip LVDS output buffers on approximately 50% of the I/Os on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO2 devices. PCI support is provided in the bottom bank of theMachXO2-640U, MachXO2-1200/U and higher density devices. Table 2-11 summarizes the I/O characteristics of the MachXO2 PLDs.

Tables 2-11 and 2-12 show the I/O standards (together with their supply and reference voltages) supported by the MachXO2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1202, MachXO2 sysIO Usage Guide.



Hot Socketing

The MachXO2 devices have been carefully designed to ensure predictable behavior during power-up and powerdown. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO2 ideal for many multiple power supply and hot-swap applications.

On-chip Oscillator

Every MachXO2 device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

- 1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
- 2. During configuration, users select a different master clock frequency.
- 3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
- 4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-14 lists all the available MCLK frequencies.

Table 2-14. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

Embedded Hardened IP Functions and User Flash Memory

All MachXO2 devices provide embedded hardened functions such as SPI, I²C and Timer/Counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2-20.



Power-On-Reset Voltage Levels^{1, 2, 3, 4, 5}

Symbol	Parameter	Min.	Тур.	Max.	Units
V _{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and $V_{CCIO0})$	0.9	_	1.06	V
V _{PORUPEXT}	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	_	2.1	V
V _{PORDNBG}	Power-On-Reset ramp down trip point (band gap based circuit monitoring $V_{CCINT})$	0.75	_	0.93	V
V _{PORDNBGEXT}	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	_	1.33	V
V _{PORDNSRAM}	Power-On-Reset ramp down trip point (SRAM based circuit monitoring $V_{\mbox{CCINT}}$)	-	0.6	_	V
V _{PORDNSRAMEXT}	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	_	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.

3. Note that V_{PORUP} (min.) and V_{PORDNBG} (max.) are in different process corners. For any given process corner V_{PORDNBG} (max.) is always 12.0 mV below V_{PORUP} (min.).

4. V_{PORUPEXT} is for HC devices only. In these devices a separate POR circuit monitors the external V_{CC} power supply.

5. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

Programming/Erase Specifications

Symbol	Parameter	Min.	Max. ¹	Units	
	Flash Programming cycles per t _{RETENTION}	—	10,000	Cycles	
PROGCYC	Flash functional programming cycles	—	100,000	Oycles	
TRETENTION	Data retention at 100 °C junction temperature	10	—	Voars	
RETENTION	Data retention at 85 °C junction temperature	20	—	rears	

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

Hot Socketing Specifications^{1, 2, 3}

I_{DK} Input or I/O leakage Current $0 < V_{IN} < V_{IH}$ (MAX) +/-1000 μ A	Symbol	Parameter	Condition	Max.	Units
	I _{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/-1000	μΑ

1. Insensitive to sequence of V_{CC} and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO} .

2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).

3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

ESD Performance

Please refer to the MachXO2 Product Family Qualification Summary for complete qualification data, including ESD performance.



Typical Building Block Function Performance – HC/HE Devices¹

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	-6 Timing	Units
Basic Functions		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

Register-to-Register Performance

Function	-6 Timing	Units
Basic Functions		·
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
Embedded Memory Functions	·	·
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
Distributed Memory Functions	·	·
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

 The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.



I²C Port Timing Specifications^{1, 2}

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCL clock frequency	—	400	kHz

1. MachXO2 supports the following modes:

• Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)

• Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)

2. Refer to the I²C specification for timing requirements.

SPI Port Timing Specifications¹

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCK clock frequency		45	MHz

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

Switching Test Conditions

Figure 3-13 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-5.

Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards



Table 3-5. Test Fixture Required Components	, Non-Terminated Interfaces
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Test Condition	R1	CL	Timing Ref.	VT
			LVTTL, LVCMOS 3.3 = 1.5 V	_
			LVCMOS 2.5 = $V_{CCIO}/2$	_
LVTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVCMOS 1.8 = $V_{CCIO}/2$	
			LVCMOS 1.5 = $V_{CCIO}/2$	_
			LVCMOS 1.2 = $V_{CCIO}/2$	_
LVTTL and LVCMOS 3.3 (Z -> H)			1.5 V	V _{OL}
LVTTL and LVCMOS 3.3 (Z -> L)			1.5 V	V _{OH}
Other LVCMOS (Z -> H)	100	0nE	V _{CCIO} /2	V _{OL}
Other LVCMOS (Z -> L)	100	opr	V _{CCIO} /2	V _{OH}
LVTTL + LVCMOS (H -> Z)	1		V _{OH} – 0.15 V	V _{OL}
LVTTL + LVCMOS (L -> Z)			V _{OL} – 0.15 V	V _{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.



MachXO2 Family Data Sheet Pinout Information

March 2017

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Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
		[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).
		[Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.
		[A/B/C/D] indicates the PIO within the group to which the pad is connected.
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic.
		During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.
NC	—	No connect.
GND	_	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together. For QFN 48 package, the exposed die pad is the device ground.
VCC	_	V_{CC} – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIOx	_	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.
PLL and Clock Functi	ons (Us	ed as user-programmable I/O pins when not used for PLL or clock pins)
[LOC]_GPLL[T, C]_IN	_	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]		Primary Clock pads. One to three clock pads per side.
Test and Programming	g (Dual t	function pins used for test access port and during sysCONFIG™)
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
ТСК	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	0	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
		Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then:
JTAGENB	I	If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O.
		If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.
		For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.
Configuration (Dual fu	nction p	ins used during sysCONFIG)
PROGRAMN	I	Initiates configuration sequence when asserted low. During configuration, or when reserved as PROGRAMN in user mode, this pin always has an active pull-up.

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		M	achXO2-120	0		MachXO2-1200U
	100 TQFP	132 csBGA	144 TQFP	25 WLCSP	32 QFN ¹	256 ftBGA
General Purpose I/O per Bank						
Bank 0	18	25	27	11	9	50
Bank 1	21	26	26	0	2	52
Bank 2	20	28	28	7	9	52
Bank 3	20	25	26	0	2	16
Bank 4	0	0	0	0	0	16
Bank 5	0	0	0	0	0	20
Total General Purpose Single Ended I/O	79	104	107	18	22	206
Differential I/O per Bank						
Bank 0	9	13	14	5	4	25
Bank 1	10	13	13	0	1	26
Bank 2	10	14	14	2	4	26
Bank 3	10	12	13	0	1	8
Bank 4	0	0	0	0	0	8
Bank 5	0	0	0	0	0	10
Total General Purpose Differential I/O	39	52	54	7	10	103
Dual Function I/O	31	33	33	18	22	33
High-speed Differential I/O						1
Bank 0	4	7	7	0	0	14
Gearboxes						1
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	4	7	7	0	0	14
Number of 7:1 or 8:1 Input Gearbox Avail- able (Bank 2)	5	7	7	0	2	14
DQS Groups						
Bank 1	1	2	2	0	0	2
VCCIO Pins	1	1				1
Bank 0	2	3	3	1	2	4
Bank 1	2	3	3	0	1	4
Bank 2	2	3	3	1	2	4
Bank 3	3	3	3	0	1	1
Bank 4	0	0	0	0	0	2
Bank 5	0	0	0	0	0	1
	I			Гг		Γ
VCC	2	4	4	2	2	8
GND	8	10	12	2	2	24
NC	1	1	8	0	0	1
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	100	132	144	25	32	256

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.



Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32C	256	1.2 V	-1	Halogen-Free QFN	32	COM
LCMXO2-256ZE-2SG32C	256	1.2 V	-2	Halogen-Free QFN	32	COM
LCMXO2-256ZE-3SG32C	256	1.2 V	-3	Halogen-Free QFN	32	COM
LCMXO2-256ZE-1UMG64C	256	1.2 V	-1	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-2UMG64C	256	1.2 V	-2	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-3UMG64C	256	1.2 V	-3	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-1TG100C	256	1.2 V	-1	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-2TG100C	256	1.2 V	-2	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-3TG100C	256	1.2 V	-3	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-1MG132C	256	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-2MG132C	256	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-3MG132C	256	1.2 V	-3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100C	640	1.2 V	-1	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-2TG100C	640	1.2 V	-2	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-3TG100C	640	1.2 V	-3	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-1MG132C	640	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-2MG132C	640	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-3MG132C	640	1.2 V	-3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1SG32C	1280	1.2 V	-1	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-2SG32C	1280	1.2 V	-2	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-3SG32C	1280	1.2 V	-3	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-1TG100C	1280	1.2 V	-1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100C	1280	1.2 V	-2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100C	1280	1.2 V	-3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132C	1280	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132C	1280	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132C	1280	1.2 V	-3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144C	1280	1.2 V	-1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144C	1280	1.2 V	-2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144C	1280	1.2 V	-3	Halogen-Free TQFP	144	COM



High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32C	256	2.5 V / 3.3 V	-4	Halogen-Free QFN	32	COM
LCMXO2-256HC-5SG32C	256	2.5 V / 3.3 V	-5	Halogen-Free QFN	32	COM
LCMXO2-256HC-6SG32C	256	2.5 V / 3.3 V	-6	Halogen-Free QFN	32	COM
LCMXO2-256HC-4SG48C	256	2.5 V / 3.3 V	-4	Halogen-Free QFN	48	COM
LCMXO2-256HC-5SG48C	256	2.5 V / 3.3 V	-5	Halogen-Free QFN	48	COM
LCMXO2-256HC-6SG48C	256	2.5 V / 3.3 V	-6	Halogen-Free QFN	48	COM
LCMXO2-256HC-4UMG64C	256	2.5 V / 3.3 V	-4	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-5UMG64C	256	2.5 V / 3.3 V	-5	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-6UMG64C	256	2.5 V / 3.3 V	-6	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-4TG100C	256	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-256HC-5TG100C	256	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-256HC-6TG100C	256	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-256HC-4MG132C	256	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-256HC-5MG132C	256	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-256HC-6MG132C	256	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48C	640	2.5 V / 3.3 V	-4	Halogen-Free QFN	48	COM
LCMXO2-640HC-5SG48C	640	2.5 V / 3.3 V	-5	Halogen-Free QFN	48	COM
LCMXO2-640HC-6SG48C	640	2.5 V / 3.3 V	-6	Halogen-Free QFN	48	COM
LCMXO2-640HC-4TG100C	640	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-640HC-5TG100C	640	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-640HC-6TG100C	640	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-640HC-4MG132C	640	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-640HC-5MG132C	640	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-640HC-6MG132C	640	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144C	640	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-5TG144C	640	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-6TG144C	640	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	COM



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484C	2112	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-5FG484C	2112	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-6FG484C	2112	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84C	4320	2.5 V / 3.3 V	-4	Halogen-Free QFN	84	COM
LCMXO2-4000HC-5QN84C	4320	2.5 V / 3.3 V	-5	Halogen-Free QFN	84	COM
LCMXO2-4000HC-6QN84C	4320	2.5 V / 3.3 V	-6	Halogen-Free QFN	84	COM
LCMXO2-4000HC-4MG132C	4320	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-5MG132C	4320	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-6MG132C	4320	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-4TG144C	4320	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-5TG144C	4320	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-6TG144C	4320	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-4BG256C	4320	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-5BG256C	4320	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-6BG256C	4320	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-4FTG256C	4320	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-5FTG256C	4320	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-6FTG256C	4320	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-4BG332C	4320	2.5 V / 3.3 V	-4	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-5BG332C	4320	2.5 V / 3.3 V	-5	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-6BG332C	4320	2.5 V / 3.3 V	-6	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-4FG484C	4320	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-5FG484C	4320	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-6FG484C	4320	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	COM



High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100C	2112	1.2 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-5TG100C	2112	1.2 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-6TG100C	2112	1.2 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-4TG144C	2112	1.2 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-5TG144C	2112	1.2 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-6TG144C	2112	1.2 V	-6	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-4MG132C	2112	1.2 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-5MG132C	2112	1.2 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-6MG132C	2112	1.2 V	-6	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-4BG256C	2112	1.2 V	-4	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-5BG256C	2112	1.2 V	-5	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-6BG256C	2112	1.2 V	-6	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-4FTG256C	2112	1.2 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-5FTG256C	2112	1.2 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-6FTG256C	2112	1.2 V	-6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484C	2112	1.2 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-5FG484C	2112	1.2 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-6FG484C	2112	1.2 V	-6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4TG144C	4320	1.2 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-5TG144C	4320	1.2 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-6TG144C	4320	1.2 V	-6	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-4MG132C	4320	1.2 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-5MG132C	4320	1.2 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-6MG132C	4320	1.2 V	-6	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-4BG256C	4320	1.2 V	-4	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4MG184C	4320	1.2 V	-4	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5MG184C	4320	1.2 V	-5	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-6MG184C	4320	1.2 V	-6	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5BG256C	4320	1.2 V	-5	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-6BG256C	4320	1.2 V	-6	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4FTG256C	4320	1.2 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-5FTG256C	4320	1.2 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-6FTG256C	4320	1.2 V	-6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-4BG332C	4320	1.2 V	-4	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-5BG332C	4320	1.2 V	-5	Halogen-Free caBGA	332	COM



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-6BG332C	4320	1.2 V	-6	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-4FG484C	4320	1.2 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-5FG484C	4320	1.2 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-6FG484C	4320	1.2 V	-6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144C	6864	1.2 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-5TG144C	6864	1.2 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-6TG144C	6864	1.2 V	-6	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-4BG256C	6864	1.2 V	-4	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-5BG256C	6864	1.2 V	-5	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-6BG256C	6864	1.2 V	-6	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-4FTG256C	6864	1.2 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-5FTG256C	6864	1.2 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-6FTG256C	6864	1.2 V	-6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-4BG332C	6864	1.2 V	-4	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-5BG332C	6864	1.2 V	-5	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-6BG332C	6864	1.2 V	-6	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-4FG484C	6864	1.2 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-5FG484C	6864	1.2 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-6FG484C	6864	1.2 V	-6	Halogen-Free fpBGA	484	COM



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4MG132I	4320	1.2 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-5MG132I	4320	1.2 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-6MG132I	4320	1.2 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-4TG144I	4320	1.2 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-5TG144I	4320	1.2 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-6TG144I	4320	1.2 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-4MG184I	4320	1.2 V	-4	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-5MG184I	4320	1.2 V	-5	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-6MG184I	4320	1.2 V	-6	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-4BG256I	4320	1.2 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-5BG256I	4320	1.2 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-6BG256I	4320	1.2 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-4FTG256I	4320	1.2 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-5FTG256I	4320	1.2 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-6FTG256I	4320	1.2 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-4BG332I	4320	1.2 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-5BG332I	4320	1.2 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-6BG332I	4320	1.2 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-4FG484I	4320	1.2 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-5FG484I	4320	1.2 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-6FG484I	4320	1.2 V	-6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144I	6864	1.2 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-5TG144I	6864	1.2 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-6TG144I	6864	1.2 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-4BG256I	6864	1.2 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-5BG256I	6864	1.2 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-6BG256I	6864	1.2 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-4FTG256I	6864	1.2 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-5FTG256I	6864	1.2 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-6FTG256I	6864	1.2 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-4BG332I	6864	1.2 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-5BG332I	6864	1.2 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-6BG332I	6864	1.2 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-4FG484I	6864	1.2 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-5FG484I	6864	1.2 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-6FG484I	6864	1.2 V	-6	Halogen-Free fpBGA	484	IND