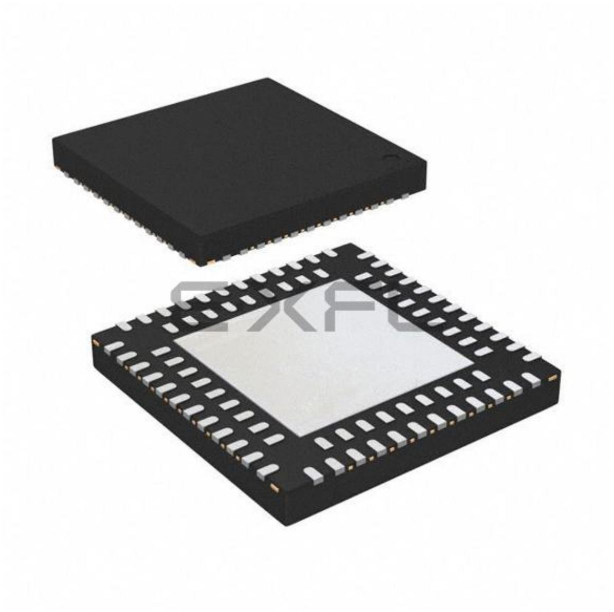
Lattice Semiconductor Corporation - LCMXO2-4000ZE-2QN84I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

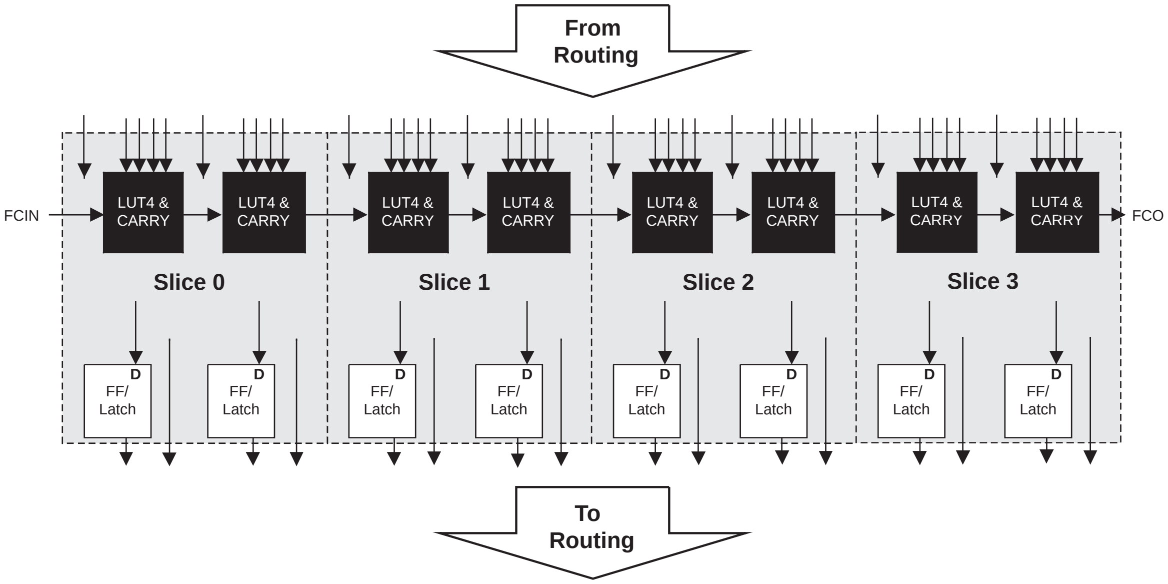
Details	
Product Status	Active
Number of LABs/CLBs	540
Number of Logic Elements/Cells	4320
Total RAM Bits	94208
Number of I/O	68
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	84-VFQFN Dual Rows, Exposed Pad
Supplier Device Package	84-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-4000ze-2qn84i

Table 1-1. MachXO2™ Family Selection Guide

		XO2-256	XO2-640	XO2-640U[1]	XO2-1200	XO2-1200U[1]	XO2-2000	XO2-2000U[1]	XO2-4000	XO2-7000
LUTs		256	640	640	1280	1280	2112	2112	4320	6864
Distributed RAM (kbits)		2	5	5	10	10	16	16	34	54
EBR SRAM (kbits)		0	18	64	64	74	74	92	92	240
Number of EBR SRAM Blocks (9 kbits/block)		0	2	7	7	8	8	10	10	26
UFM (kbits)		0	24	64	64	80	80	96	96	256
Device Options:	HC[2]	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	HE[3]						Yes	Yes	Yes	Yes
	ZE[4]	Yes	Yes		Yes		Yes		Yes	Yes
Number of PLLs		0	0	1	1	1	1	2	2	2
Hardened Functions:	I2C	2	2	2	2	2	2	2	2	2
	SPI	1	1	1	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1	1	1	1
Packages		**IO**								
25-ball WLCSP[5] (2.5 mm x 2.5 mm, 0.4 mm)					18					
32 QFN[6] (5 mm x 5 mm, 0.5 mm)		21			21					
48 QFN[8, 9] (7 mm x 7 mm, 0.5 mm)		40	40							
49-ball WLCSP[5] (3.2 mm x 3.2 mm, 0.4 mm)							38			
64-ball ucBGA (4 mm x 4 mm, 0.4 mm)		44								
84 QFN[7] (7 mm x 7 mm, 0.5 mm)									68	
100-pin TQFP (14 mm x 14 mm)		55	78		79		79			
132-ball csBGA (8 mm x 8 mm, 0.5 mm)		55	79		104		104		104	
144-pin TQFP (20 mm x 20 mm)				107	107		111		114	114
184-ball csBGA[7] (8 mm x 8 mm, 0.5 mm)									150	
256-ball caBGA (14 mm x 14 mm, 0.8 mm)							206		206	206
256-ball ftBGA (17 mm x 17 mm, 1.0 mm)						206	206		206	206
332-ball caBGA (17 mm x 17 mm, 0.8 mm)									274	278
484-ball ftBGA (23 mm x 23 mm, 1.0 mm)								278	278	334

1. Ultra high I/O device.
2. High performance with regulator – VCC = 2.5 V, 3.3 V
3. High performance without regulator – V_{CC} = 1.2 V
4. Low power without regulator – V_{CC} = 1.2 V
5. WLCSP package only available for ZE devices.
6. 32 QFN package only available for HC and ZE devices.
7. 184 csBGA package only available for HE devices.
8. 48-pin QFN information is ‘Advanced’.
9. 48 QFN package only available for HC devices.

Figure 2-3. PFU Block Diagram



Slices

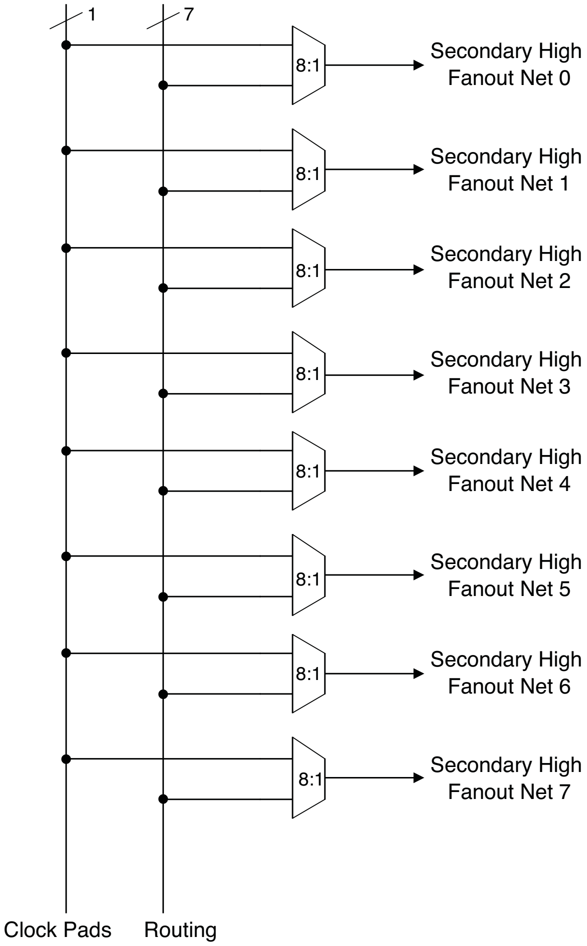
Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1. Resources and Modes Available per Slice

	PFU Block	
Slice	**Resources**	**Modes**
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.

Figure 2-6. Secondary High Fanout Nets for MachXO2 Devices



sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The MachXO2-640U, MachXO2-1200/U and larger devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

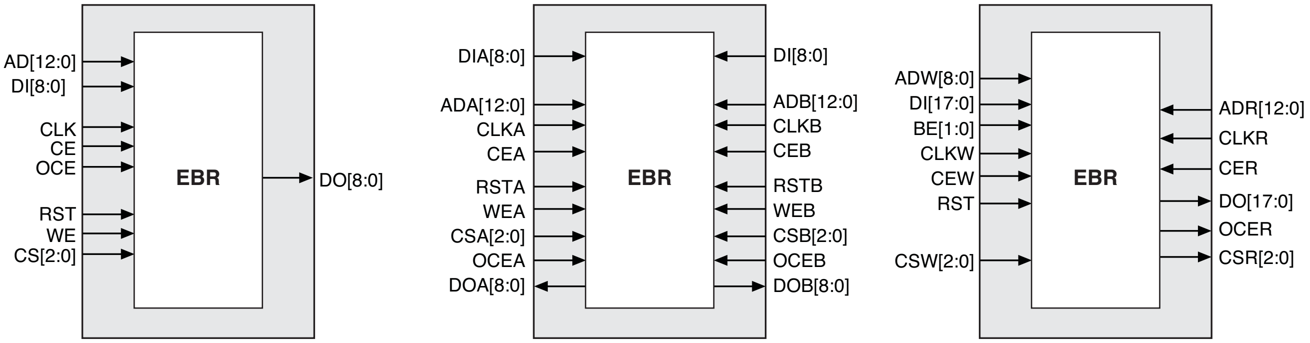
The MachXO2 sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO2 clock distribution network directly or general purpose routing resources can be used.

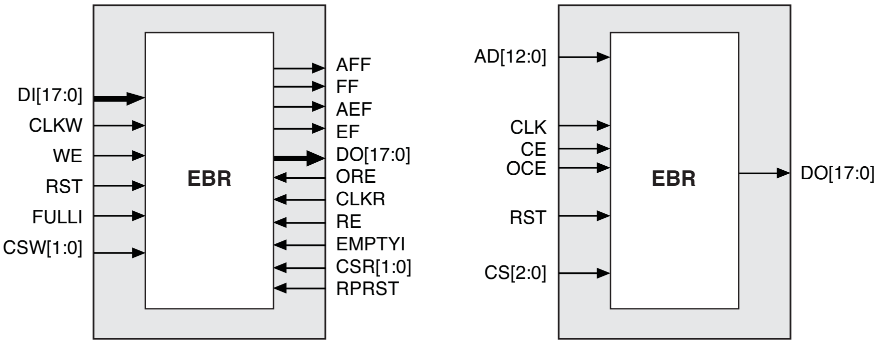
The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.

Figure 2-8. sysMEM Memory Primitives



Single-Port RAM **True Dual Port RAM** **Pseudo Dual Port RAM**



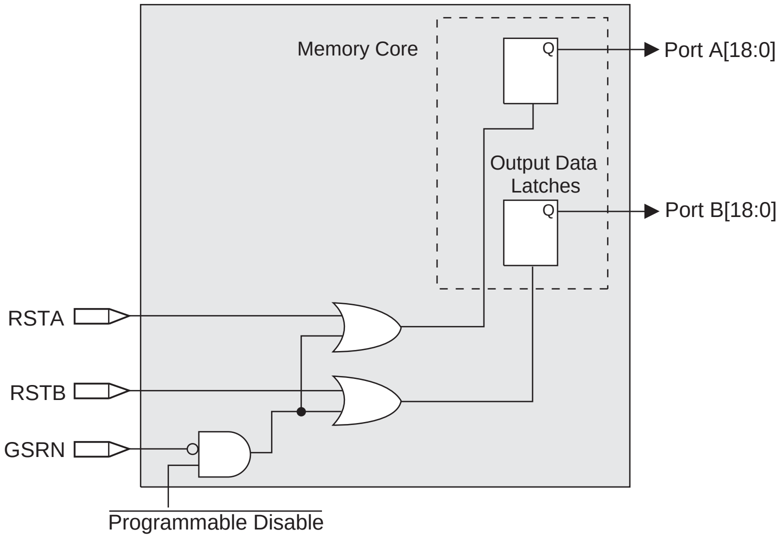
FIFO RAM **ROM**

Table 2-6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE[1]	Output Clock Enable	Active High
RST	Reset	Active High
BE[1]	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	—
DI	Data In	—
DO	Data Out	—
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	—
FF	FIFO RAM Full Flag	—
AEF	FIFO RAM Almost Empty Flag	—
EF	FIFO RAM Empty Flag	—
RPRST	FIFO RAM Read Pointer Reset	—

1. Optional signals.
2. For dual port EBR primitives a trailing ‘A’ or ‘B’ in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing ‘R’ or ‘W’ in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

Figure 2-9. Memory Core Reset

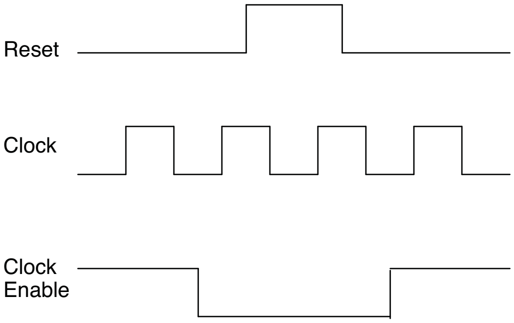


For further information on the sysMEM EBR block, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram



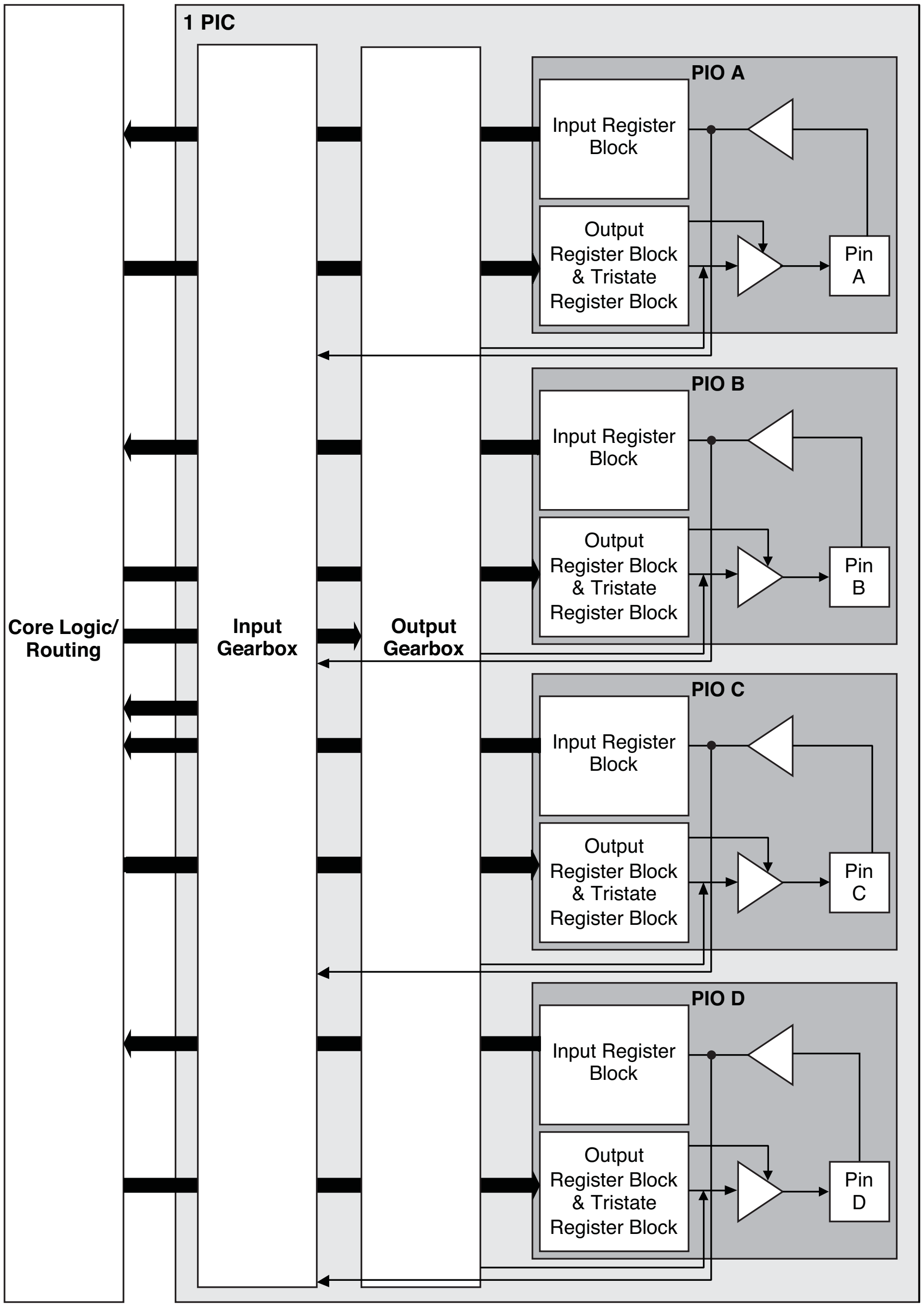
If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-10. The reset timing rules apply to the RPReset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For more details refer to TN1201, Memory Usage Guide for MachXO2 Devices.

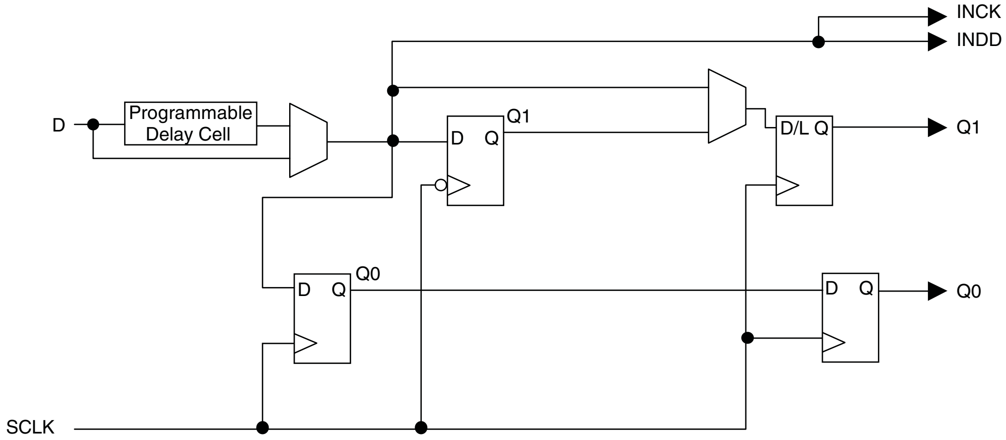
Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

Figure 2-11. Group of Four Programmable I/O Cells



Notes:
1. Input gearbox is available only in PIC on the bottom edge of MachXO2-640U, MachXO2-1200/U and larger devices.
2. Output gearbox is available only in PIC on the top edge of MachXO2-640U, MachXO2-1200/U and larger devices.

Figure 2-12. MachXO2 Input Register Block Diagram (PIO on Left, Top and Bottom Edges)



Right Edge

The input register block on the right edge is a superset of the same block on the top, bottom, and left edges. In addition to the modes described above, the input register block on the right edge also supports DDR memory mode.

In DDR memory mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (DQSR90) in the DDR Memory mode creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the DQS domain. The DQSR90 and DDRCLKPOL signals are generated in the DQS read-write block.

Figure 2-13. MachXO2 Input Register Block Diagram (PIO on Right Edge)

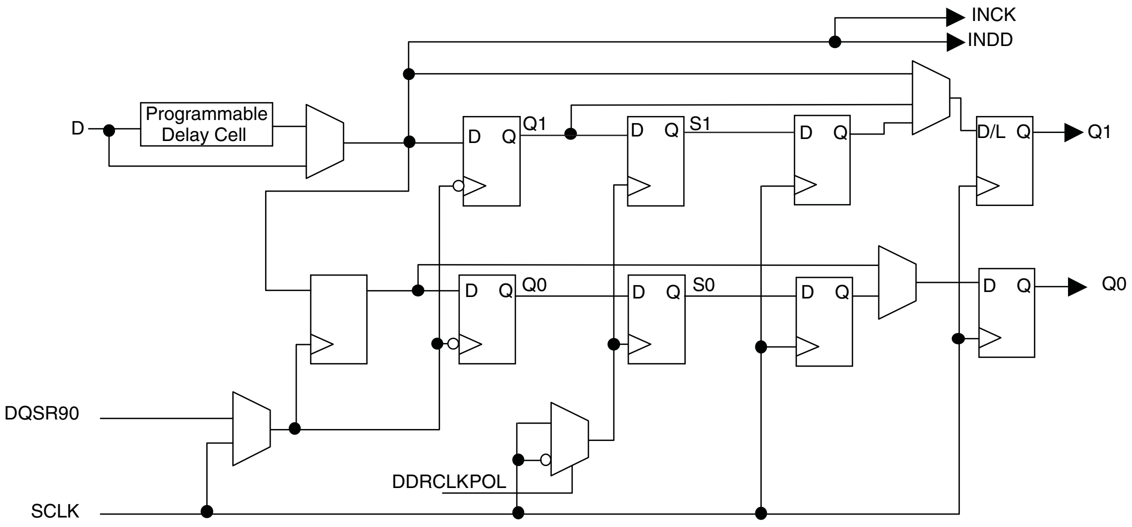


Table 2-13. Supported Output Standards

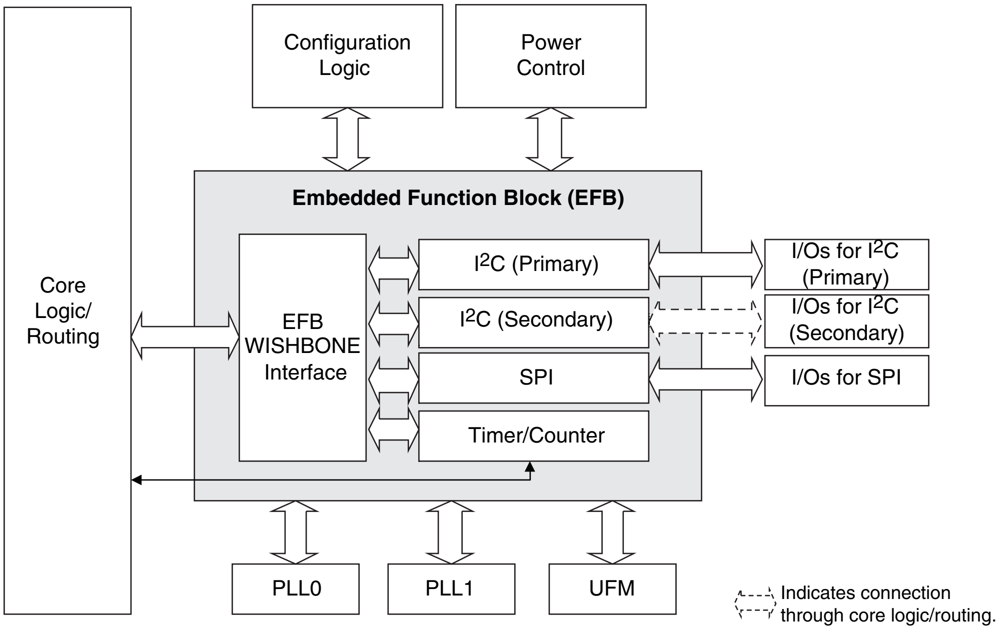
Output Standard	V_{CCIO} (Typ.)
Single-Ended Interfaces	
LVTTL	3.3
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8
LVCMOS15	1.5
LVCMOS12	1.2
LVCMOS33, Open Drain	—
LVCMOS25, Open Drain	—
LVCMOS18, Open Drain	—
LVCMOS15, Open Drain	—
LVCMOS12, Open Drain	—
PCI33	3.3
SSTL25 (Class I)	2.5
SSTL18 (Class I)	1.8
HSTL18(Class I)	1.8
Differential Interfaces	
LVDS[1, 2]	2.5, 3.3
BLVDS, MLVDS, RSDS [2]	2.5
LVPECL[2]	3.3
MIPI[2]	2.5
Differential SSTL18	1.8
Differential SSTL25	2.5
Differential HSTL18	1.8

1. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.

sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO2-1200U, MachXO2-2000/U and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO2-1200 and lower density devices have four banks (one bank per side). Figures 2-18 and 2-19 show the sysIO banks and their associated supplies for all devices.

Figure 2-20. Embedded Function Block Interface



Hardened I²C IP Core

Every MachXO2 device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I²C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface

For more details on these embedded functions, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

User Flash Memory (UFM)

MachXO2-640/U and higher density devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I^2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

Standby Mode and Power Saving Options

MachXO2 devices are available in three options for maximum flexibility: ZE, HC and HE devices. The ZE devices have ultra low static and dynamic power consumption. These devices use a 1.2 V core voltage that further reduces power consumption. The HC and HE devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the HE devices operate at 1.2 V V_{CC}.

MachXO2 devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO2 devices support an ultra low power Stand-by mode. While most of these features are available in all three device types, these features are mainly intended for use with MachXO2 ZE devices to manage power consumption.

In the stand-by mode the MachXO2 devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I^2C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO2 devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I^2C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

1. Internal Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I^2C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, MachXO2 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

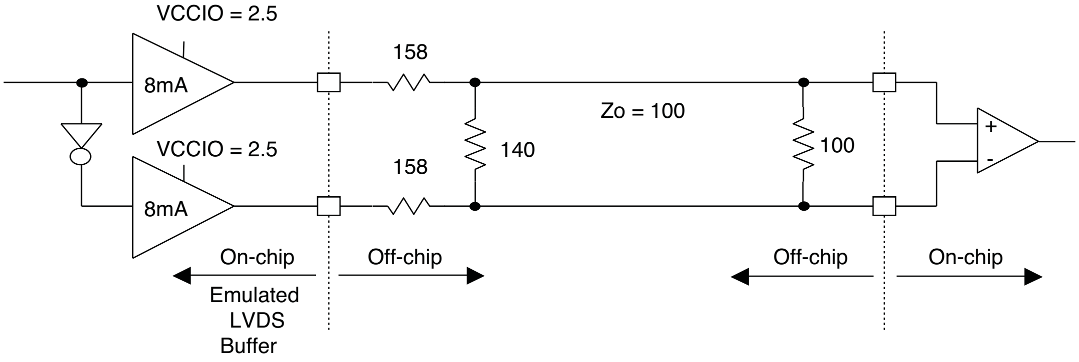
sysIO Single-Ended DC Electrical Characteristics[1, 2]

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max.[4] (mA)	I_{OH} Max.[4] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3 LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
							16	–16
							24	–24
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
							16	–16
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	0.35V_{CCIO}	0.65V_{CCIO}	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
							12	–12
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.5	–0.3	0.35V_{CCIO}	0.65V_{CCIO}	3.6	0.4	V_{CCIO} – 0.4	4	–4
							8	–8
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.2	–0.3	0.35V_{CCIO}	0.65V_{CCIO}	3.6	0.4	V_{CCIO} – 0.4	4	–2
							8	–6
					0.2	V_{CCIO} – 0.2	0.1	–0.1
PCI	–0.3	0.3V_{CCIO}	0.5V_{CCIO}	3.6	0.1V_{CCIO}	0.9V_{CCIO}	1.5	–0.5
SSTL25 Class I	–0.3	V_{REF} – 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	8	8
SSTL25 Class II	–0.3	V_{REF} – 0.18	V_{REF} + 0.18	3.6	NA	NA	NA	NA
SSTL18 Class I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	3.6	0.40	V_{CCIO} - 0.40	8	8
SSTL18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	3.6	NA	NA	NA	NA
HSTL18 Class I	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	V_{CCIO} - 0.40	8	8
HSTL18 Class II	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS25R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS12R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain

LVDS Emulation

MachXO2 devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

Figure 3-1. LVDS Using External Resistors (LVDS25E)



Note: All resistors are ±1%.

Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	158	Ohms
R_P	Driver parallel resistor	140	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	6.03	mA

Typical Building Block Function Performance – ZE Devices[1]

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–3 Timing	Units
Basic Functions		
16-bit decoder	13.9	ns
4:1 MUX	10.9	ns
16:1 MUX	12.0	ns

Register-to-Register Performance

Function	–3 Timing	Units
Basic Functions		
16:1 MUX	191	MHz
16-bit adder	134	MHz
16-bit counter	148	MHz
64-bit counter	77	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	90	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	214	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-256ZE	2.62	—	2.91	—	3.14	—	ns
		MachXO2-640ZE	2.56	—	2.85	—	3.08	—	ns
		MachXO2-1200ZE	2.30	—	2.57	—	2.79	—	ns
		MachXO2-2000ZE	2.25	—	2.50	—	2.70	—	ns
		MachXO2-4000ZE	2.39	—	2.60	—	2.76	—	ns
		MachXO2-7000ZE	2.17	—	2.33	—	2.43	—	ns
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-256ZE	–0.44	—	–0.44	—	–0.44	—	ns
		MachXO2-640ZE	–0.43	—	–0.43	—	–0.43	—	ns
		MachXO2-1200ZE	–0.28	—	–0.28	—	–0.28	—	ns
		MachXO2-2000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-4000ZE	–0.34	—	–0.34	—	–0.34	—	ns
		MachXO2-7000ZE	–0.21	—	–0.21	—	–0.21	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices	—	150	—	125	—	104	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
t_{COE}	Clock to Output – PIO Output Register	MachXO2-1200ZE	—	11.10	—	11.51	—	11.91	ns
		MachXO2-2000ZE	—	11.10	—	11.51	—	11.91	ns
		MachXO2-4000ZE	—	10.89	—	11.28	—	11.67	ns
		MachXO2-7000ZE	—	11.10	—	11.51	—	11.91	ns
t_{SUE}	Clock to Data Setup – PIO Input Register	MachXO2-1200ZE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-2000ZE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000ZE	–0.15	—	–0.15	—	–0.15	—	ns
		MachXO2-7000ZE	–0.23	—	–0.23	—	–0.23	—	ns
t_{HE}	Clock to Data Hold – PIO Input Register	MachXO2-1200ZE	3.81	—	4.11	—	4.52	—	ns
		MachXO2-2000ZE	3.81	—	4.11	—	4.52	—	ns
		MachXO2-4000ZE	3.60	—	3.89	—	4.28	—	ns
		MachXO2-7000ZE	3.81	—	4.11	—	4.52	—	ns
t_{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200ZE	2.78	—	3.11	—	3.40	—	ns
		MachXO2-2000ZE	2.78	—	3.11	—	3.40	—	ns
		MachXO2-4000ZE	3.11	—	3.48	—	3.79	—	ns
		MachXO2-7000ZE	2.94	—	3.30	—	3.60	—	ns
t_{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200ZE	–0.29	—	-0.29	—	–0.29	—	ns
		MachXO2-2000ZE	–0.29	—	-0.29	—	–0.29	—	ns
		MachXO2-4000ZE	–0.46	—	-0.46	—	–0.46	—	ns
		MachXO2-7000ZE	–0.37	—	-0.37	—	–0.37	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t_{COPLL}	Clock to Output – PIO Output Register	MachXO2-1200ZE	—	7.95	—	8.07	—	8.19	ns
		MachXO2-2000ZE	—	7.97	—	8.10	—	8.22	ns
		MachXO2-4000ZE	—	7.98	—	8.10	—	8.23	ns
		MachXO2-7000ZE	—	8.02	—	8.14	—	8.26	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO2-1200ZE	0.85	—	0.85	—	0.89	—	ns
		MachXO2-2000ZE	0.84	—	0.84	—	0.86	—	ns
		MachXO2-4000ZE	0.84	—	0.84	—	0.85	—	ns
		MachXO2-7000ZE	0.83	—	0.83	—	0.81	—	ns

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HPLL}	Clock to Data Hold – PIO Input Register	MachXO2-1200ZE	0.66	—	0.68	—	0.80	—	ns
		MachXO2-2000ZE	0.68	—	0.70	—	0.83	—	ns
		MachXO2-4000ZE	0.68	—	0.71	—	0.84	—	ns
		MachXO2-7000ZE	0.73	—	0.74	—	0.87	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200ZE	5.14	—	5.69	—	6.20	—	ns
		MachXO2-2000ZE	5.11	—	5.67	—	6.17	—	ns
		MachXO2-4000ZE	5.27	—	5.84	—	6.35	—	ns
		MachXO2-7000ZE	5.15	—	5.71	—	6.23	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200ZE	–1.36	—	–1.36	—	–1.36	—	ns
		MachXO2-2000ZE	–1.35	—	–1.35	—	–1.35	—	ns
		MachXO2-4000ZE	–1.43	—	–1.43	—	–1.43	—	ns
		MachXO2-7000ZE	–1.41	—	–1.41	—	–1.41	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.382	—	0.401	—	0.417	UI
t_{DVE}	Input Data Hold After CLK		0.670	—	0.684	—	0.693	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	All MachXO2 devices, all sides	1.319	—	1.412	—	1.462	—	ns
t_{HO}	Input Data Hold After CLK		0.717	—	1.010	—	1.340	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.361	—	0.346	—	0.334	UI
t_{DVE}	Input Data Hold After CLK		0.602	—	0.625	—	0.648	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.472	—	0.672	—	0.865	—	ns
t_{HO}	Input Data Hold After CLK		0.363	—	0.501	—	0.743	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input - GDDRX4_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.307	—	0.316	—	0.326	UI
t_{DVE}	Input Data Hold After ECLK		0.662	—	0.650	—	0.649	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz

MachXO2 Family Data Sheet
Ordering Information

March 2017 **Data Sheet DS1035**

MachXO2 Part Number Description

LCMXO2 – XXXX X X X – X XXXXXX X XX XX

Device Family
MachXO2 PLD

Logic Capacity
256 = 256 LUTs
640 = 640 LUTs
1200 = 1280 LUTs
2000 = 2112 LUTs
4000 = 4320 LUTs
7000 = 6864 LUTs

I/O Count
Blank = Standard Device
U = Ultra High I/O Device

Power/Performance
Z = Low Power
H = High Performance

Supply Voltage
C = 2.5 V / 3.3 V
E = 1.2 V

Speed
1 = Slowest
2
3 = Fastest
} Low Power

4 = Slowest
5
6 = Fastest
} High Performance

Package
UWG25 = 25-Ball Halogen-Free WLCSP (0.4 mm Pitch)
SG32 = 32-Pin Halogen-Free QFN (0.5 mm Pitch)
SG48 = 48-Pin Halogen-Free QFN (0.5 mm Pitch)
UWG49 = 49-ball Halogen-Free WLCSP (0.4 mm Pitch)
UMG64 = 64-Ball Halogen-Free ucBGA (0.4 mm Pitch)
QN84 = 84-Pin Halogen-Free QFN (0.5 mm Pitch)
TG100 = 100-Pin Halogen-Free TQFP
TG144 = 144-Pin Halogen-Free TQFP
MG132 = 132-Ball Halogen-Free csBGA (0.5 mm Pitch)
MG184 = 184-Ball Halogen-Free csBGA (0.5 mm Pitch)
BG256 = 256-Ball Halogen-Free caBGA (0.8 mm Pitch)
FTG256 = 256-Ball Halogen-Free ftBGA (1.0 mm Pitch)
BG332 = 332-Ball Halogen-Free caBGA (0.8 mm Pitch)
FG484 = 484-Ball Halogen-Free fpBGA (1.0 mm Pitch)

Grade
C = Commercial
I = Industrial

Shipping Method
Blank = Trays
TR = Tape and Reel

Device Status
Blank = Production Device
ES = Engineering Sample
R1 = Production Release 1 Device
1K = WLCSP Package, 1,000 parts per reel

* 48-pin QFN information is 'Advanced'.

Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32I	256	1.2 V	–1	Halogen-Free QFN	32	IND
LCMXO2-256ZE-2SG32I	256	1.2 V	–2	Halogen-Free QFN	32	IND
LCMXO2-256ZE-3SG32I	256	1.2 V	–3	Halogen-Free QFN	32	IND
LCMXO2-256ZE-1UMG64I	256	1.2 V	–1	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-2UMG64I	256	1.2 V	–2	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-3UMG64I	256	1.2 V	–3	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-1TG100I	256	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-2TG100I	256	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-3TG100I	256	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-1MG132I	256	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-2MG132I	256	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-3MG132I	256	1.2 V	–3	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100I	640	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-2TG100I	640	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-3TG100I	640	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-1MG132I	640	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-2MG132I	640	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-3MG132I	640	1.2 V	–3	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1UWG25ITR[1]	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR50[3]	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR1K[2]	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1SG32I	1280	1.2 V	–1	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-2SG32I	1280	1.2 V	–2	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-3SG32I	1280	1.2 V	–3	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-1TG100I	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100I	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100I	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132I	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132I	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132I	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144I	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144I	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144I	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

MachXO2 Family Data Sheet Supplemental Information

April 2012 **Data Sheet DS1035**

For Further Information

A variety of technical notes for the MachXO2 family are available on the Lattice web site.

- TN1198, Power Estimation and Management for MachXO2 Devices
- TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide
- TN1201, Memory Usage Guide for MachXO2 Devices
- TN1202, MachXO2 sysIO Usage Guide
- TN1203, Implementing High-Speed Interfaces with MachXO2 Devices
- TN1204, MachXO2 Programming and Configuration Usage Guide
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices
- TN1206, MachXO2 SRAM CRC Error Detection Usage Guide
- TN1207, Using TraceID in MachXO2 Devices
- TN1074, PCB Layout Recommendations for BGA Packages
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices
- AN8066, Boundary Scan Testability with Lattice sysIO Capability

- MachXO2 Device Pinout Files
- Thermal Management document
- Lattice design tools

For further information on interface standards, refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, LVDS, DDR, DDR2, LPDDR): www.jedec.org
- PCI: www.pcisig.com

Date	Version	Section	Change Summary
May 2011	01.3	Multiple	Replaced “SED” with “SRAM CRC Error Detection” throughout the document.
		DC and Switching Characteristics	Added footnote 1 to Program Erase Specifications table.
		Pinout Information	Updated Pin Information Summary tables.
			Signal name SO/SISPISO changed to SO/SPISO in the Signal Descriptions table.
April 2011	01.2	—	Data sheet status changed from Advance to Preliminary.
		Introduction	Updated MachXO2 Family Selection Guide table.
		Architecture	Updated Supported Input Standards table.
			Updated sysMEM Memory Primitives diagram.
			Added differential SSTL and HSTL IO standards.
		DC and Switching Characteristics	Updates following parameters: POR voltage levels, DC electrical characteristics, static supply current for ZE/HE/HC devices, static power consumption contribution of different components – ZE devices, programming and erase Flash supply current.
			Added VREF specifications to sysIO recommended operating conditions.
			Updating timing information based on characterization.
			Added differential SSTL and HSTL IO standards.
		Ordering Information	Added Ordering Part Numbers for R1 devices, and devices in WLCSP packages.
			Added R1 device specifications.
January 2011	01.1	All	Included ultra-high I/O devices.
		DC and Switching Characteristics	Recommended Operating Conditions table – Added footnote 3.
			DC Electrical Characteristics table – Updated data for I_{IL}, I_{IH}. V_{HYST} typical values updated.
			Generic DDRX2 Outputs with Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and $T_{DIB.}$
			Generic DDRX4 Outputs with Clock and Data Aligned at Pin (GDDRX4_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and $T_{DIB.}$
			Power-On-Reset Voltage Levels table - clarified note 3.
			Clarified VCCIO related recommended operating conditions specifications.
			Added power supply ramp rate requirements.
			Added Power Supply Ramp Rates table.
			Updated Programming/Erase Specifications table.
			Removed references to $V_{CCP.}$
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Removed references to $V_{CCP.}$
November 2010	01.0	—	Initial release.