E · K Fattice Semiconductor Corporation - <u>LCMX02-4000ZE-3BG256I Datasheet</u>



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	540
Number of Logic Elements/Cells	4320
Total RAM Bits	94208
Number of I/O	206
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-CABGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-4000ze-3bg256i

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MachXO2 Family Data Sheet Introduction

May 2016

Features

- Flexible Logic Architecture
 - Six devices with 256 to 6864 LUT4s and 18 to 334 I/Os
- Ultra Low Power Devices
 - Advanced 65 nm low power process
 - As low as 22 μW standby power
 - Programmable low swing differential I/Os
 - · Stand-by mode and other power saving options

Embedded and Distributed Memory

- Up to 240 kbits sysMEM™ Embedded Block RAM
- Up to 54 kbits Distributed RAM
- Dedicated FIFO control logic
- On-Chip User Flash Memory
 - Up to 256 kbits of User Flash Memory
 - 100,000 write cycles
 - Accessible through WISHBONE, SPI, I²C and JTAG interfaces
 - Can be used as soft processor PROM or as Flash memory

Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/Os
- Generic DDR, DDRX2, DDRX4
- Dedicated DDR/DDR2/LPDDR memory with DQS support

■ High Performance, Flexible I/O Buffer

- Programmable sysIO[™] buffer supports wide range of interfaces:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2
 - LVTTL
 - PCI
 - LVDS, Bus-LVDS, MLVDS, RSDS, LVPECL
 - SSTL 25/18
 - HSTL 18
 - Schmitt trigger inputs, up to 0.5 V hysteresis
- I/Os support hot socketing
- On-chip differential termination
- · Programmable pull-up or pull-down mode

- Flexible On-Chip Clocking
 - · Eight primary clocks
 - Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
 - Up to two analog PLLs per device with fractional-n frequency synthesis
 - Wide input frequency range (7 MHz to 400 MHz)

Data Sheet DS1035

- Non-volatile, Infinitely Reconfigurable
 - Instant-on powers up in microseconds
 - Single-chip, secure solution
 - Programmable through JTAG, SPI or I²C
 - Supports background programming of non-volatile memory
 - Optional dual boot with external SPI memory
- TransFR[™] Reconfiguration
 - In-field logic update while system operates

Enhanced System Level Support

- On-chip hardened functions: SPI, I²C, timer/ counter
- On-chip oscillator with 5.5% accuracy
- Unique TraceID for system tracking
- One Time Programmable (OTP) mode
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming
- Broad Range of Package Options
 - TQFP, WLCSP, ucBGA, csBGA, caBGA, ftBGA, fpBGA, QFN package options
 - Small footprint package options
 As small as 2.5 mm x 2.5 mm
 - · Density migration supported
 - · Advanced halogen-free packaging



The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag "hard" control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysl/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2-640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO2 devices provide commonly used hardened functions such as SPI controller, I²C controller and timer/ counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I²C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

PFU Blocks

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.



ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

Routing

There are many resources provided in the MachXO2 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Each MachXO2 device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO2 architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO2-640U, MachXO2-1200/U and higher density devices have two edge clocks each on the top and bottom edges. Lower density devices have no edge clocks. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO2 devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO2 External Switching Characteristics table.

The primary clock signals for the MachXO2-256 and MachXO2-640 are generated from eight 17:1 muxes The available clock sources include eight I/O sources and 9 routing inputs. Primary clock signals for the MachXO2-640U, MachXO2-1200/U and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.



Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-14 shows the output register block on the left, top and bottom edges.

Figure 2-14. MachXO2 Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)



Right Edge

The output register block on the right edge is a superset of the output register on left, top and bottom edges of the device. In addition to supporting SDR and Generic DDR modes, the output register blocks for PIOs on the right edge include additional logic to support DDR-memory interfaces. Operation of this block is similar to that of the output register block on other edges.

In DDR memory mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the DQSW90 signal is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-15 shows the output register block on the right edge.



Figure 2-17. Output Gearbox



More information on the output gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.



Figure 2-20. Embedded Function Block Interface



Hardened I²C IP Core

Every MachXO2 device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I^2C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I^2C Master. The I^2C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface



There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology (Appendix B)
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices

Figure 2-22. SPI Core Block Diagram



Table 2-16 describes the signals interfacing with the SPI cores.

Table 2-16. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	0	Master	SPI master chip-select output
spi_csn[17]	0	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	0	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
ufm_sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the User Flash Memory (UFM).
cfg_stdby	0	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.
cfg_wake	0	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.



Power-On-Reset Voltage Levels^{1, 2, 3, 4, 5}

Symbol	Parameter	Min.	Тур.	Max.	Units
V _{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and $V_{CCIO0})$	0.9	_	1.06	V
V _{PORUPEXT}	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	_	2.1	V
V _{PORDNBG}	Power-On-Reset ramp down trip point (band gap based circuit monitoring $V_{CCINT})$	0.75	_	0.93	V
V _{PORDNBGEXT}	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	_	1.33	V
V _{PORDNSRAM}	Power-On-Reset ramp down trip point (SRAM based circuit monitoring $V_{\mbox{CCINT}}$)	-	0.6	_	V
V _{PORDNSRAMEXT}	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	_	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.

3. Note that V_{PORUP} (min.) and V_{PORDNBG} (max.) are in different process corners. For any given process corner V_{PORDNBG} (max.) is always 12.0 mV below V_{PORUP} (min.).

4. V_{PORUPEXT} is for HC devices only. In these devices a separate POR circuit monitors the external V_{CC} power supply.

5. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

Programming/Erase Specifications

Symbol	Parameter	Min.	Max. ¹	Units	
	Flash Programming cycles per t _{RETENTION}	—	10,000	Cycles	
PROGCYC	Flash functional programming cycles	—	100,000	Cycles	
+	Data retention at 100 °C junction temperature	10	—	Voars	
RETENTION	Data retention at 85 °C junction temperature	20	—	leais	

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

Hot Socketing Specifications^{1, 2, 3}

I_{DK} Input or I/O leakage Current $0 < V_{IN} < V_{IH}$ (MAX) +/-1000 μ A	Symbol	Parameter	Condition	Max.	Units
	I _{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/-1000	μΑ

1. Insensitive to sequence of V_{CC} and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO} .

2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).

3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

ESD Performance

Please refer to the MachXO2 Product Family Qualification Summary for complete qualification data, including ESD performance.



Programming and Erase Flash Supply Current – ZE Devices^{1, 2, 3, 4}

Symbol	Parameter	Device	Typ.⁵	Units
		LCMXO2-256ZE	13	mA
		LCMXO2-640ZE	14	mA
1	Core Power Supply	LCMXO2-1200ZE	15	mA
CC		LCMXO2-2000ZE	17	mA
		LCMXO2-4000ZE	18	mA
		LCMXO2-7000ZE	20	mA
I _{CCIO}	Bank Power Supply ⁶	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.

2. Assumes all inputs are held at $V_{\mbox{CCIO}}$ or GND and all outputs are tri-stated.

3. Typical user pattern.

4. JTAG programming is at 25 MHz.

5. TJ = 25 °C, power supplies at nominal voltage.

6. Per bank. $V_{CCIO} = 2.5$ V. Does not include pull-up/pull-down.



sysIO Recommended Operating Conditions

	V _{CCIO} (V) V _{REF} (V)					
Standard	Min.	Тур.	Max.	Min.	Тур.	Max.
LVCMOS 3.3	3.135	3.3	3.6	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.6	—	—	—
PCI ³	3.135	3.3	3.6	—	—	—
SSTL25	2.375	2.5	2.625	1.15	1.25	1.35
SSTL18	1.71	1.8	1.89	0.833	0.9	0.969
HSTL18	1.71	1.8	1.89	0.816	0.9	1.08
LVCMOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVCMOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVCMOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVCMOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVCMOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVCMOS12R334	3.135	3.3	3.6	0.45	0.6	0.75
LVCMOS12R254	2.375	2.5	2.625	0.45	0.6	0.75
LVCMOS10R334	3.135	3.3	3.6	0.35	0.5	0.65
LVCMOS10R254	2.375	2.5	2.625	0.35	0.5	0.65
LVDS25 ^{1, 2}	2.375	2.5	2.625	—	—	—
LVDS33 ^{1, 2}	3.135	3.3	3.6	—	—	—
LVPECL ¹	3.135	3.3	3.6	—	—	—
BLVDS ¹	2.375	2.5	2.625	—	—	—
RSDS ¹	2.375	2.5	2.625	—	—	—
SSTL18D	1.71	1.8	1.89	—	—	—
SSTL25D	2.375	2.5	2.625	—	—	—
HSTL18D	1.71	1.8	1.89	—	—	—

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.

2. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.

3. Input on the bottom bank of the MachXO2-640U, MachXO2-1200/U and larger devices only.

4. Supported only for inputs and BIDIs for all ZE devices, and -6 speed grade for HE and HC devices.



Input/Output	V _{IL}		V _{IH}		V _{OL} Max.	V _{OH} Min.	I _{OL} Max. ⁴	I _{OH} Max. ⁴	
Standard	Min. (V) ³	Max. (V)	Min. (V)	Max. (V)	ς(Λ)	(V)	ິ(mA)	(mA)	
LVCMOS10R25	-0.3	V _{REF} – 0.1	V _{REF} + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain	

MachXO2 devices allow LVCMOS inputs to be placed in I/O banks where V_{CCIO} is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO2 devices do not meet the relevant JEDEC specification are documented in the table below.

2. MachXO2 devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1202, MachXO2 sysIO Usage Guide.

3. The dual function I²C pins SCL and SDA are limited to a V_{IL} min of -0.25 V or to -0.3 V with a duration of <10 ns.

4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive VCCIO or GND pad connections, or between the last VCCIO or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n * 8 mA. "n" is the number of I/O pads between the two consecutive bank VCCIO or GND connections or between the last VCCIO and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

Input Standard	V _{CCIO} (V)	V _{IL} Max. (V)
LVCMOS 33	1.5	0.685
LVCMOS 25	1.5	0.687
LVCMOS 18	1.5	0.655

sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of MachXO2-640U, MachXO2-1200/U and higher density devices in the MachXO2 PLD family.

LVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Тур.	Max.	Units
V	Input Voltage	V _{CCIO} = 3.3 V	0		2.605	V
VINB VINM	input voltage	V _{CCIO} = 2.5 V	0		2.05	V
V _{THD}	Differential Input Threshold		±100			mV
V	Input Common Mode Voltage	V _{CCIO} = 3.3 V	0.05		2.6	V
V CM	input common mode voltage	V _{CCIO} = 2.5 V	0.05		2.0	V
I _{IN}	Input current	Power on	_		±10	μΑ
V _{OH}	Output high voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	_	1.375	_	V
V _{OL}	Output low voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	0.90	1.025	_	V
V _{OD}	Output voltage differential	(V _{OP} - V _{OM}), R _T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V _{OD} between high and low		_		50	mV
V _{OS}	Output voltage offset	$(V_{OP} + V_{OM})/2, R_{T} = 100 \text{ Ohm}$	1.125	1.20	1.395	V
ΔV_{OS}	Change in V _{OS} between H and L		_	_	50	mV
I _{OSD}	Output short circuit current	V _{OD} = 0 V driver outputs shorted	_		24	mA



LVDS Emulation

MachXO2 devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.





Note: All resistors are ±1%.

Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Тур.	Units
Z _{OUT}	Output impedance	20	Ohms
R _S	Driver series resistor	158	Ohms
R _P	Driver parallel resistor	140	Ohms
R _T	Receiver termination	100	Ohms
V _{OH}	Output high voltage	1.43	V
V _{OL}	Output low voltage	1.07	V
V _{OD}	Output differential voltage		V
V _{CM}	CM Output common mode voltage		V
Z _{BACK}	Back impedance	100.5	Ohms
I _{DC}	DC output current	6.03	mA





			_	6	_	5	_	4	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
		MachXO2-256HC-HE	1.42	_	1.59	_	1.96	_	ns
	Clock to Data Setup – PIO	MachXO2-640HC-HE	1.41	_	1.58	_	1.96	_	ns
		MachXO2-1200HC-HE	1.63	_	1.79	_	2.17	_	ns
t _{SU_DEL} Inpi Del	Delav	MachXO2-2000HC-HE	1.61	_	1.76	_	2.13	_	ns
		MachXO2-4000HC-HE	1.66	_	1.81	_	2.19	_	ns
		MachXO2-7000HC-HE	1.53	_	1.67		2.03		ns
		MachXO2-256HC-HE	-0.24	_	-0.24		-0.24		ns
		MachXO2-640HC-HE	-0.23	_	-0.23	_	-0.23	_	ns
+	Clock to Data Hold – PIO Input	MachXO2-1200HC-HE	-0.24	_	-0.24	_	-0.24	_	ns
'H_DEL	Register with Input Data Delay	MachXO2-2000HC-HE	-0.23	_	-0.23		-0.23		ns
		MachXO2-4000HC-HE	-0.25	_	-0.25		-0.25		ns
		MachXO2-7000HC-HE	-0.21		-0.21		-0.21		ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices		388	_	323	_	269	MHz
General I/O	Pin Parameters (Using Edge C	lock without PLL)							
		MachXO2-1200HC-HE	_	7.53		7.76		8.10	ns
+	Clock to Output – PIO Output	MachXO2-2000HC-HE		7.53		7.76		8.10	ns
t _{COE}	Register	MachXO2-4000HC-HE		7.45		7.68		8.00	ns
		MachXO2-7000HC-HE		7.53		7.76		8.10	ns
	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	-0.19	_	-0.19	_	-0.19	_	ns
		MachXO2-2000HC-HE	-0.19	_	-0.19	_	-0.19	_	ns
SUE		MachXO2-4000HC-HE	-0.16	_	-0.16	_	-0.16	_	ns
		MachXO2-7000HC-HE	-0.19	_	-0.19		-0.19		ns
		MachXO2-1200HC-HE	1.97	_	2.24	_	2.52	_	ns
	Clock to Data Hold – PIO Input	MachXO2-2000HC-HE	1.97	_	2.24	_	2.52	_	ns
ЧЕ	Register	MachXO2-4000HC-HE	1.89	_	2.16	_	2.43		ns
		MachXO2-7000HC-HE	1.97	_	2.24	_	2.52	_	ns
		MachXO2-1200HC-HE	1.56	_	1.69	_	2.05	_	ns
	Clock to Data Setup – PIO	MachXO2-2000HC-HE	1.56	_	1.69	_	2.05	_	ns
^I SU_DELE	Delay	MachXO2-4000HC-HE	1.74	_	1.88	_	2.25	_	ns
t _{HE} t _{SU_DELE}		MachXO2-7000HC-HE	1.66	_	1.81	_	2.17	_	ns
		MachXO2-1200HC-HE	-0.23	_	-0.23	_	-0.23	_	ns
+	Clock to Data Hold – PIO Input	MachXO2-2000HC-HE	-0.23	_	-0.23		-0.23		ns
'H_DELE	Register with Input Data Delay	MachXO2-4000HC-HE	-0.34	_	-0.34		-0.34		ns
		MachXO2-7000HC-HE	-0.29	_	-0.29		-0.29		ns
General I/O	Pin Parameters (Using Primary	y Clock with PLL)							
		MachXO2-1200HC-HE	—	5.97		6.00		6.13	ns
	Clock to Output – PIO Output	MachXO2-2000HC-HE		5.98		6.01		6.14	ns
COPLL	Register	MachXO2-4000HC-HE		5.99		6.02		6.16	ns
		MachXO2-7000HC-HE		6.02		6.06		6.20	ns
		MachXO2-1200HC-HE	0.36	—	0.36	—	0.65	—	ns
+.	Clock to Data Setup – PIO	MachXO2-2000HC-HE	0.36	—	0.36	—	0.63	—	ns
SUPLL	Input Register	MachXO2-4000HC-HE	0.35	—	0.35	—	0.62	—	ns
		MachXO2-7000HC-HE	0.34	—	0.34	—	0.59	—	ns
	1	•			•		•		



			-6		-5		-4		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Generic DDR	X2 Outputs with Clock and Data	Centered at Pin Using P	CLK Pin	for Cloc	k Input –	GDDRX	2_TX.EC	LK.Cen	tered ^{9, 12}
t _{DVB}	Output Data Valid Before CLK Output		0.535	_	0.670	_	0.830	_	ns
t _{DVA}	Output Data Valid After CLK Output	MachXO2-640U,	0.535	—	0.670	_	0.830	_	ns
f _{DATA}	DDRX2 Serial Output Data Speed	MachXO2-1200/U and larger devices, top side	_	664	_	554	_	462	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		_	332	_	277	_	231	MHz
f _{SCLK}	SCLK Frequency			166	—	139		116	MHz
Generic DDF	X4 Outputs with Clock and Data	a Aligned at Pin Using P	CLK Pin	for Cloc	k Input	- GDDR	X4_TX.E	CLK.Ali	gned ^{9, 12}
t _{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	_	0.200	_	0.215	_	0.230	ns
t _{DIB}	Output Data Invalid Before CLK Output		_	0.200	_	0.215	_	0.230	ns
f _{DATA}	DDRX4 Serial Output Data Speed		_	756	_	630	_	524	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency			378		315		262	MHz
f _{SCLK}	SCLK Frequency			95	—	79	—	66	MHz
Generic DDF	X4 Outputs with Clock and Data	Centered at Pin Using P	CLK Pin	for Cloc	k Input –	GDDRX	4_ TX.EC	LK.Cen	tered ^{9, 12}
t _{DVB}	Output Data Valid Before CLK Output		0.455	_	0.570	_	0.710	_	ns
t _{DVA}	Output Data Valid After CLK Output	MachXO2-640U,	0.455	_	0.570	_	0.710	_	ns
f _{DATA}	DDRX4 Serial Output Data Speed	larger devices, top side	_	756	_	630	_	524	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)	only.	_	378	_	315	_	262	MHz
f _{SCLK}	SCLK Frequency			95	—	79	—	66	MHz
7:1 LVDS Ou	utputs – GDDR71_TX.ECLK.7:	1 ^{9, 12}						•	
t _{DIB}	Output Data Invalid Before CLK Output		_	0.160	_	0.180	_	0.200	ns
t _{DIA}	Output Data Invalid After CLK Output	MachXO2-640U.	_	0.160	_	0.180	_	0.200	ns
f _{DATA}	DDR71 Serial Output Data Speed	MachXO2-1200/U and larger devices, top side	_	756	_	630	_	524	Mbps
f _{DDR71}	DDR71 ECLK Frequency	only.		378	—	315	_	262	MHz
fclkout	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		_	108	_	90	_	75	MHz



			-6		-5		-4		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
LPDDR ^{9, 12}	·	·			•	•			
t _{DVADQ}	Input Data Valid After DQS Input		_	0.369	_	0.395	_	0.421	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.529	_	0.530	_	0.527	_	UI
t _{DQVBS}	Output Data Invalid Before DQS Output	MachXO2-1200/U and	0.25	_	0.25		0.25	_	UI
t _{DQVAS}	Output Data Invalid After DQS Output	larger devices, right side only. ¹³	0.25	_	0.25	_	0.25	_	UI
f _{DATA}	MEM LPDDR Serial Data Speed	-	_	280	_	250	_	208	Mbps
f _{SCLK}	SCLK Frequency			140	—	125	—	104	MHz
f _{LPDDR}	LPDDR Data Transfer Rate		0	280	0	250	0	208	Mbps
DDR ^{9, 12}									
t _{DVADQ}	Input Data Valid After DQS Input		_	0.350	_	0.387	_	0.414	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.545	_	0.538		0.532	_	UI
t _{DQVBS}	Output Data Invalid Before DQS Output	MachXO2-1200/U and larger devices, right	0.25	_	0.25	_	0.25	_	UI
t _{DQVAS}	Output Data Invalid After DQS Output	side only. ¹³	0.25	_	0.25	_	0.25	_	UI
f _{DATA}	MEM DDR Serial Data Speed			300	—	250	—	208	Mbps
f _{SCLK}	SCLK Frequency			150	—	125	—	104	MHz
f _{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps
DDR2 ^{9, 12}									
t _{DVADQ}	Input Data Valid After DQS Input		_	0.360	_	0.378	_	0.406	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.555	_	0.549	_	0.542	_	UI
t _{DQVBS}	Output Data Invalid Before DQS Output	MachXO2-1200/U and	0.25	_	0.25	_	0.25	_	UI
t _{DQVAS}	Output Data Invalid After DQS Output	larger devices, right side only. ¹³	0.25	_	0.25	_	0.25	_	UI
f _{DATA}	MEM DDR Serial Data Speed	1	—	300	—	250	—	208	Mbps
f _{SCLK}	SCLK Frequency	1	—	150	—	125	—	104	MHz
f _{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.

3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).

4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.

5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).

6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$.

7. The $t_{SU_{DEL}}$ and $t_{H_{DEL}}$ values use the SCLK_ZERHOLD default step size. Each step is 105 ps (-6), 113 ps (-5), 120 ps (-4).

8. This number for general purpose usage. Duty cycle tolerance is +/- 10%.

9. Duty cycle is +/-5% for system usage.

10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.

11. High-speed DDR and LVDS not supported in SG32 (32 QFN) packages.

12. Advance information for MachXO2 devices in 48 QFN packages.

13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.



sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Modes			1		
t _{PRGM}	PROGRAMN low p	ulse accept	55		ns
t _{PRGMJ}	PROGRAMN low p	ulse rejection	—	25	ns
t _{INITL}	INITN low time	LCMXO2-256	—	30	μs
		LCMXO2-640	—	35	μs
		LCMXO2-640U/ LCMXO2-1200	_	55	μs
		LCMXO2-1200U/ LCMXO2-2000	—	70	μs
		LCMXO2-2000U/ LCMXO2-4000	—	105	μs
		LCMXO2-7000	—	130	μs
t _{DPPINIT}	PROGRAMN low to	D INITN Iow	—	150	ns
t _{DPPDONE}	PROGRAMN low to	DONE low	—	150	ns
t _{IODISS}	PROGRAMN low to	o I/O disable	—	120	ns
Slave SPI	·				
f _{MAX}	CCLK clock frequency		—	66	MHz
t _{ССLКН}	CCLK clock pulse width high		7.5	—	ns
t _{CCLKL}	CCLK clock pulse width low		7.5	_	ns
t _{STSU}	CCLK setup time		2	—	ns
t _{STH}	CCLK hold time		0	—	ns
t _{STCO}	CCLK falling edge	to valid output	—	10	ns
t _{STOZ}	CCLK falling edge	to valid disable	—	10	ns
t _{STOV}	CCLK falling edge	to valid enable	—	10	ns
t _{SCS}	Chip select high tim	ne	25	—	ns
t _{SCSS}	Chip select setup ti	me	3	—	ns
t _{SCSH}	Chip select hold tim	ne	3	—	ns
Master SPI					
f _{MAX}	MCLK clock freque	ncy	—	133	MHz
t _{MCLKH}	MCLK clock pulse v	width high	3.75	—	ns
t _{MCLKL}	MCLK clock pulse v	width low	3.75	—	ns
t _{STSU}	MCLK setup time		5		ns
t _{STH}	MCLK hold time		1		ns
t _{CSSPI}	INITN high to chip	select low	100	200	ns
t _{MCLK}	INITN high to first N	MCLK edge	0.75	1	μs



				MachX	02-4000			
	84 QFN	132 csBGA	144 TQFP	184 csBGA	256 caBGA	256 ftBGA	332 caBGA	484 fpBGA
General Purpose I/O per Bank								
Bank 0	27	25	27	37	50	50	68	70
Bank 1	10	26	29	37	52	52	68	68
Bank 2	22	28	29	39	52	52	70	72
Bank 3	0	7	9	10	16	16	24	24
Bank 4	9	8	10	12	16	16	16	16
Bank 5	0	10	10	15	20	20	28	28
Total General Purpose Single Ended I/O	68	104	114	150	206	206	274	278
Differential I/O per Bank								
Bank 0	13	13	14	18	25	25	34	35
Bank 1	4	13	14	18	26	26	34	34
Bank 2	11	14	14	19	26	26	35	36
Bank 3	0	3	4	4	8	8	12	12
Bank 4	4	4	5	6	8	8	8	8
Bank 5	0	5	5	7	10	10	14	14
Total General Purpose Differential I/O	32	52	56	72	103	103	137	139
Dual Function I/O	28	37	37	37	37	37	37	37
High-speed Differential I/O								
Bank 0	8	8	9	8	18	18	18	18
Gearboxes					-			-
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	8	8	9	9	18	18	18	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	11	14	14	12	18	18	18	18
DQS Groups								
Bank 1	1	2	2	2	2	2	2	2
VCCIO Pins								
Bank 0	3	3	3	3	4	4	4	10
Bank 1	1	3	3	3	4	4	4	10
Bank 2	2	3	3	3	4	4	4	10
Bank 3	1	1	1	1	1	1	2	3
Bank 4	1	1	1	1	2	2	1	4
Bank 5	1	1	1	1	1	1	2	3
		1						
VCC	4	4	4	4	8	8	8	12
GND	4	10	12	16	24	24	27	48
NC	1	1	1	1	1	1	5	105
Reserved for configuration	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	84	132	144	184	256	256	332	484



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-6BG332C	4320	1.2 V	-6	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-4FG484C	4320	1.2 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-5FG484C	4320	1.2 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-6FG484C	4320	1.2 V	-6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144C	6864	1.2 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-5TG144C	6864	1.2 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-6TG144C	6864	1.2 V	-6	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-4BG256C	6864	1.2 V	-4	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-5BG256C	6864	1.2 V	-5	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-6BG256C	6864	1.2 V	-6	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-4FTG256C	6864	1.2 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-5FTG256C	6864	1.2 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-6FTG256C	6864	1.2 V	-6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-4BG332C	6864	1.2 V	-4	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-5BG332C	6864	1.2 V	-5	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-6BG332C	6864	1.2 V	-6	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-4FG484C	6864	1.2 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-5FG484C	6864	1.2 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-6FG484C	6864	1.2 V	-6	Halogen-Free fpBGA	484	COM



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1UWG49ITR ¹	2112	1.2 V	-1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR50 ³	2112	1.2 V	-1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR1K ²	2112	1.2 V	-1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1TG100I	2112	1.2 V	-1	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-2TG100I	2112	1.2 V	-2	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-3TG100I	2112	1.2 V	-3	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-1MG132I	2112	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-2MG132I	2112	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-3MG132I	2112	1.2 V	-3	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-1TG144I	2112	1.2 V	-1	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-2TG144I	2112	1.2 V	-2	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-3TG144I	2112	1.2 V	-3	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-1BG256I	2112	1.2 V	-1	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-2BG256I	2112	1.2 V	-2	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-3BG256I	2112	1.2 V	-3	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-1FTG256I	2112	1.2 V	-1	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-2FTG256I	2112	1.2 V	-2	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-3FTG256I	2112	1.2 V	-3	Halogen-Free ftBGA	256	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.

2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.

3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100IR11	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100IR11	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100IR11	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132IR11	1280	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132IR1 ¹	1280	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132IR11	1280	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144IR1 ¹	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144IR1 ¹	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144IR11	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND

1. Specifications for the "LCMXO2-1200HC-speed package IR1" are the same as the "LCMXO2-1200ZE-speed package I" devices respectively, except as specified in the R1 Device Specifications section of this data sheet.