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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Active
Number of LABs/CLBs	540
Number of Logic Elements/Cells	4320
Total RAM Bits	94208
Number of I/O	274
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	332-FBGA
Supplier Device Package	332-CABGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmx02-4000ze-3bg332c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmx02-4000ze-3bg332c</a>

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## Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I<sup>2</sup>C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external V<sub>CC</sub> supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V<sub>CC</sub> supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I<sup>2</sup>C port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

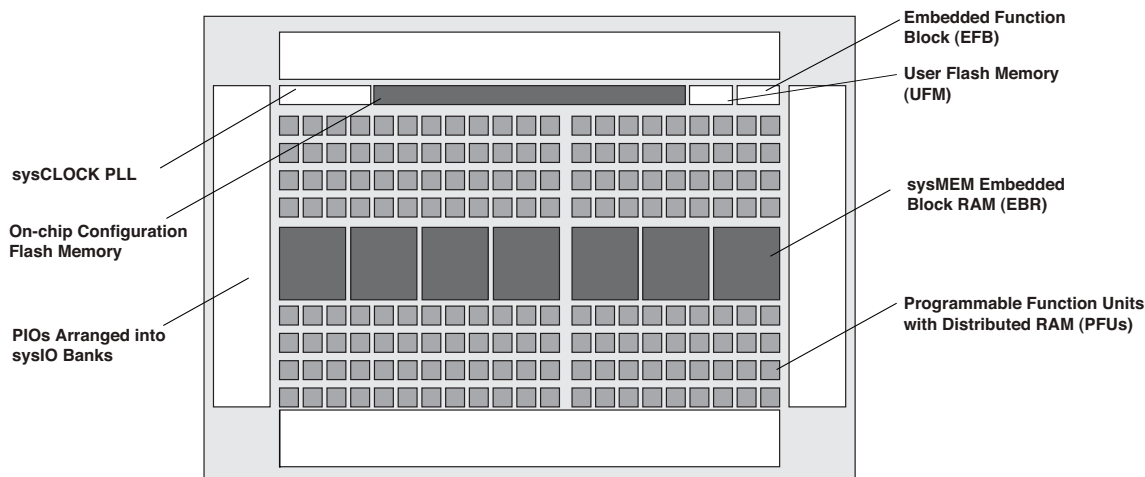
Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

## Architecture Overview

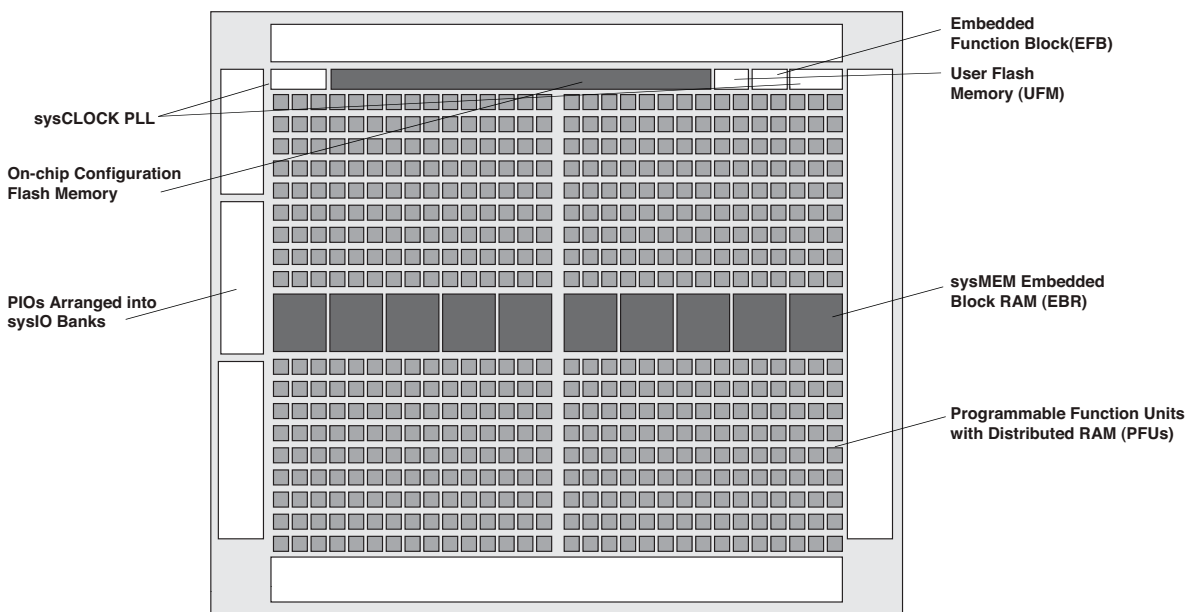
The MachXO2 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.

**Figure 2-1. Top View of the MachXO2-1200 Device**



Note: MachXO2-256, and MachXO2-640/U are similar to MachXO2-1200. MachXO2-256 has a lower LUT count and no PLL or EBR blocks. MachXO2-640 has no PLL, a lower LUT count and two EBR blocks. MachXO2-640U has a lower LUT count, one PLL and seven EBR blocks.

**Figure 2-2. Top View of the MachXO2-4000 Device**



Note: MachXO2-1200U, MachXO2-2000/U and MachXO2-7000 are similar to MachXO2-4000. MachXO2-1200U and MachXO2-2000 have a lower LUT count, one PLL, and eight EBR blocks. MachXO2-2000U has a lower LUT count, two PLLs, and 10 EBR blocks. MachXO2-7000 has a higher LUT count, two PLLs, and 26 EBR blocks.

**Table 2-13. Supported Output Standards**

Output Standard	V <sub>CCIO</sub> (Typ.)
<b>Single-Ended Interfaces</b>	
LVTTL	3.3
LVC MOS33	3.3
LVC MOS25	2.5
LVC MOS18	1.8
LVC MOS15	1.5
LVC MOS12	1.2
LVC MOS33, Open Drain	—
LVC MOS25, Open Drain	—
LVC MOS18, Open Drain	—
LVC MOS15, Open Drain	—
LVC MOS12, Open Drain	—
PCI33	3.3
SSTL25 (Class I)	2.5
SSTL18 (Class I)	1.8
HSTL18(Class I)	1.8
<b>Differential Interfaces</b>	
LVDS <sup>1,2</sup>	2.5, 3.3
BLVDS, MLVDS, RSDS <sup>2</sup>	2.5
LVPECL <sup>2</sup>	3.3
MIPI <sup>2</sup>	2.5
Differential SSTL18	1.8
Differential SSTL25	2.5
Differential HSTL18	1.8

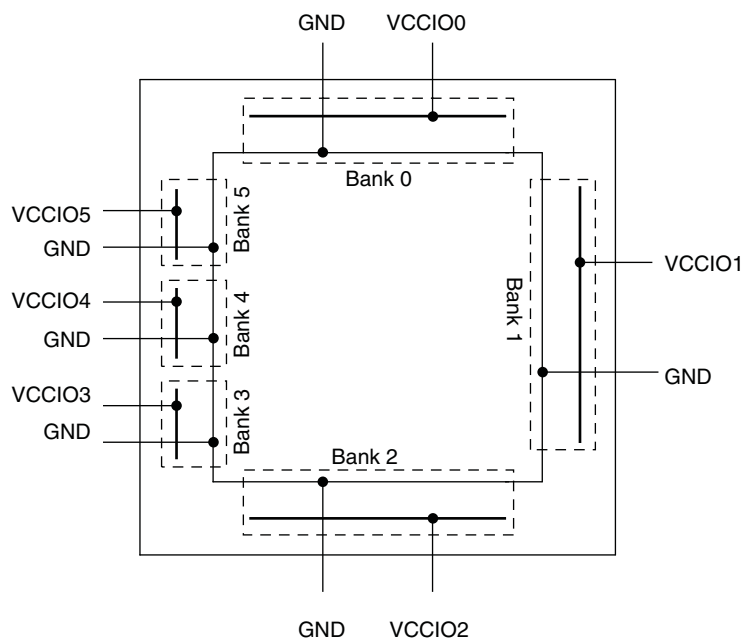
1. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.

2. These interfaces can be emulated with external resistors in all devices.

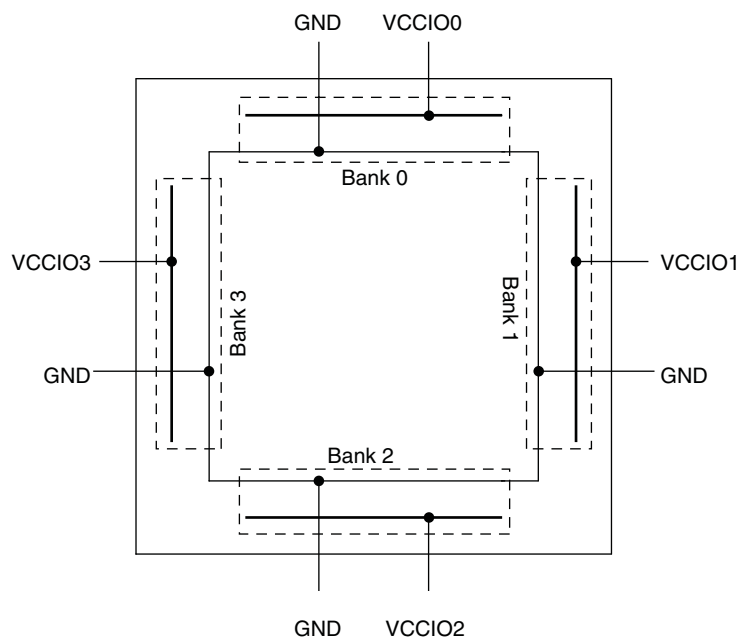
## sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO2-1200U, MachXO2-2000/U and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO2-1200 and lower density devices have four banks (one bank per side). Figures 2-18 and 2-19 show the sysIO banks and their associated supplies for all devices.

**Figure 2-18. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 Banks**



**Figure 2-19. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks**



## Hot Socketing

The MachXO2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO2 ideal for many multiple power supply and hot-swap applications.

## On-chip Oscillator

Every MachXO2 device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
2. During configuration, users select a different master clock frequency.
3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-14 lists all the available MCLK frequencies.

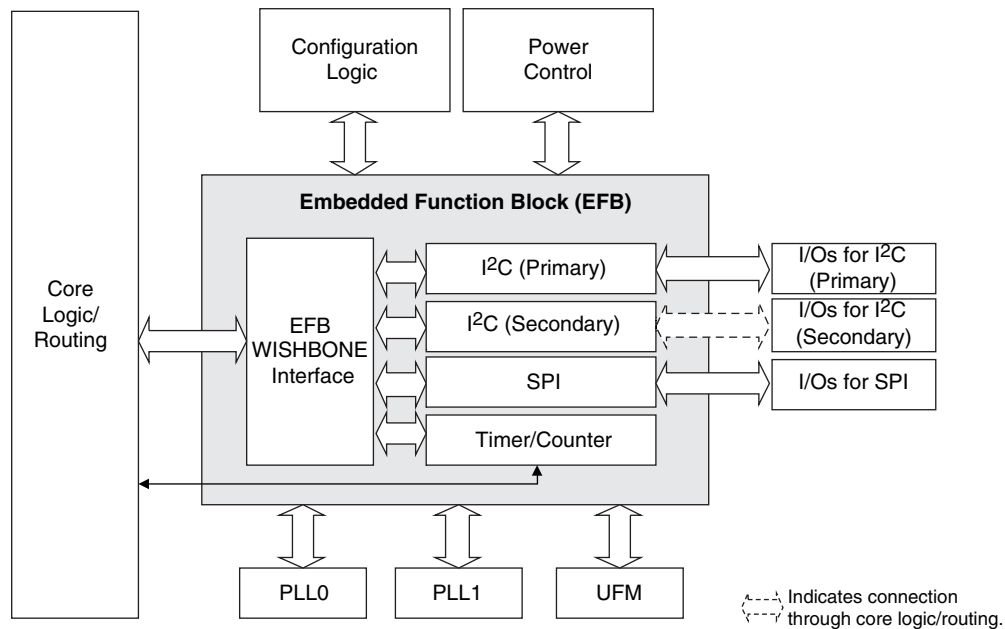
**Table 2-14. Available MCLK Frequencies**

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

## Embedded Hardened IP Functions and User Flash Memory

All MachXO2 devices provide embedded hardened functions such as SPI, I<sup>2</sup>C and Timer/Counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2-20.

**Figure 2-20. Embedded Function Block Interface**



## Hardened I<sup>2</sup>C IP Core

Every MachXO2 device contains two I<sup>2</sup>C IP cores. These are the primary and secondary I<sup>2</sup>C IP cores. Either of the two cores can be configured either as an I<sup>2</sup>C master or as an I<sup>2</sup>C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I<sup>2</sup>C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I<sup>2</sup>C Master. The I<sup>2</sup>C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface

**Figure 2-21. I<sup>2</sup>C Core Block Diagram**

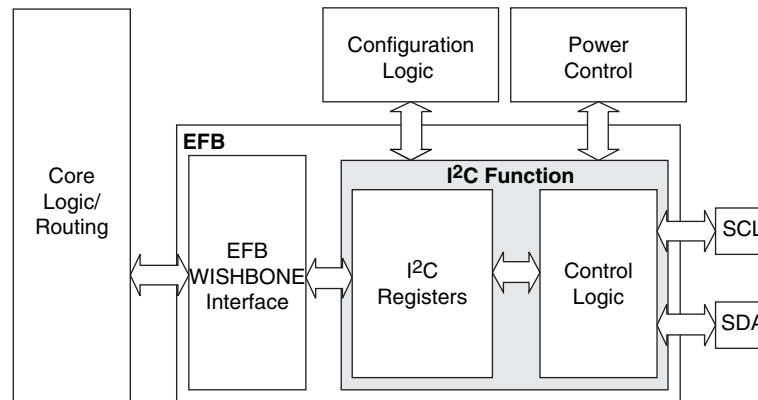


Table 2-15 describes the signals interfacing with the I<sup>2</sup>C cores.

**Table 2-15. I<sup>2</sup>C Core Signal Description**

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I <sup>2</sup> C core. The signal is an output if the I <sup>2</sup> C core is in master mode. The signal is an input if the I <sup>2</sup> C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I <sup>2</sup> C ports in each MachXO2 device.
i2c_sda	Bi-directional	Bi-directional data line of the I <sup>2</sup> C core. The signal is an output when data is transmitted from the I <sup>2</sup> C core. The signal is an input when data is received into the I <sup>2</sup> C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I <sup>2</sup> C ports in each MachXO2 device.
i2c_irqo	Output	Interrupt request output signal of the I <sup>2</sup> C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I <sup>2</sup> C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I <sup>2</sup> C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I <sup>2</sup> C Tab.

## Hardened SPI IP Core

Every MachXO2 device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO2 devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface

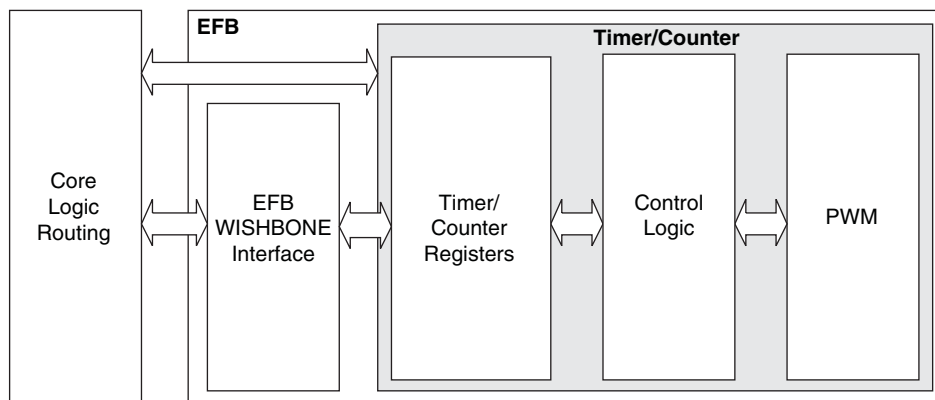


## Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  - Watchdog timer
  - Clear timer on compare match
  - Fast PWM
  - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

**Figure 2-23. Timer/Counter Block Diagram**



**Table 2-17. Timer/Counter Signal Description**

Port	I/O	Description
tc_clk	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	O	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	O	Timer counter output signal

**Table 2-18. MachXO2 Power Saving Features Description**

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors V <sub>CC</sub> levels. In the event of unsafe V <sub>CC</sub> drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).

## Power On Reset

MachXO2 devices have power-on reset circuitry to monitor V<sub>CCINT</sub> and V<sub>CCIO</sub> voltage levels during power-up and operation. At power-up, the POR circuitry monitors V<sub>CCINT</sub> and V<sub>CCIO0</sub> (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the V<sub>PORUP</sub> level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices), V<sub>CCINT</sub> is the same as the V<sub>CC</sub> supply voltage. For devices with voltage regulators (HC devices), V<sub>CCINT</sub> is regulated from the V<sub>CC</sub> supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time (t<sub>REFRESH</sub>) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external V<sub>CC</sub> voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V<sub>CCINT</sub> levels. If V<sub>CCINT</sub> drops below V<sub>PORDNBG</sub> level (with the bandgap circuitry switched on) or below V<sub>PORDNSRAM</sub> level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V<sub>CCINT</sub> and V<sub>CCIO</sub> voltage levels. V<sub>PORDNBG</sub> and V<sub>PORDNSRAM</sub> are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the V<sub>PORDNSRAM</sub> reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V<sub>CC</sub> supply dropping below V<sub>CC</sub> (min) they should not shut down the bandgap or POR circuit.

### Power-On-Reset Voltage Levels<sup>1, 2, 3, 4, 5</sup>

Symbol	Parameter	Min.	Typ.	Max.	Units
$V_{PORUP}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring $V_{CCINT}$ and $V_{CCIO0}$ )	0.9	—	1.06	V
$V_{PORUPEXT}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring external $V_{CC}$ power supply)	1.5	—	2.1	V
$V_{PORDNBG}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring $V_{CCINT}$ )	0.75	—	0.93	V
$V_{PORDNBGEXT}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring $V_{CC}$ )	0.98	—	1.33	V
$V_{PORDNSRAM}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring $V_{CCINT}$ )	—	0.6	—	V
$V_{PORDNSRAMEXT}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring $V_{CC}$ )	—	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators  $V_{CCINT}$  is the same as the  $V_{CC}$  supply voltage. For devices with voltage regulators,  $V_{CCINT}$  is regulated from the  $V_{CC}$  supply voltage.
3. Note that  $V_{PORUP}$  (min.) and  $V_{PORDNBG}$  (max.) are in different process corners. For any given process corner  $V_{PORDNBG}$  (max.) is always 12.0 mV below  $V_{PORUP}$  (min.).
4.  $V_{PORUPEXT}$  is for HC devices only. In these devices a separate POR circuit monitors the external  $V_{CC}$  power supply.
5.  $V_{CCIO0}$  does not have a Power-On-Reset ramp down trip point.  $V_{CCIO0}$  must remain within the Recommended Operating Conditions to ensure proper operation.

### Programming/Erase Specifications

Symbol	Parameter	Min.	Max. <sup>1</sup>	Units
$N_{PROG}$	Flash Programming cycles per $t_{RETENTION}$	—	10,000	Cycles
	Flash functional programming cycles	—	100,000	
$t_{RETENTION}$	Data retention at 100 °C junction temperature	10	—	Years
	Data retention at 85 °C junction temperature	20	—	

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

### Hot Socketing Specifications<sup>1, 2, 3</sup>

Symbol	Parameter	Condition	Max.	Units
$I_{DK}$	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/-1000	$\mu A$

1. Insensitive to sequence of  $V_{CC}$  and  $V_{CCIO}$ . However, assumes monotonic rise/fall rates for  $V_{CC}$  and  $V_{CCIO}$ .
2.  $0 < V_{CC} < V_{CC} (MAX)$ ,  $0 < V_{CCIO} < V_{CCIO} (MAX)$ .
3.  $I_{DK}$  is additive to  $I_{PU}$ ,  $I_{PD}$  or  $I_{BH}$ .

### ESD Performance

Please refer to the [MachXO2 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

### Static Supply Current – ZE Devices<sup>1, 2, 3, 6</sup>

Symbol	Parameter	Device	Typ. <sup>4</sup>	Units
$I_{CC}$	Core Power Supply	LCMXO2-256ZE	18	$\mu A$
		LCMXO2-640ZE	28	$\mu A$
		LCMXO2-1200ZE	56	$\mu A$
		LCMXO2-2000ZE	80	$\mu A$
		LCMXO2-4000ZE	124	$\mu A$
		LCMXO2-7000ZE	189	$\mu A$
$I_{CCIO}$	Bank Power Supply <sup>5</sup> $V_{CCIO} = 2.5 V$	All devices	1	$\mu A$

- For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).
- Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at  $V_{CCIO}$  or GND, on-chip oscillator is off, on-chip PLL is off. To estimate the impact of turning each of these items on, please refer to the following table or for more detail with your specific design use the Power Calculator tool.
- Frequency = 0 MHz.
- $T_J = 25^\circ C$ , power supplies at nominal voltage.
- Does not include pull-up/pull-down.
- To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

### Static Power Consumption Contribution of Different Components – ZE Devices

The table below can be used for approximating static power consumption. For a more accurate power analysis for your design please use the Power Calculator tool.

Symbol	Parameter	Typ.	Units
$I_{DCBG}$	Bandgap DC power contribution	101	$\mu A$
$I_{DCPOR}$	POR DC power contribution	38	$\mu A$
$I_{DCIOBANKCONTROLLER}$	DC power contribution per I/O bank controller	143	$\mu A$

### Static Supply Current – HC/HE Devices<sup>1, 2, 3, 6</sup>

Symbol	Parameter	Device	Typ. <sup>4</sup>	Units
$I_{CC}$	Core Power Supply	LCMXO2-256HC	1.15	mA
		LCMXO2-640HC	1.84	mA
		LCMXO2-640UHC	3.48	mA
		LCMXO2-1200HC	3.49	mA
		LCMXO2-1200UHC	4.80	mA
		LCMXO2-2000HC	4.80	mA
		LCMXO2-2000UHC	8.44	mA
		LCMXO2-4000HC	8.45	mA
		LCMXO2-7000HC	12.87	mA
		LCMXO2-2000HE	1.39	mA
		LCMXO2-4000HE	2.55	mA
		LCMXO2-7000HE	4.06	mA
$I_{CCIO}$	Bank Power Supply <sup>5</sup> $V_{CCIO} = 2.5\text{ V}$	All devices	0	mA

- For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).
- Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at  $V_{CCIO}$  or GND, on-chip oscillator is off, on-chip PLL is off.
- Frequency = 0 MHz.
- $T_J = 25\text{ }^{\circ}\text{C}$ , power supplies at nominal voltage.
- Does not include pull-up/pull-down.
- To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

### Programming and Erase Flash Supply Current – HC/HE Devices<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Device	Typ. <sup>5</sup>	Units
$I_{CC}$	Core Power Supply	LCMXO2-256HC	14.6	mA
		LCMXO2-640HC	16.1	mA
		LCMXO2-640UHC	18.8	mA
		LCMXO2-1200HC	18.8	mA
		LCMXO2-1200UHC	22.1	mA
		LCMXO2-2000HC	22.1	mA
		LCMXO2-2000UHC	26.8	mA
		LCMXO2-4000HC	26.8	mA
		LCMXO2-7000HC	33.2	mA
		LCMXO2-2000HE	18.3	mA
		LCMXO2-2000UHE	20.4	mA
		LCMXO2-4000HE	20.4	mA
		LCMXO2-7000HE	23.9	mA
$I_{CCIO}$	Bank Power Supply <sup>6</sup>	All devices	0	mA

- For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).
- Assumes all inputs are held at  $V_{CCIO}$  or GND and all outputs are tri-stated.
- Typical user pattern.
- JTAG programming is at 25 MHz.
- $T_J = 25\text{ }^{\circ}\text{C}$ , power supplies at nominal voltage.
- Per bank.  $V_{CCIO} = 2.5\text{ V}$ . Does not include pull-up/pull-down.

**Programming and Erase Flash Supply Current – ZE Devices<sup>1, 2, 3, 4</sup>**

Symbol	Parameter	Device	Typ. <sup>5</sup>	Units
$I_{CC}$	Core Power Supply	LCMXO2-256ZE	13	mA
		LCMXO2-640ZE	14	mA
		LCMXO2-1200ZE	15	mA
		LCMXO2-2000ZE	17	mA
		LCMXO2-4000ZE	18	mA
		LCMXO2-7000ZE	20	mA
$I_{CCIO}$	Bank Power Supply <sup>6</sup>	All devices	0	mA

1. For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).

2. Assumes all inputs are held at  $V_{CCIO}$  or GND and all outputs are tri-stated.

3. Typical user pattern.

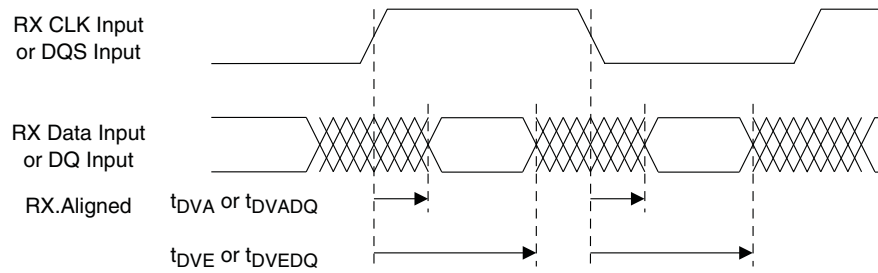
4. JTAG programming is at 25 MHz.

5.  $T_J = 25^\circ\text{C}$ , power supplies at nominal voltage.

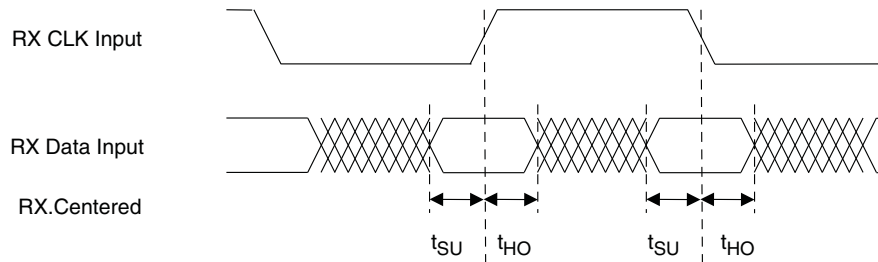
6. Per bank.  $V_{CCIO} = 2.5\text{ V}$ . Does not include pull-up/pull-down.

Parameter	Description	Device	-3		-2		-1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR4_RX.ECLK.Centered <sup>9, 12</sup>									
t <sub>SU</sub>	Input Data Setup Before ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only <sup>11</sup>	0.434	—	0.535	—	0.630	—	ns
t <sub>HO</sub>	Input Data Hold After ECLK		0.385	—	0.395	—	0.463	—	ns
f <sub>DATA</sub>	DDR4 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f <sub>DDR4</sub>	DDR4 ECLK Frequency		—	210	—	176	—	146	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	53	—	44	—	37	MHz
7:1 LVDS Inputs – GDDR71_RX.ECLK.7.1 <sup>9, 12</sup>									
t <sub>DVA</sub>	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only <sup>11</sup>	—	0.307	—	0.316	—	0.326	UI
t <sub>DVE</sub>	Input Data Hold After ECLK		0.662	—	0.650	—	0.649	—	UI
f <sub>DATA</sub>	DDR71 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f <sub>DDR71</sub>	DDR71 ECLK Frequency		—	210	—	176	—	146	MHz
f <sub>CLKIN</sub>	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	60	—	50	—	42	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Aligned <sup>9, 12</sup>									
t <sub>DIA</sub>	Output Data Invalid After CLK Output	All MachXO2 devices, all sides	—	0.850	—	0.910	—	0.970	ns
t <sub>DIB</sub>	Output Data Invalid Before CLK Output		—	0.850	—	0.910	—	0.970	ns
f <sub>DATA</sub>	DDR1 Output Data Speed		—	140	—	116	—	98	Mbps
f <sub>DDR1</sub>	DDR1 SCLK frequency		—	70	—	58	—	49	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Centered <sup>9, 12</sup>									
t <sub>DVB</sub>	Output Data Valid Before CLK Output	All MachXO2 devices, all sides	2.720	—	3.380	—	4.140	—	ns
t <sub>DVA</sub>	Output Data Valid After CLK Output		2.720	—	3.380	—	4.140	—	ns
f <sub>DATA</sub>	DDR1 Output Data Speed		—	140	—	116	—	98	Mbps
f <sub>DDR1</sub>	DDR1 SCLK Frequency (minimum limited by PLL)		—	70	—	58	—	49	MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_TX.ECLK.Aligned <sup>9, 12</sup>									
t <sub>DIA</sub>	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	—	0.270	—	0.300	—	0.330	ns
t <sub>DIB</sub>	Output Data Invalid Before CLK Output		—	0.270	—	0.300	—	0.330	ns
f <sub>DATA</sub>	DDR2 Serial Output Data Speed		—	280	—	234	—	194	Mbps
f <sub>DDR2</sub>	DDR2 ECLK frequency		—	140	—	117	—	97	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	70	—	59	—	49	MHz

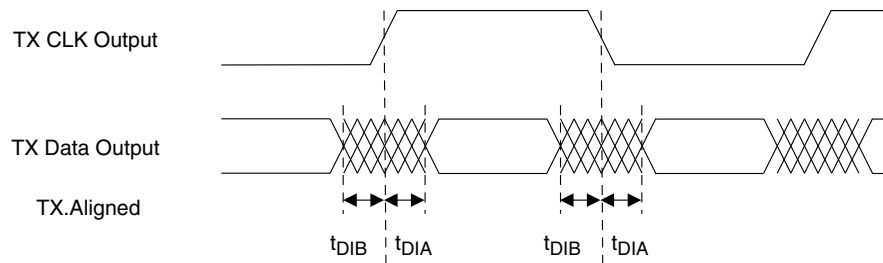
**Figure 3-5. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms**



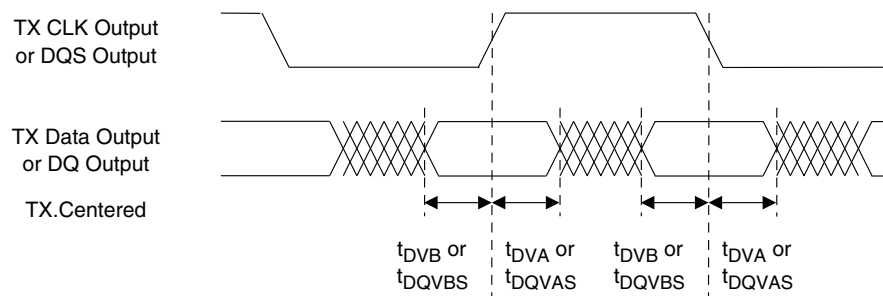
**Figure 3-6. Receiver RX.CLK.Centered Waveforms**



**Figure 3-7. Transmitter TX.CLK.Aligned Waveforms**



**Figure 3-8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms**





## sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Modes					
t <sub>PRGM</sub>	PROGRAMN low pulse accept		55	—	ns
t <sub>PRGMJ</sub>	PROGRAMN low pulse rejection		—	25	ns
t <sub>INITL</sub>	INITN low time	LCMXO2-256	—	30	μs
		LCMXO2-640	—	35	μs
		LCMXO2-640U/ LCMXO2-1200	—	55	μs
		LCMXO2-1200U/ LCMXO2-2000	—	70	μs
		LCMXO2-2000U/ LCMXO2-4000	—	105	μs
		LCMXO2-7000	—	130	μs
t <sub>DPPINIT</sub>	PROGRAMN low to INITN low		—	150	ns
t <sub>DPPDONE</sub>	PROGRAMN low to DONE low		—	150	ns
t <sub>IODISS</sub>	PROGRAMN low to I/O disable		—	120	ns
Slave SPI					
f <sub>MAX</sub>	CCLK clock frequency		—	66	MHz
t <sub>CCLKH</sub>	CCLK clock pulse width high		7.5	—	ns
t <sub>CCLKL</sub>	CCLK clock pulse width low		7.5	—	ns
t <sub>STSU</sub>	CCLK setup time		2	—	ns
t <sub>STH</sub>	CCLK hold time		0	—	ns
t <sub>STCO</sub>	CCLK falling edge to valid output		—	10	ns
t <sub>STOZ</sub>	CCLK falling edge to valid disable		—	10	ns
t <sub>STOV</sub>	CCLK falling edge to valid enable		—	10	ns
t <sub>SCS</sub>	Chip select high time		25	—	ns
t <sub>SCSS</sub>	Chip select setup time		3	—	ns
t <sub>SCSH</sub>	Chip select hold time		3	—	ns
Master SPI					
f <sub>MAX</sub>	MCLK clock frequency		—	133	MHz
t <sub>MCLKH</sub>	MCLK clock pulse width high		3.75	—	ns
t <sub>MCLKL</sub>	MCLK clock pulse width low		3.75	—	ns
t <sub>STSU</sub>	MCLK setup time		5	—	ns
t <sub>STH</sub>	MCLK hold time		1	—	ns
t <sub>CSSPI</sub>	INITN high to chip select low		100	200	ns
t <sub>MCLK</sub>	INITN high to first MCLK edge		0.75	1	μs

	MachXO2-2000						MachXO2-2000U
	49 WLCSP	100 TQFP	132 csBGA	144 TQFP	256 caBGA	256 ftBGA	484 ftBGA
<b>General Purpose I/O per Bank</b>							
Bank 0	19	18	25	27	50	50	70
Bank 1	0	21	26	28	52	52	68
Bank 2	13	20	28	28	52	52	72
Bank 3	0	6	7	8	16	16	24
Bank 4	0	6	8	10	16	16	16
Bank 5	6	8	10	10	20	20	28
Total General Purpose Single-Ended I/O	38	79	104	111	206	206	278
<b>Differential I/O per Bank</b>							
Bank 0	7	9	13	14	25	25	35
Bank 1	0	10	13	14	26	26	34
Bank 2	6	10	14	14	26	26	36
Bank 3	0	3	3	4	8	8	12
Bank 4	0	3	4	5	8	8	8
Bank 5	3	4	5	5	10	10	14
Total General Purpose Differential I/O	16	39	52	56	103	103	139
<b>Dual Function I/O</b>							
	24	31	33	33	33	33	37
<b>High-speed Differential I/O</b>							
Bank 0	5	4	8	9	14	14	18
<b>Gearboxes</b>							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	4	8	9	14	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	10	14	14	14	14	18
<b>DQS Groups</b>							
Bank 1	0	1	2	2	2	2	2
<b>VCCIO Pins</b>							
Bank 0	2	2	3	3	4	4	10
Bank 1	0	2	3	3	4	4	10
Bank 2	1	2	3	3	4	4	10
Bank 3	0	1	1	1	1	1	3
Bank 4	0	1	1	1	2	2	4
Bank 5	1	1	1	1	1	1	3
VCC	2	2	4	4	8	8	12
GND	4	8	10	12	24	24	48
NC	0	1	1	4	1	1	105
Reserved for Configuration	1	1	1	1	v	1	1
Total Count of Bonded Pins	39	100	132	144	256	256	484

	MachXO2-4000							
	84 QFN	132 csBGA	144 TQFP	184 csBGA	256 caBGA	256 ftBGA	332 caBGA	484 fpBGA
<b>General Purpose I/O per Bank</b>								
Bank 0	27	25	27	37	50	50	68	70
Bank 1	10	26	29	37	52	52	68	68
Bank 2	22	28	29	39	52	52	70	72
Bank 3	0	7	9	10	16	16	24	24
Bank 4	9	8	10	12	16	16	16	16
Bank 5	0	10	10	15	20	20	28	28
Total General Purpose Single Ended I/O	68	104	114	150	206	206	274	278
<b>Differential I/O per Bank</b>								
Bank 0	13	13	14	18	25	25	34	35
Bank 1	4	13	14	18	26	26	34	34
Bank 2	11	14	14	19	26	26	35	36
Bank 3	0	3	4	4	8	8	12	12
Bank 4	4	4	5	6	8	8	8	8
Bank 5	0	5	5	7	10	10	14	14
Total General Purpose Differential I/O	32	52	56	72	103	103	137	139
<b>Dual Function I/O</b>								
	28	37	37	37	37	37	37	37
<b>High-speed Differential I/O</b>								
Bank 0	8	8	9	8	18	18	18	18
<b>Gearboxes</b>								
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	8	8	9	9	18	18	18	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	11	14	14	12	18	18	18	18
<b>DQS Groups</b>								
Bank 1	1	2	2	2	2	2	2	2
<b>VCCIO Pins</b>								
Bank 0	3	3	3	3	4	4	4	10
Bank 1	1	3	3	3	4	4	4	10
Bank 2	2	3	3	3	4	4	4	10
Bank 3	1	1	1	1	1	1	2	3
Bank 4	1	1	1	1	2	2	1	4
Bank 5	1	1	1	1	1	1	2	3
<b>VCC</b>								
	4	4	4	4	8	8	8	12
<b>GND</b>								
	4	10	12	16	24	24	27	48
<b>NC</b>								
	1	1	1	1	1	1	5	105
<b>Reserved for configuration</b>								
	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	84	132	144	184	256	256	332	484

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100IR1 <sup>1</sup>	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100IR1 <sup>1</sup>	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100IR1 <sup>1</sup>	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132IR1 <sup>1</sup>	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132IR1 <sup>1</sup>	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132IR1 <sup>1</sup>	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144IR1 <sup>1</sup>	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144IR1 <sup>1</sup>	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144IR1 <sup>1</sup>	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200ZE-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

Date	Version	Section	Change Summary
May 2011	01.3	Multiple	Replaced “SED” with “SRAM CRC Error Detection” throughout the document.
		DC and Switching Characteristics	Added footnote 1 to Program Erase Specifications table.
		Pinout Information	Updated Pin Information Summary tables.
			Signal name SO/SISPISO changed to SO/SPISO in the Signal Descriptions table.
April 2011	01.2	—	Data sheet status changed from Advance to Preliminary.
		Introduction	Updated MachXO2 Family Selection Guide table.
		Architecture	Updated Supported Input Standards table.
			Updated sysMEM Memory Primitives diagram.
			Added differential SSTL and HSTL IO standards.
		DC and Switching Characteristics	Updates following parameters: POR voltage levels, DC electrical characteristics, static supply current for ZE/HE/HC devices, static power consumption contribution of different components – ZE devices, programming and erase Flash supply current.
			Added VREF specifications to sysIO recommended operating conditions.
			Updating timing information based on characterization.
			Added differential SSTL and HSTL IO standards.
		Ordering Information	Added Ordering Part Numbers for R1 devices, and devices in WLCSP packages.
			Added R1 device specifications.
January 2011	01.1	All	Included ultra-high I/O devices.
		DC and Switching Characteristics	Recommended Operating Conditions table – Added footnote 3.
			DC Electrical Characteristics table – Updated data for $I_{IL}$ , $I_{IH}$ , $V_{HYST}$ typical values updated.
			Generic DDRX2 Outputs with Clock and Data Aligned at Pin (GDDR2_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for $T_{DIA}$ and $T_{DIB}$ .
			Generic DDRX4 Outputs with Clock and Data Aligned at Pin (GDDR4_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for $T_{DIA}$ and $T_{DIB}$ .
			Power-On-Reset Voltage Levels table - clarified note 3.
			Clarified VCCIO related recommended operating conditions specifications.
			Added power supply ramp rate requirements.
			Added Power Supply Ramp Rates table.
			Updated Programming/Erase Specifications table.
			Removed references to $V_{CCP}$ .
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Removed references to $V_{CCP}$ .
November 2010	01.0	—	Initial release.