E.) Featrice Semiconductor Corporation - <u>LCMXO2-640HC-5TG100C Datasheet</u>



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	18432
Number of I/O	78
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-640hc-5tg100c

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MachXO2 Family Data Sheet Introduction

May 2016

Features

- Flexible Logic Architecture
 - Six devices with 256 to 6864 LUT4s and 18 to 334 I/Os
- Ultra Low Power Devices
 - Advanced 65 nm low power process
 - As low as 22 μ W standby power
 - Programmable low swing differential I/Os
 - · Stand-by mode and other power saving options

Embedded and Distributed Memory

- Up to 240 kbits sysMEM™ Embedded Block RAM
- Up to 54 kbits Distributed RAM
- Dedicated FIFO control logic
- On-Chip User Flash Memory
 - Up to 256 kbits of User Flash Memory
 - 100,000 write cycles
 - Accessible through WISHBONE, SPI, I²C and JTAG interfaces
 - Can be used as soft processor PROM or as Flash memory

Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/Os
- Generic DDR, DDRX2, DDRX4
- Dedicated DDR/DDR2/LPDDR memory with DQS support

■ High Performance, Flexible I/O Buffer

- Programmable sysIO[™] buffer supports wide range of interfaces:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2
 - LVTTL
 - PCI
 - LVDS, Bus-LVDS, MLVDS, RSDS, LVPECL
 - SSTL 25/18
 - HSTL 18
 - Schmitt trigger inputs, up to 0.5 V hysteresis
- I/Os support hot socketing
- On-chip differential termination
- · Programmable pull-up or pull-down mode

- Flexible On-Chip Clocking
 - · Eight primary clocks
 - Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
 - Up to two analog PLLs per device with fractional-n frequency synthesis
 - Wide input frequency range (7 MHz to 400 MHz)

Data Sheet DS1035

- Non-volatile, Infinitely Reconfigurable
 - Instant-on powers up in microseconds
 - Single-chip, secure solution
 - Programmable through JTAG, SPI or I²C
 - Supports background programming of non-volatile memory
 - Optional dual boot with external SPI memory
- TransFR[™] Reconfiguration
 - In-field logic update while system operates

Enhanced System Level Support

- On-chip hardened functions: SPI, I²C, timer/ counter
- On-chip oscillator with 5.5% accuracy
- Unique TraceID for system tracking
- One Time Programmable (OTP) mode
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming
- Broad Range of Package Options
 - TQFP, WLCSP, ucBGA, csBGA, caBGA, ftBGA, fpBGA, QFN package options
 - Small footprint package options
 As small as 2.5 mm x 2.5 mm
 - · Density migration supported
 - · Advanced halogen-free packaging



ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

Routing

There are many resources provided in the MachXO2 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Each MachXO2 device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO2 architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO2-640U, MachXO2-1200/U and higher density devices have two edge clocks each on the top and bottom edges. Lower density devices have no edge clocks. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO2 devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO2 External Switching Characteristics table.

The primary clock signals for the MachXO2-256 and MachXO2-640 are generated from eight 17:1 muxes The available clock sources include eight I/O sources and 9 routing inputs. Primary clock signals for the MachXO2-640U, MachXO2-1200/U and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.



Figure 2-17. Output Gearbox



More information on the output gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.



Figure 2-20. Embedded Function Block Interface



Hardened I²C IP Core

Every MachXO2 device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I^2C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I^2C Master. The I^2C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface



Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
 - Watchdog timer
 - Clear timer on compare match
 - Fast PWM
 - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- · Stand-alone mode with preloaded control registers and direct reset input

Figure 2-23. Timer/Counter Block Diagram



Table 2-17. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	0	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	0	Timer counter output signal



Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I²C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

- 1. Internal Flash Download
- 2. JTAG
- 3. Standard Serial Peripheral Interface (Master SPI mode) interface to boot PROM memory
- 4. System microprocessor to drive a serial slave SPI port (SSPI mode)
- 5. Standard I²C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, MachXO2 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.



When implementing background programming of the on-chip Flash, care must be taken for the operation of the PLL. For devices that have two PLLs (XO2-2000U, -4000 and -7000), the system must put the RPLL (Right-side PLL) in reset state during the background Flash programming. More detailed description can be found in TN1204, MachXO2 Programming and Configuration Usage Guide.

Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO2 devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile Flash memory spaces. The device can be in one of two modes:

- 1. Unlocked Readback of the SRAM configuration and non-volatile Flash memory spaces is allowed.
- 2. Permanently Locked The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Dual Boot

MachXO2 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the on-chip Flash. The golden image MUST reside in an external SPI Flash. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1206, MachXO2 Soft Error Detection Usage Guide.

TraceID

Each MachXO2 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I²C, or JTAG interfaces.

Density Shifting

The MachXO2 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO2 migration files.



Power-On-Reset Voltage Levels^{1, 2, 3, 4, 5}

Symbol	Parameter	Min.	Тур.	Max.	Units
V _{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and $V_{CCIO0})$	0.9	_	1.06	V
V _{PORUPEXT}	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	_	2.1	V
V _{PORDNBG}	Power-On-Reset ramp down trip point (band gap based circuit monitoring $V_{CCINT})$	0.75	_	0.93	V
V _{PORDNBGEXT}	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	_	1.33	V
V _{PORDNSRAM}	Power-On-Reset ramp down trip point (SRAM based circuit monitoring $V_{\mbox{CCINT}}$)	-	0.6	_	V
V _{PORDNSRAMEXT}	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	_	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.

3. Note that V_{PORUP} (min.) and V_{PORDNBG} (max.) are in different process corners. For any given process corner V_{PORDNBG} (max.) is always 12.0 mV below V_{PORUP} (min.).

4. V_{PORUPEXT} is for HC devices only. In these devices a separate POR circuit monitors the external V_{CC} power supply.

5. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

Programming/Erase Specifications

Symbol	Parameter	Min.	Max. ¹	Units	
N	Flash Programming cycles per t _{RETENTION}	—	10,000	Cycles	
PROGCYC	Flash functional programming cycles	—	100,000	Oycles	
t _{RETENTION}	Data retention at 100 °C junction temperature	10	—	Vears	
	Data retention at 85 °C junction temperature	20	—	leais	

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

Hot Socketing Specifications^{1, 2, 3}

I_{DK} Input or I/O leakage Current $0 < V_{IN} < V_{IH}$ (MAX) +/-1000 μ A	Symbol	Parameter	Condition	Max.	Units
	I _{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/-1000	μΑ

1. Insensitive to sequence of V_{CC} and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO} .

2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).

3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

ESD Performance

Please refer to the MachXO2 Product Family Qualification Summary for complete qualification data, including ESD performance.



RSDS

The MachXO2 family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.



Figure 3-4. RSDS (Reduced Swing Differential Standard)

Table 3-4. RSDS DC Conditions

Parameter Description		Typical	Units
Z _{OUT}	Output impedance	20	Ohms
R _S	Driver series resistor	294	Ohms
R _P	Driver parallel resistor	121	Ohms
R _T	T Receiver termination		Ohms
V _{OH}	Output high voltage	1.35	V
V _{OL}	Output low voltage	1.15	V
V _{OD}	Output differential voltage	0.20	V
V _{CM}	CM Output common mode voltage		V
Z _{BACK}	Back impedance 101.5		Ohms
I _{DC}	DC output current	3.66	mA





			_	6	_	5	_	4	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
		MachXO2-256HC-HE	1.42	_	1.59	_	1.96	_	ns
		MachXO2-640HC-HE	1.41	_	1.58	_	1.96	_	ns
	Clock to Data Setup – PIO	MachXO2-1200HC-HE	1.63	_	1.79	_	2.17	_	ns
^I SU_DEL	Delav	MachXO2-2000HC-HE	1.61	_	1.76	_	2.13	_	ns
		MachXO2-4000HC-HE	1.66	_	1.81	_	2.19	_	ns
		MachXO2-7000HC-HE	1.53	_	1.67		2.03		ns
		MachXO2-256HC-HE	-0.24	_	-0.24		-0.24		ns
		MachXO2-640HC-HE	-0.23	_	-0.23	_	-0.23	_	ns
+	Clock to Data Hold – PIO Input	MachXO2-1200HC-HE	-0.24	_	-0.24	_	-0.24	_	ns
'H_DEL	Register with Input Data Delay	MachXO2-2000HC-HE	-0.23	_	-0.23		-0.23		ns
		MachXO2-4000HC-HE	-0.25	_	-0.25		-0.25		ns
		MachXO2-7000HC-HE	-0.21		-0.21		-0.21		ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices		388	_	323	_	269	MHz
General I/O	Pin Parameters (Using Edge C	lock without PLL)							
		MachXO2-1200HC-HE	_	7.53		7.76		8.10	ns
+	Clock to Output – PIO Output	MachXO2-2000HC-HE		7.53		7.76		8.10	ns
COE	Register	MachXO2-4000HC-HE		7.45		7.68		8.00	ns
		MachXO2-7000HC-HE		7.53		7.76		8.10	ns
		MachXO2-1200HC-HE	-0.19	_	-0.19	_	-0.19	_	ns
	Clock to Data Setup – PIO Input Register	MachXO2-2000HC-HE	-0.19	_	-0.19	_	-0.19	_	ns
ISUE		MachXO2-4000HC-HE	-0.16	_	-0.16	_	-0.16	_	ns
		MachXO2-7000HC-HE	-0.19	_	-0.19		-0.19		ns
		MachXO2-1200HC-HE	1.97	_	2.24	_	2.52	_	ns
	Clock to Data Hold – PIO Input	MachXO2-2000HC-HE	1.97	_	2.24	_	2.52	_	ns
ΉE	Register	MachXO2-4000HC-HE	1.89	_	2.16	_	2.43		ns
		MachXO2-7000HC-HE	1.97	_	2.24	_	2.52	_	ns
		MachXO2-1200HC-HE	1.56	_	1.69	_	2.05	_	ns
	Clock to Data Setup – PIO	MachXO2-2000HC-HE	1.56	_	1.69	_	2.05	_	ns
^I SU_DELE	Delay	MachXO2-4000HC-HE	1.74	_	1.88	_	2.25	_	ns
		MachXO2-7000HC-HE	1.66	_	1.81	_	2.17		ns
		MachXO2-1200HC-HE	-0.23	_	-0.23	_	-0.23	_	ns
+	Clock to Data Hold – PIO Input	MachXO2-2000HC-HE	-0.23	_	-0.23		-0.23		ns
'H_DELE	Register with Input Data Delay	MachXO2-4000HC-HE	-0.34	_	-0.34		-0.34		ns
		MachXO2-7000HC-HE	-0.29	_	-0.29		-0.29		ns
General I/O	Pin Parameters (Using Primary	y Clock with PLL)							
t _{COPLL}		MachXO2-1200HC-HE	—	5.97		6.00		6.13	ns
	Clock to Output – PIO Output	MachXO2-2000HC-HE		5.98		6.01		6.14	ns
	Register	MachXO2-4000HC-HE		5.99		6.02		6.16	ns
		MachXO2-7000HC-HE		6.02		6.06		6.20	ns
		MachXO2-1200HC-HE	0.36	—	0.36	—	0.65	—	ns
+.	Clock to Data Setup – PIO	MachXO2-2000HC-HE	0.36	—	0.36	—	0.63	—	ns
SUPLL	Input Register	MachXO2-4000HC-HE	0.35	—	0.35	—	0.62	—	ns
		MachXO2-7000HC-HE	0.34	—	0.34	—	0.59	—	ns
	1	•			•		•		



			-	-3	-	-2	-	1	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
		MachXO2-1200ZE	0.66	—	0.68		0.80		ns
, o	Clock to Data Hold – PIO Input Register	MachXO2-2000ZE	0.68	—	0.70		0.83		ns
^I HPLL		MachXO2-4000ZE	0.68	—	0.71		0.84		ns
	MachXO2-7000ZE	0.73	—	0.74	—	0.87	—	ns	
		MachXO2-1200ZE	5.14	—	5.69	—	6.20	—	ns
	Clock to Data Setup – PIO	MachXO2-2000ZE	5.11	—	5.67	—	6.17	—	ns
^I SU_DELPLL	Delav	MachXO2-4000ZE	5.27	—	5.84		6.35	—	ns
	Delay	MachXO2-7000ZE	5.15	—	5.71	—	6.23	—	ns
		MachXO2-1200ZE	-1.36	—	-1.36	—	-1.36	—	ns
	Clock to Data Hold – PIO Input	MachXO2-2000ZE	-1.35	—	-1.35		-1.35	—	ns
^I H_DELPLL	Register with Input Data Delay	MachXO2-4000ZE	-1.43	—	-1.43	—	-1.43	—	ns
		MachXO2-7000ZE	-1.41	—	-1.41	—	-1.41	—	ns
Generic DDR	X1 Inputs with Clock and Data A	ligned at Pin Using PO	CLK Pin	for Cloc	k Input -	GDDR	(1_RX.S	CLK.Ali	gned ^{9, 12}
t _{DVA}	Input Data Valid After CLK		_	0.382		0.401		0.417	UI
t _{DVE}	Input Data Hold After CLK	All MachXO2	0.670	—	0.684		0.693	—	UI
f _{DATA}	DDRX1 Input Data Speed	devices, all sides	_	140		116	—	98	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency		_	70		58	—	49	MHz
Generic DDR	X1 Inputs with Clock and Data Ce	entered at Pin Using PC	LK Pin f	for Clock	Input –	GDDRX	1_RX.SC	LK.Cen	tered ^{9, 12}
t _{SU}	Input Data Setup Before CLK		1.319	—	1.412		1.462	—	ns
t _{HO}	Input Data Hold After CLK	All MachXO2	0.717	—	1.010	—	1.340	—	ns
f _{DATA}	DDRX1 Input Data Speed	devices, all sides	—	140	—	116	—	98	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDR	X2 Inputs with Clock and Data A	ligned at Pin Using PO	CLK Pin	for Cloc	k Input -	GDDR)	(2_RX.E	CLK.Ali	gned ^{9, 12}
t _{DVA}	Input Data Valid After CLK		_	0.361		0.346	_	0.334	UI
t _{DVE}	Input Data Hold After CLK	MachXO2-640U,	0.602	—	0.625		0.648	—	UI
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO2-1200/U and larger devices,	—	280	—	234	—	194	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency	bottom side only ¹¹		140	—	117		97	MHz
f _{SCLK}	SCLK Frequency			70		59		49	MHz
Generic DDR	X2 Inputs with Clock and Data Ce	entered at Pin Using PC	LK Pin f	for Clock	Input –	GDDRX	2_RX.EC	LK.Cen	tered ^{9, 12}
t _{SU}	Input Data Setup Before CLK		0.472	—	0.672		0.865		ns
t _{HO}	Input Data Hold After CLK	MachXO2-640U,	0.363	—	0.501	—	0.743	—	ns
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	280	_	234	_	194	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency	bottom side only"		140	—	117		97	MHz
f _{SCLK}	SCLK Frequency			70		59		49	MHz
Generic DDR	4 Inputs with Clock and Data A	ligned at Pin Using PC	LK Pin	for Cloc	k Input -	GDDRX	4_RX.E	CLK.Ali	gned ^{9, 12}
t _{DVA}	Input Data Valid After ECLK		—	0.307		0.316		0.326	UI
t _{DVE}	Input Data Hold After ECLK	MachXO2-640U.	0.662	—	0.650		0.649	—	UI
f _{DATA}	DDRX4 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	420	_	352	_	292	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency	bottom side only ¹¹	—	210	—	176	—	146	MHz
f _{SCLK}	SCLK Frequency	1	—	53	—	44	—	37	MHz



Figure 3-9. GDDR71 Video Timing Waveforms



Figure 3-10. Receiver GDDR71_RX. Waveforms



Figure 3-11. Transmitter GDDR71_TX. Waveforms





MachXO2 Oscillator Output Frequency

Symbol	Parameter	Min.	Тур.	Max	Units
f _{MAX}	Oscillator Output Frequency (Commercial Grade Devices, 0 to 85°C)	125.685	133	140.315	MHz
	Oscillator Output Frequency (Industrial Grade Devices, -40 °C to 100 °C)	124.355	133	141.645	MHz
t _{DT}	Output Clock Duty Cycle	43	50	57	%
t _{OPJIT} 1	Output Clock Period Jitter	0.01	0.012	0.02	UIPP
t _{STABLEOSC}	STDBY Low to Oscillator Stable	0.01	0.05	0.1	μs

1. Output Clock Period Jitter specified at 133 MHz. The values for lower frequencies will be smaller UIPP. The typical value for 133 MHz is 95 ps and for 2.08 MHz the typical value is 1.54 ns.

MachXO2 Standby Mode Timing – HC/HE Devices

Symbol	Parameter	Device	Min.	Тур.	Max	Units
t _{PWRDN}	USERSTDBY High to Stop	All	_	—	9	ns
Symbol t _{PWRDN}		LCMXO2-256		—		μs
		LCMXO2-640		—		μs
t _{PWRUP}	USERSTDBY Low to Power Up	LCMXO2-640U		—		μs
		LCMXO2-1200	20	—	50	μs
		LCMXO2-1200U		—		μs
		LCMXO2-2000		—		μs
		LCMXO2-2000U		—		μs
		LCMXO2-4000		—		μs
		LCMXO2-7000		—		μs
t _{WSTDBY}	USERSTDBY Pulse Width	All	18	_	—	ns



MachXO2 Standby Mode Timing – ZE Devices

Symbol	Parameter	Device	Min.	Тур.	Max	Units
t _{PWRDN}	USERSTDBY High to Stop	All	_		13	ns
Symbol t _{PWRDN} t _{PWRUP}	USERSTDBY Low to Power Up	LCMXO2-256		_		μs
		LCMXO2-640		_		μs
		LCMXO2-1200	20	_	50	μs
PWRUP		LCMXO2-2000		_		μs
		arameter Device Min. Typ. Max to Stop All — — 13 LCMXO2-256 — — 12 LCMXO2-640 — — 12 LCMXO2-1200 20 — 50 LCMXO2-2000 — — 12 LCMXO2-2000 — — 12 LCMXO2-4000 — — 12 LCMXO2-7000 — — 12 width All 19 — — noto Bandgap Stable All — — 15	μs			
		LCMXO2-7000		_		μs
t _{WSTDBY}	USERSTDBY Pulse Width	All	19	_	_	ns
t _{BNDGAPSTBL}	USERSTDBY High to Bandgap Stable	All			15	ns



I²C Port Timing Specifications^{1, 2}

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCL clock frequency	—	400	kHz

1. MachXO2 supports the following modes:

• Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)

• Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)

2. Refer to the I²C specification for timing requirements.

SPI Port Timing Specifications¹

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCK clock frequency		45	MHz

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

Switching Test Conditions

Figure 3-13 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-5.

Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards



Table 3-5. Test Fixture Required Components	, Non-Terminated Interfaces
---	-----------------------------

Test Condition	R1	CL	Timing Ref.	VT
			LVTTL, LVCMOS 3.3 = 1.5 V	_
			LVCMOS 2.5 = $V_{CCIO}/2$	_
LVTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVCMOS 1.8 = $V_{CCIO}/2$	
			LVCMOS 1.5 = $V_{CCIO}/2$	_
			LVCMOS 1.2 = $V_{CCIO}/2$	_
LVTTL and LVCMOS 3.3 (Z -> H)			1.5 V	V _{OL}
LVTTL and LVCMOS 3.3 (Z -> L)	100		1.5 V	V _{OH}
Other LVCMOS (Z -> H)		0.5	V _{CCIO} /2	V _{OL}
Other LVCMOS (Z -> L)	100	opr	V _{CCIO} /2	V _{OH}
LVTTL + LVCMOS (H -> Z)			V _{OH} – 0.15 V	V _{OL}
LVTTL + LVCMOS (L -> Z)			V _{OL} – 0.15 V	V _{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.



	MachXO2-2000						MachXO2-2000U
	49 WLCSP	100 TQFP	132 csBGA	144 TQFP	256 caBGA	256 ftBGA	484 ftBGA
General Purpose I/O per Bank			1				
Bank 0	19	18	25	27	50	50	70
Bank 1	0	21	26	28	52	52	68
Bank 2	13	20	28	28	52	52	72
Bank 3	0	6	7	8	16	16	24
Bank 4	0	6	8	10	16	16	16
Bank 5	6	8	10	10	20	20	28
Total General Purpose Single-Ended I/O	38	79	104	111	206	206	278
Differential I/O per Bank							
Bank 0	7	9	13	14	25	25	35
Bank 1	0	10	13	14	26	26	34
Bank 2	6	10	14	14	26	26	36
Bank 3	0	3	3	4	8	8	12
Bank 4	0	3	4	5	8	8	8
Bank 5	3	4	5	5	10	10	14
Total General Purpose Differential I/O	16	39	52	56	103	103	139
	-		_				
Dual Function I/O	24	31	33	33	33	33	37
High-speed Differential I/O	•	•	•			•	
Bank 0	5	4	8	9	14	14	18
Gearboxes						•	
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	4	8	9	14	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	10	14	14	14	14	18
DQS Groups			1				
Bank 1	0	1	2	2	2	2	2
VCCIO Pins							
Bank 0	2	2	3	3	4	4	10
Bank 1	0	2	3	3	4	4	10
Bank 2	1	2	3	3	4	4	10
Bank 3	0	1	1	1	1	1	3
Bank 4	0	1	1	1	2	2	4
Bank 5	1	1	1	1	1	1	3
VCC	2	2	4	4	8	8	12
GND	4	8	10	12	24	24	48
NC	0	1	1	4	1	1	105
Reserved for Configuration	1	1	1	1	v	1	1
Total Count of Bonded Pins	39	100	132	144	256	256	484



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144C	6864	1.2 V	-1	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-2TG144C	6864	1.2 V	-2	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-3TG144C	6864	1.2 V	-3	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-1BG256C	6864	1.2 V	-1	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-2BG256C	6864	1.2 V	-2	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-3BG256C	6864	1.2 V	-3	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-1FTG256C	6864	1.2 V	-1	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-2FTG256C	6864	1.2 V	-2	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-3FTG256C	6864	1.2 V	-3	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-1BG332C	6864	1.2 V	-1	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-2BG332C	6864	1.2 V	-2	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-3BG332C	6864	1.2 V	-3	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-1FG484C	6864	1.2 V	-1	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-2FG484C	6864	1.2 V	-2	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-3FG484C	6864	1.2 V	-3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100CR11	1280	1.2 V	-1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100CR11	1280	1.2 V	-2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100CR11	1280	1.2 V	-3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132CR1 ¹	1280	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132CR11	1280	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132CR1 ¹	1280	1.2 V	-3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144CR1 ¹	1280	1.2 V	-1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144CR1 ¹	1280	1.2 V	-2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144CR1 ¹	1280	1.2 V	-3	Halogen-Free TQFP	144	COM

1. Specifications for the "LCMXO2-1200ZE-speed package CR1" are the same as the "LCMXO2-1200ZE-speed package C" devices respectively, except as specified in the R1 Device Specifications section of this data sheet.



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484C	2112	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-5FG484C	2112	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-6FG484C	2112	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84C	4320	2.5 V / 3.3 V	-4	Halogen-Free QFN	84	COM
LCMXO2-4000HC-5QN84C	4320	2.5 V / 3.3 V	-5	Halogen-Free QFN	84	COM
LCMXO2-4000HC-6QN84C	4320	2.5 V / 3.3 V	-6	Halogen-Free QFN	84	COM
LCMXO2-4000HC-4MG132C	4320	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-5MG132C	4320	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-6MG132C	4320	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-4TG144C	4320	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-5TG144C	4320	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-6TG144C	4320	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-4BG256C	4320	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-5BG256C	4320	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-6BG256C	4320	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-4FTG256C	4320	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-5FTG256C	4320	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-6FTG256C	4320	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-4BG332C	4320	2.5 V / 3.3 V	-4	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-5BG332C	4320	2.5 V / 3.3 V	-5	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-6BG332C	4320	2.5 V / 3.3 V	-6	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-4FG484C	4320	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-5FG484C	4320	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-6FG484C	4320	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	COM



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100IR11	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100IR11	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100IR11	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132IR11	1280	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132IR1 ¹	1280	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132IR11	1280	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144IR1 ¹	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144IR1 ¹	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144IR11	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND

1. Specifications for the "LCMXO2-1200HC-speed package IR1" are the same as the "LCMXO2-1200ZE-speed package I" devices respectively, except as specified in the R1 Device Specifications section of this data sheet.



MachXO2 Family Data Sheet Supplemental Information

April 2012

Data Sheet DS1035

For Further Information

A variety of technical notes for the MachXO2 family are available on the Lattice web site.

- TN1198, Power Estimation and Management for MachXO2 Devices
- TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide
- TN1201, Memory Usage Guide for MachXO2 Devices
- TN1202, MachXO2 sysIO Usage Guide
- TN1203, Implementing High-Speed Interfaces with MachXO2 Devices
- TN1204, MachXO2 Programming and Configuration Usage Guide
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices
- TN1206, MachXO2 SRAM CRC Error Detection Usage Guide
- TN1207, Using TraceID in MachXO2 Devices
- TN1074, PCB Layout Recommendations for BGA Packages
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices
- AN8066, Boundary Scan Testability with Lattice sysIO Capability
- MachXO2 Device Pinout Files
- Thermal Management document
- · Lattice design tools

For further information on interface standards, refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, LVDS, DDR, DDR2, LPDDR): www.jedec.org
- PCI: www.pcisig.com

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Date	Version	Section	Change Summary
May 2011	01.3	Multiple	Replaced "SED" with "SRAM CRC Error Detection" throughout the document.
		DC and Switching Characteristics	Added footnote 1 to Program Erase Specifications table.
		Pinout Information	Updated Pin Information Summary tables.
			Signal name SO/SISPISO changed to SO/SPISO in the Signal Descriptions table.
April 2011	01.2	—	Data sheet status changed from Advance to Preliminary.
		Introduction	Updated MachXO2 Family Selection Guide table.
		Architecture	Updated Supported Input Standards table.
			Updated sysMEM Memory Primitives diagram.
			Added differential SSTL and HSTL IO standards.
		DC and Switching Characteristics	Updates following parameters: POR voltage levels, DC electrical characteristics, static supply current for ZE/HE/HC devices, static power consumption contribution of different components – ZE devices, programming and erase Flash supply current.
			Added VREF specifications to sysIO recommended operating condi- tions.
			Updating timing information based on characterization.
			Added differential SSTL and HSTL IO standards.
		Ordering Information	Added Ordering Part Numbers for R1 devices, and devices in WLCSP packages.
			Added R1 device specifications.
January 2011	01.1	All	Included ultra-high I/O devices.
		DC and Switching Characteristics	Recommended Operating Conditions table – Added footnote 3.
			DC Electrical Characteristics table – Updated data for $\rm I_{IL}, I_{IH}, V_{HYST}$ typical values updated.
			Generic DDRX2 Outputs with Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB} .
			Generic DDRX4 Outputs with Clock and Data Aligned at Pin (GDDRX4_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T _{DIA} and T _{DIB.}
			Power-On-Reset Voltage Levels table - clarified note 3.
			Clarified VCCIO related recommended operating conditions specifications.
			Added power supply ramp rate requirements.
			Added Power Supply Ramp Rates table.
			Updated Programming/Erase Specifications table.
			Removed references to V _{CCP.}
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Removed references to V _{CCP.}
November 2010	01.0	_	Initial release.