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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	18432
Number of I/O	79
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-640ze-1mg132c

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MachXO2 Family Data Sheet Introduction

May 2016

Features

- Flexible Logic Architecture
 - Six devices with 256 to 6864 LUT4s and 18 to 334 I/Os
- Ultra Low Power Devices
 - Advanced 65 nm low power process
 - As low as 22 μ W standby power
 - Programmable low swing differential I/Os
 - · Stand-by mode and other power saving options

Embedded and Distributed Memory

- Up to 240 kbits sysMEM™ Embedded Block RAM
- Up to 54 kbits Distributed RAM
- Dedicated FIFO control logic
- On-Chip User Flash Memory
 - Up to 256 kbits of User Flash Memory
 - 100,000 write cycles
 - Accessible through WISHBONE, SPI, I²C and JTAG interfaces
 - Can be used as soft processor PROM or as Flash memory

Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/Os
- Generic DDR, DDRX2, DDRX4
- Dedicated DDR/DDR2/LPDDR memory with DQS support

■ High Performance, Flexible I/O Buffer

- Programmable sysIO[™] buffer supports wide range of interfaces:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2
 - LVTTL
 - PCI
 - LVDS, Bus-LVDS, MLVDS, RSDS, LVPECL
 - SSTL 25/18
 - HSTL 18
 - Schmitt trigger inputs, up to 0.5 V hysteresis
- I/Os support hot socketing
- On-chip differential termination
- · Programmable pull-up or pull-down mode

- Flexible On-Chip Clocking
 - · Eight primary clocks
 - Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
 - Up to two analog PLLs per device with fractional-n frequency synthesis
 - Wide input frequency range (7 MHz to 400 MHz)

Data Sheet DS1035

- Non-volatile, Infinitely Reconfigurable
 - Instant-on powers up in microseconds
 - Single-chip, secure solution
 - Programmable through JTAG, SPI or I²C
 - Supports background programming of non-volatile memory
 - Optional dual boot with external SPI memory
- TransFR[™] Reconfiguration
 - In-field logic update while system operates

Enhanced System Level Support

- On-chip hardened functions: SPI, I²C, timer/ counter
- On-chip oscillator with 5.5% accuracy
- Unique TraceID for system tracking
- One Time Programmable (OTP) mode
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming
- Broad Range of Package Options
 - TQFP, WLCSP, ucBGA, csBGA, caBGA, ftBGA, fpBGA, QFN package options
 - Small footprint package options
 As small as 2.5 mm x 2.5 mm
 - · Density migration supported
 - · Advanced halogen-free packaging



Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), preengineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I²C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external V_{CC} supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V_{CC} supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pulldown and bus-keeper features are controllable on a "per-pin" basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I²C port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE[™] modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.



The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag "hard" control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysl/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2-640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO2 devices provide commonly used hardened functions such as SPI controller, I²C controller and timer/ counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I²C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

PFU Blocks

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.



Figure 2-5. Primary Clocks for MachXO2 Devices



Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO2 External Switching Characteristics table.







Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

The tri-state register blocks on the right edge contain an additional register for DDR memory operation. In DDR memory mode, the register TS input is fed into another register that is clocked using the DQSW90 signal. The output of this register is used as a tri-state control.

Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

Table 2-9.	Input	Gearbox	Sianal List
14010 2 01	mpat	acaison	orginal Eloc

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3



Hot Socketing

The MachXO2 devices have been carefully designed to ensure predictable behavior during power-up and powerdown. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO2 ideal for many multiple power supply and hot-swap applications.

On-chip Oscillator

Every MachXO2 device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

- 1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
- 2. During configuration, users select a different master clock frequency.
- 3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
- 4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-14 lists all the available MCLK frequencies.

Table 2-14. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

Embedded Hardened IP Functions and User Flash Memory

All MachXO2 devices provide embedded hardened functions such as SPI, I²C and Timer/Counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2-20.



BLVDS

The MachXO2 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example



Table 3-2. BLVDS DC Conditions¹

Over Recommended	Operating	Conditions
	operating	oonantions

		Noi	ninal	
Symbol	Description	Zo = 45	Zo = 90	Units
Z _{OUT}	Output impedance	20	20	Ohms
R _S	Driver series resistance	80	80	Ohms
R _{TLEFT}	Left end termination	45	90	Ohms
R _{TRIGHT}	Right end termination	45	90	Ohms
V _{OH}	Output high voltage	1.376	1.480	V
V _{OL}	Output low voltage	1.124	1.020	V
V _{OD}	Output differential voltage	0.253	0.459	V
V _{CM}	Output common mode voltage	1.250	1.250	V
I _{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.



Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
LVDS25	400	MHz
LVDS25E	150	MHz
RSDS25	150	MHz
RSDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
SSTL25_I	150	MHz
SSTL25_II	150	MHz
SSTL25D_I	150	MHz
SSTL25D_II	150	MHz
SSTL18_I	150	MHz
SSTL18_II	150	MHz
SSTL18D_I	150	MHz
SSTL18D_II	150	MHz
HSTL18_I	150	MHz
HSTL18_II	150	MHz
HSTL18D_I	150	MHz
HSTL18D_II	150	MHz
PCI33	134	MHz
LVTTL33	150	MHz
LVTTL33D	150	MHz
LVCMOS33	150	MHz
LVCMOS33D	150	MHz
LVCMOS25	150	MHz
LVCMOS25D	150	MHz
LVCMOS25R33	150	MHz
LVCMOS18	150	MHz
LVCMOS18D	150	MHz
LVCMOS18R33	150	MHz
LVCMOS18R25	150	MHz
LVCMOS15	150	MHz
LVCMOS15D	150	MHz
LVCMOS15R33	150	MHz
LVCMOS15R25	150	MHz
LVCMOS12	91	MHz
LVCMOS12D	91	MHz



MachXO2 External Switching Characteristics – HC/HE Devices^{1, 2, 3, 4, 5, 6, 7}

			-6		-6 -5		-4			
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units	
Clocks	•			1	1				1	
Primary Clo	ocks									
f _{MAX_PRI} ⁸	Frequency for Primary Clock Tree	All MachXO2 devices	_	388	_	323	_	269	MHz	
t _{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	0.5	_	0.6	_	0.7		ns	
		MachXO2-256HC-HE	—	912		939	—	975	ps	
		MachXO2-640HC-HE	_	844	—	871	—	908	ps	
	Primary Clock Skew Within a	MachXO2-1200HC-HE	_	868	—	902	—	951	ps	
^I SKEW_PRI	Device	MachXO2-2000HC-HE	_	867	—	897	—	941	ps	
		MachXO2-4000HC-HE	_	865	—	892	—	931	ps	
		MachXO2-7000HC-HE	_	902	—	942	—	989	ps	
Edge Clock										
f _{MAX_EDGE} ⁸	Frequency for Edge Clock	MachXO2-1200 and larger devices	_	400	_	333	_	278	MHz	
Pin-LUT-Pin	Propagation Delay									
t _{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	_	6.72		6.96		7.24	ns	
General I/O	Pin Parameters (Using Primar	y Clock without PLL)		1	1			1	1	
		MachXO2-256HC-HE	_	7.13		7.30	_	7.57	ns	
		MachXO2-640HC-HE	_	7.15		7.30	—	7.57	ns	
	Clock to Output – PIO Output	MachXO2-1200HC-HE	_	7.44		7.64	—	7.94	ns	
^I CO	Register	MachXO2-2000HC-HE	_	7.46	—	7.66	—	7.96	ns	
		MachXO2-4000HC-HE	_	7.51		7.71	—	8.01	ns	
		MachXO2-7000HC-HE	_	7.54	—	7.75	—	8.06	ns	
		MachXO2-256HC-HE	-0.06	—	-0.06	—	-0.06	—	ns	
		MachXO2-640HC-HE	-0.06	—	-0.06	-	-0.06	—	ns	
+	Clock to Data Setup – PIO	MachXO2-1200HC-HE	-0.17	—	-0.17	—	-0.17	—	ns	
ISU	Input Register	MachXO2-2000HC-HE	-0.20	—	-0.20	—	-0.20	—	ns	
		MachXO2-4000HC-HE	-0.23	—	-0.23	-	-0.23	—	ns	
		MachXO2-7000HC-HE	-0.23	—	-0.23	—	-0.23	—	ns	
		MachXO2-256HC-HE	1.75	—	1.95	—	2.16	—	ns	
		MachXO2-640HC-HE	1.75	—	1.95	—	2.16	—	ns	
+	Clock to Data Hold - PIO Input	MachXO2-1200HC-HE	1.88	—	2.12	—	2.36	—	ns	
Ч	Register	MachXO2-2000HC-HE	1.89		2.13	—	2.37	—	ns	
		MachXO2-4000HC-HE	1.94		2.18	—	2.43	—	ns	
		MachXO2-7000HC-HE	1.98		2.23	_	2.49		ns	

Over Recommended Operating Conditions



			-6		-6 -5		-5	-4		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units	
Generic DDF	R4 Inputs with Clock and Data A	Aligned at Pin Using PC	LK Pin f	or Clock	Input –	GDDRX	4_RX.E	CLK.Ali	gned ^{9, 12}	
t _{DVA}	Input Data Valid After ECLK		_	0.290	_	0.320	—	0.345	UI	
t _{DVE}	Input Data Hold After ECLK	MachXO2-640U,	0.739	—	0.699	—	0.703	—	UI	
f _{DATA}	DDRX4 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	756	_	630	_	524	Mbps	
f _{DDRX4}	DDRX4 ECLK Frequency	bottom side only."	—	378		315	—	262	MHz	
f _{SCLK}	SCLK Frequency			95	_	79	—	66	MHz	
Generic DDF	R4 Inputs with Clock and Data Co	entered at Pin Using PCI	LK Pin fo	or Clock	Input –	GDDRX4	4_RX.EC	LK.Cen	tered ^{9, 12}	
t _{SU}	Input Data Setup Before ECLK		0.233	—	0.219	—	0.198		ns	
t _{HO}	Input Data Hold After ECLK	MachXO2-640U,	0.287	—	0.287	—	0.344	—	ns	
f _{DATA}	DDRX4 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	756	_	630	_	524	Mbps	
f _{DDRX4}	DDRX4 ECLK Frequency	bottom side only.11	_	378	_	315	—	262	MHz	
f _{SCLK}	SCLK Frequency	-		95	_	79	—	66	MHz	
7:1 LVDS In	puts (GDDR71_RX.ECLK.7:1) ^{9,}	12	1						L	
t _{DVA}	Input Data Valid After ECLK			0.290		0.320	—	0.345	UI	
t _{DVE}	Input Data Hold After ECLK	-	0.739	—	0.699	—	0.703	—	UI	
f _{DATA}	DDR71 Serial Input Data Speed	MachXO2-640U, MachXO2-1200/U and		756		630		524	Mbps	
f _{DDR71}	DDR71 ECLK Frequency	larger devices, bottom		378		315	—	262	MHz	
f _{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)	Side Only.	_	108	_	90	_	75	MHz	
Generic DDF	R Outputs with Clock and Data	Aligned at Pin Using PC	LK Pin f	for Clock	c Input –	GDDR	(1_TX.S	CLK.Ali	gned ^{9, 12}	
t _{DIA}	Output Data Invalid After CLK Output		_	0.520	_	0.550	_	0.580	ns	
t _{DIB}	Output Data Invalid Before CLK Output	All MachXO2 devices, all sides.	_	0.520	_	0.550	_	0.580	ns	
f _{DATA}	DDRX1 Output Data Speed		_	300	_	250		208	Mbps	
f _{DDBX1}	DDRX1 SCLK frequency			150	_	125		104	MHz	
Generic DDF	Outputs with Clock and Data C	entered at Pin Using PC	LK Pin f	or Clock	Input –	GDDRX	1_TX.SC	LK.Cen	tered ^{9, 12}	
t _{DVB}	Output Data Valid Before CLK Output		1.210	_	1.510	_	1.870	_	ns	
t _{DVA}	Output Data Valid After CLK Output	All MachXO2 devices,	1.210	_	1.510	_	1.870	_	ns	
f _{DATA}	DDRX1 Output Data Speed	all sides.		300		250	—	208	Mbps	
f _{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		_	150	_	125	_	104	MHz	
Generic DDF	X2 Outputs with Clock and Data	Aligned at Pin Using P	CLK Pin	for Cloc	k Input	GDDR	X2_TX.E	CLK.Ali	gned ^{9, 12}	
t _{DIA}	Output Data Invalid After CLK Output		_	0.200	_	0.215		0.230	ns	
t _{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/LL and		0.200		0.215		0.230	ns	
f _{DATA}	DDRX2 Serial Output Data Speed	larger devices, top side only.	_	664	_	554	_	462	Mbps	
f _{DDRX2}	DDRX2 ECLK frequency		—	332		277	—	231	MHz	
f _{SCLK}	SCLK Frequency	1	—	166	_	139	—	116	MHz	



sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min.	Max.	Units
f _{IN}	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
fout	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)		1.5625	400	MHz
f _{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f _{VCO}	PLL VCO Frequency		200	800	MHz
f _{PFD}	Phase Detector Input Frequency		7	400	MHz
AC Characteri	stics				
t _{DT}	Output Clock Duty Cycle	Without duty trim selected ³	45	55	%
t _{DT_TRIM} ⁷	Edge Duty Trim Accuracy		-75	75	%
t _{PH} ⁴	Output Phase Accuracy		-6	6	%
	Output Cleak Pariad littar	f _{OUT} > 100 MHz	—	150	ps p-p
		f _{OUT} < 100 MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	f _{OUT} > 100 MHz	—	180	ps p-p
		f _{OUT} < 100 MHz	—	0.009	UIPP
. 1.8	Output Clock Phase Jitter	f _{PFD} > 100 MHz	—	160	ps p-p
^I OPJIT ^{''''}		f _{PFD} < 100 MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	f _{OUT} > 100 MHz	—	230	ps p-p
		f _{OUT} < 100 MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter	f _{OUT} > 100 MHz	—	230	ps p-p
	(Fractional-N)	f _{OUT} < 100 MHz	—	0.12	UIPP
t _{SPO}	Static Phase Offset	Divider ratio = integer	-120	120	ps
t _W	Output Clock Pulse Width	At 90% or 10% ³	0.9		ns
tLOCK ^{2, 5}	PLL Lock-in Time		—	15	ms
t _{UNLOCK}	PLL Unlock Time		—	50	ns
+ 6	Innut Cleak Davied Litter	f _{PFD} ≥ 20 MHz	—	1,000	ps p-p
ЧРЈІТ		f _{PFD} < 20 MHz	—	0.02	UIPP
t _{HI}	Input Clock High Time	90% to 90%	0.5	_	ns
t _{LO}	Input Clock Low Time	10% to 10%	0.5	_	ns
t _{STABLE} ⁵	STANDBY High to PLL Stable		—	15	ms
t _{RST}	RST/RESETM Pulse Width		1		ns
t _{RSTREC}	RST Recovery Time		1	—	ns
t _{RST_DIV}	RESETC/D Pulse Width		10	—	ns
t _{RSTREC_DIV}	RESETC/D Recovery Time		1	—	ns
t _{ROTATE} -SETUP	PHASESTEP Setup Time		10	—	ns

Over Recommended Operating Conditions



sysCLOCK PLL Timing (Continued)

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
t _{ROTATE_WD}	PHASESTEP Pulse Width		4		VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide for more details.

5. At minimum f_{PFD} As the f_{PFD} increases the time will decrease to approximately 60% the value listed.

6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.

7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.

8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.



sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Modes			1		
t _{PRGM}	PROGRAMN low p	55		ns	
t _{PRGMJ}	PROGRAMN low p	PROGRAMN low pulse rejection			ns
t _{INITL}	INITN low time	LCMXO2-256	—	30	μs
		LCMXO2-640	—	35	μs
		LCMXO2-640U/ LCMXO2-1200	_	55	μs
		LCMXO2-1200U/ LCMXO2-2000	—	70	μs
		LCMXO2-2000U/ LCMXO2-4000	—	105	μs
		LCMXO2-7000	—	130	μs
t _{DPPINIT}	PROGRAMN low to	D INITN Iow	—	150	ns
t _{DPPDONE}	PROGRAMN low to	DONE low	—	150	ns
t _{IODISS}	PROGRAMN low to	PROGRAMN low to I/O disable		120	ns
Slave SPI	·				
f _{MAX}	CCLK clock freque	CCLK clock frequency		66	MHz
t _{ССLКН}	CCLK clock pulse v	CCLK clock pulse width high		—	ns
t _{CCLKL}	CCLK clock pulse v	CCLK clock pulse width low		_	ns
t _{STSU}	CCLK setup time		2	—	ns
t _{STH}	CCLK hold time		0	—	ns
t _{STCO}	CCLK falling edge	to valid output	—	10	ns
t _{STOZ}	CCLK falling edge	to valid disable	—	10	ns
t _{STOV}	CCLK falling edge	to valid enable	—	10	ns
t _{SCS}	Chip select high tim	ne	25	—	ns
t _{SCSS}	Chip select setup ti	me	3	—	ns
t _{SCSH}	Chip select hold tim	ne	3	—	ns
Master SPI					
f _{MAX}	MCLK clock freque	ncy	—	133	MHz
t _{MCLKH}	MCLK clock pulse width high		3.75	—	ns
t _{MCLKL}	MCLK clock pulse width low		3.75	—	ns
t _{STSU}	MCLK setup time		5		ns
t _{STH}	MCLK hold time		1		ns
t _{CSSPI}	INITN high to chip	select low	100	200	ns
t _{MCLK}	INITN high to first N	MCLK edge	0.75	1	μs



I²C Port Timing Specifications^{1, 2}

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCL clock frequency	—	400	kHz

1. MachXO2 supports the following modes:

• Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)

• Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)

2. Refer to the I²C specification for timing requirements.

SPI Port Timing Specifications¹

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCK clock frequency		45	MHz

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

Switching Test Conditions

Figure 3-13 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-5.

Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards



Table 3-5. Test Fixture Required Components	, Non-Terminated Interfaces
---	-----------------------------

Test Condition	R1	CL	Timing Ref.	VT
			LVTTL, LVCMOS 3.3 = 1.5 V	_
LVTTL and LVCMOS settings (L -> H, H -> L)			LVCMOS 2.5 = $V_{CCIO}/2$	_
	∞	0pF	LVCMOS 1.8 = $V_{CCIO}/2$	
			LVCMOS 1.5 = $V_{CCIO}/2$	_
			LVCMOS 1.2 = $V_{CCIO}/2$	_
LVTTL and LVCMOS 3.3 (Z -> H)			1.5 V	V _{OL}
LVTTL and LVCMOS 3.3 (Z -> L)			1.5 V	V _{OH}
Other LVCMOS (Z -> H)	100	0nE	V _{CCIO} /2	V _{OL}
Other LVCMOS (Z -> L)	100	opr	V _{CCIO} /2	V _{OH}
LVTTL + LVCMOS (H -> Z)	1		V _{OH} – 0.15 V	V _{OL}
LVTTL + LVCMOS (L -> Z)			V _{OL} – 0.15 V	V _{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.



MachXO2 Family Data Sheet Pinout Information

March 2017

Data Sheet DS1035

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
		[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).
		[Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.
		[A/B/C/D] indicates the PIO within the group to which the pad is connected.
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic.
		During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.
NC	—	No connect.
GND	_	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together. For QFN 48 package, the exposed die pad is the device ground.
VCC	_	V_{CC} – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIOx	_	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.
PLL and Clock Functi	ons (Us	ed as user-programmable I/O pins when not used for PLL or clock pins)
[LOC]_GPLL[T, C]_IN	_	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]		Primary Clock pads. One to three clock pads per side.
Test and Programming	g (Dual t	function pins used for test access port and during sysCONFIG™)
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
ТСК	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	0	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
		Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then:
JTAGENB	I	If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O.
		If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.
		For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.
Configuration (Dual fu	nction p	ins used during sysCONFIG)
PROGRAMN	I	Initiates configuration sequence when asserted low. During configuration, or when reserved as PROGRAMN in user mode, this pin always has an active pull-up.

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Pinout Information Summary

		Ма	achXO2-2	256		MachXO2-640			MachXO2-640U
	32 QFN ¹	48 QFN ³	64 ucBGA	100 TQFP	132 csBGA	48 QFN ³	100 TQFP	132 csBGA	144 TQFP
General Purpose I/O per Bank	•				•			•	
Bank 0	8	10	9	13	13	10	18	19	27
Bank 1	2	10	12	14	14	10	20	20	26
Bank 2	9	10	11	14	14	10	20	20	28
Bank 3	2	10	12	14	14	10	20	20	26
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Single Ended I/O	21	40	44	55	55	40	78	79	107
Differential I/O per Bank									
Bank 0	4	5	5	7	7	5	9	10	14
Bank 1	1	5	6	7	7	5	10	10	13
Bank 2	4	5	5	7	7	5	10	10	10
Bank 3	1	5	6	7	7	5	10	10	13
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Differential I/O	10	20	22	28	28	20	39	40	54
	10	20		20	20	20	00	10	01
Dual Function I/O	22	25	27	29	29	25	29	29	33
High-speed Differential I/O									
Bank 0	0	0	0	0	0	0	0	0	7
Gearboxes									
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	0	0	0	0	0	0	0	0	7
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	0	0	0	0	0	0	0	0	7
DQS Groups	•		•		•			•	
Bank 1	0	0	0	0	0	0	0	0	2
									•
VCCIO Pins									
Bank 0	2	2	2	2	2	2	2	2	3
Bank 1	1	1	2	2	2	1	2	2	3
Bank 2	2	2	2	2	2	2	2	2	3
Bank 3	1	1	2	2	2	1	2	2	3
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
									•
VCC	2	2	2	2	2	2	2	2	4
GND ²	2	1	8	8	8	1	8	10	12
NC	0	0	1	26	58	0	3	32	8
Reserved for Configuration	1	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	32	49	64	100	132	49	100	132	144

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.

2. For 48 QFN package, exposed die pad is the device ground.

3. 48-pin QFN information is 'Advanced'.



				MachX	02-4000			
	84 QFN	132 csBGA	144 TQFP	184 csBGA	256 caBGA	256 ftBGA	332 caBGA	484 fpBGA
General Purpose I/O per Bank								
Bank 0	27	25	27	37	50	50	68	70
Bank 1	10	26	29	37	52	52	68	68
Bank 2	22	28	29	39	52	52	70	72
Bank 3	0	7	9	10	16	16	24	24
Bank 4	9	8	10	12	16	16	16	16
Bank 5	0	10	10	15	20	20	28	28
Total General Purpose Single Ended I/O	68	104	114	150	206	206	274	278
Differential I/O per Bank								
Bank 0	13	13	14	18	25	25	34	35
Bank 1	4	13	14	18	26	26	34	34
Bank 2	11	14	14	19	26	26	35	36
Bank 3	0	3	4	4	8	8	12	12
Bank 4	4	4	5	6	8	8	8	8
Bank 5	0	5	5	7	10	10	14	14
Total General Purpose Differential I/O	32	52	56	72	103	103	137	139
Dual Function I/O	28	37	37	37	37	37	37	37
High-speed Differential I/O								
Bank 0	8	8	9	8	18	18	18	18
Gearboxes					-			-
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	8	8	9	9	18	18	18	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	11	14	14	12	18	18	18	18
DQS Groups				-				
Bank 1	1	2	2	2	2	2	2	2
VCCIO Pins								
Bank 0	3	3	3	3	4	4	4	10
Bank 1	1	3	3	3	4	4	4	10
Bank 2	2	3	3	3	4	4	4	10
Bank 3	1	1	1	1	1	1	2	3
Bank 4	1	1	1	1	2	2	1	4
Bank 5	1	1	1	1	1	1	2	3
VCC	4	4	4	4	8	8	8	12
GND	4	10	12	16	24	24	27	48
NC	1	1	1	1	1	1	5	105
Reserved for configuration	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	84	132	144	184	256	256	332	484





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	MachXO2-7000						
	144 TQFP	256 caBGA	256 ftBGA	332 caBGA	400 caBGA	484 fpBGA	
General Purpose I/O per Bank							
Bank 0	27	50	50	68	83	82	
Bank 1	29	52	52	70	84	84	
Bank 2	29	52	52	70	84	84	
Bank 3	9	16	16	24	28	28	
Bank 4	10	16	16	16	24	24	
Bank 5	10	20	20	30	32	32	
Total General Purpose Single Ended I/O	114	206	206	278	335	334	
		·					
Differential I/O per Bank							
Bank 0	14	25	25	34	42	41	
Bank 1	14	26	26	35	42	42	
Bank 2	14	26	26	35	42	42	
Bank 3	4	8	8	12	14	14	
Bank 4	5	8	8	8	12	12	
Bank 5	5	10	10	15	16	16	
Total General Purpose Differential I/O	56	103	103	139	168	167	
		•			1	1	
Dual Function I/O	37	37	37	37	37	37	
High-speed Differential I/O							
Bank 0	9	20	20	21	21	21	
Gearboxes	1	I			I		
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	9	20	20	21	21	21	
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	14	20	20	21	21	21	
DQS Groups							
Bank 1	2	2	2	2	2	2	
VCCIO Pins							
Bank 0	3	4	4	4	5	10	
Bank 1	3	4	4	4	5	10	
Bank 2	3	4	4	4	5	10	
Bank 3	1	1	1	2	2	3	
Bank 4	1	2	2	1	2	4	
Bank 5	1	1	1	2	2	3	
		•					
VCC	4	8	8	8	10	12	
GND	12	24	24	27	33	48	
NC	1	1	1	1	0	49	
Reserved for Configuration	1	1	1	1	1	1	
Total Count of Bonded Pins	144	256	256	332	400	484	



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32I	1280	2.5 V / 3.3 V	-4	Halogen-Free QFN	32	IND
LCMXO2-1200HC-5SG32I	1280	2.5 V / 3.3 V	-5	Halogen-Free QFN	32	IND
LCMXO2-1200HC-6SG32I	1280	2.5 V / 3.3 V	-6	Halogen-Free QFN	32	IND
LCMXO2-1200HC-4TG100I	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100I	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100I	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132I	1280	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132I	1280	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132I	1280	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144I	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144I	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144I	1280	2.5 V/ 3.3 V	-6	Halogen-Free TQFP	144	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256I	1280	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-5FTG256I	1280	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-6FTG256I	1280	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100I	2112	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-5TG100I	2112	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-6TG100I	2112	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-4MG132I	2112	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-5MG132I	2112	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-6MG132I	2112	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-4TG144I	2112	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-5TG144I	2112	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-6TG144I	2112	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-4BG256I	2112	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-5BG256I	2112	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-6BG256I	2112	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-4FTG256I	2112	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-5FTG256I	2112	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-6FTG256I	2112	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484I	2112	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-5FG484I	2112	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-6FG484I	2112	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	IND



High Performance Industrial Grade Devices Without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100I	2112	1.2 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-5TG100I	2112	1.2 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-6TG100I	2112	1.2 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-4MG132I	2112	1.2 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-5MG132I	2112	1.2 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-6MG132I	2112	1.2 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-4TG144I	2112	1.2 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-5TG144I	2112	1.2 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-6TG144I	2112	1.2 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-4BG256I	2112	1.2 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-5BG256I	2112	1.2 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-6BG256I	2112	1.2 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-4FTG256I	2112	1.2 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-5FTG256I	2112	1.2 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-6FTG256I	2112	1.2 V	-6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484I	2112	1.2 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-5FG484I	2112	1.2 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-6FG484I	2112	1.2 V	-6	Halogen-Free fpBGA	484	IND