Lattice Semiconductor Corporation - LCMXO2-640ZE-3TG100C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	18432
Number of I/O	78
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-640ze-3tg100c

MachXO2 Family Data Sheet Introduction

May 2016 **Data Sheet DS1035**

Features

- **Flexible Logic Architecture**
  - Six devices with 256 to 6864 LUT4s and 18 to 334 I/Os
- **Ultra Low Power Devices**
  - Advanced 65 nm low power process
  - As low as 22 µW standby power
  - Programmable low swing differential I/Os
  - Stand-by mode and other power saving options
- **Embedded and Distributed Memory**
  - Up to 240 kbits sysMEM™ Embedded Block RAM
  - Up to 54 kbits Distributed RAM
  - Dedicated FIFO control logic
- **On-Chip User Flash Memory**
  - Up to 256 kbits of User Flash Memory
  - 100,000 write cycles
  - Accessible through WISHBONE, SPI, I^{2}C and JTAG interfaces
  - Can be used as soft processor PROM or as Flash memory
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated gearing logic
  - 7:1 Gearing for Display I/Os
  - Generic DDR, DDRX2, DDRX4
  - Dedicated DDR/DDR2/LPDDR memory with DQS support
- **High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - PCI
    - LVDS, Bus-LVDS, MLVDS, RSDS, LVPECL
    - SSTL 25/18
    - HSTL 18
    - Schmitt trigger inputs, up to 0.5 V hysteresis
  - I/Os support hot socketing
  - On-chip differential termination
  - Programmable pull-up or pull-down mode
- **Flexible On-Chip Clocking**
  - Eight primary clocks
  - Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
  - Up to two analog PLLs per device with fractional-n frequency synthesis
    - Wide input frequency range (7 MHz to 400 MHz)
- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - Single-chip, secure solution
  - Programmable through JTAG, SPI or I^{2}C
  - Supports background programming of non-volatile memory
  - Optional dual boot with external SPI memory
- **TransFR™ Reconfiguration**
  - In-field logic update while system operates
- **Enhanced System Level Support**
  - On-chip hardened functions: SPI, I^{2}C, timer/counter
  - On-chip oscillator with 5.5% accuracy
  - Unique TraceID for system tracking
  - One Time Programmable (OTP) mode
  - Single power supply with extended operating range
  - IEEE Standard 1149.1 boundary scan
  - IEEE 1532 compliant in-system programming
- **Broad Range of Package Options**
  - TQFP, WLCSP, ucBGA, csBGA, caBGA, ftBGA, fpBGA, QFN package options
  - Small footprint package options
    - As small as 2.5 mm x 2.5 mm
  - Density migration supported
  - Advanced halogen-free packaging

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - — A greater-than-or-equal-to B
  - — A not-equal-to B
  - — A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO2 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO2 devices, please see TN1201, Memory Usage Guide for MachXO2 Devices.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

Routing

There are many resources provided in the MachXO2 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Each MachXO2 device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

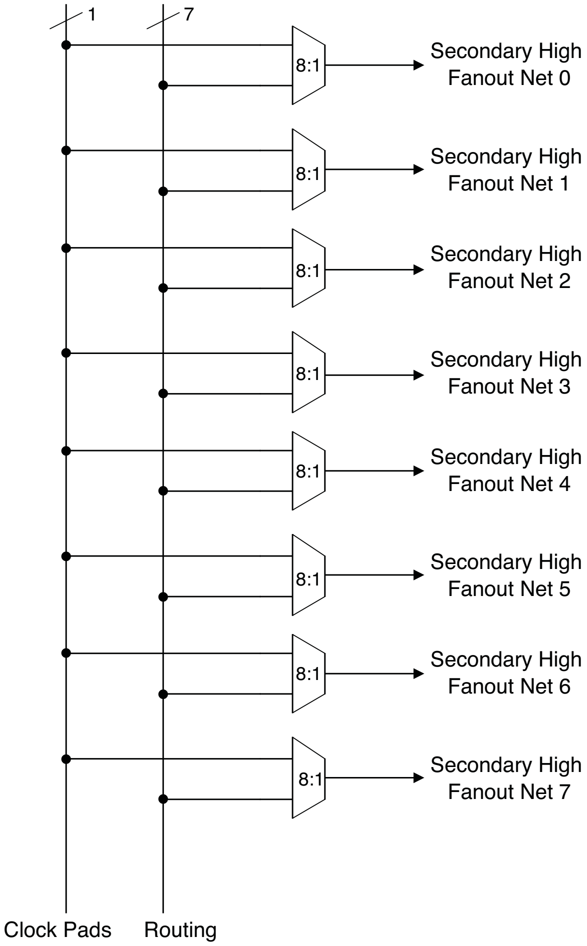
The MachXO2 architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO2-640U, MachXO2-1200/U and higher density devices have two edge clocks each on the top and bottom edges. Lower density devices have no edge clocks. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO2 devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO2 External Switching Characteristics table.

The primary clock signals for the MachXO2-256 and MachXO2-640 are generated from eight 17:1 muxes The available clock sources include eight I/O sources and 9 routing inputs. Primary clock signals for the MachXO2-640U, MachXO2-1200/U and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.

Figure 2-6. Secondary High Fanout Nets for MachXO2 Devices



sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The MachXO2-640U, MachXO2-1200/U and larger devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO2 sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO2 clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO2 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

For more details on these embedded functions, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

User Flash Memory (UFM)

MachXO2-640/U and higher density devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I^2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

Standby Mode and Power Saving Options

MachXO2 devices are available in three options for maximum flexibility: ZE, HC and HE devices. The ZE devices have ultra low static and dynamic power consumption. These devices use a 1.2 V core voltage that further reduces power consumption. The HC and HE devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the HE devices operate at 1.2 V V_{CC}.

MachXO2 devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO2 devices support an ultra low power Stand-by mode. While most of these features are available in all three device types, these features are mainly intended for use with MachXO2 ZE devices to manage power consumption.

In the stand-by mode the MachXO2 devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I^2C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO2 devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

Table 2-18. MachXO2 Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe V_{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1198, Power Estimation and Management for MachXO2 Devices.

Power On Reset

MachXO2 devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the V_{PORUP} level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices), V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators (HC devices), V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time ($t_{REFRESH}$) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tristate. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min) they should not shut down the bandgap or POR circuit.

Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I^2C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

1. Internal Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I^2C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, MachXO2 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

RSDS

The MachXO2 family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

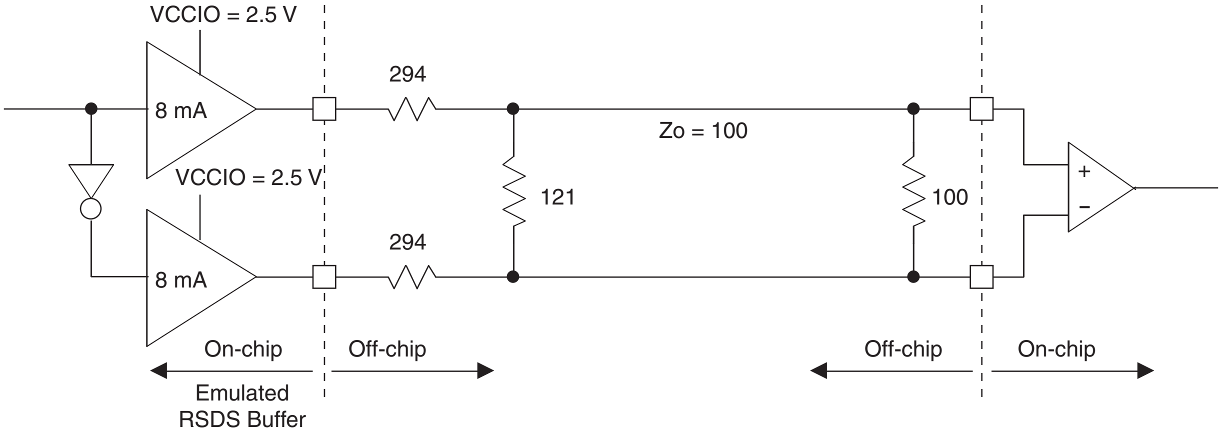


Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	294	Ohms
R_P	Driver parallel resistor	121	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	Ohms
I_{DC}	DC output current	3.66	mA

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.535	—	0.670	—	0.830	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	0.830	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.455	—	0.570	—	0.710	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.455	—	0.570	—	0.710	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[9, 12]									
t_{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.160	—	0.180	—	0.200	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.160	—	0.180	—	0.200	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.369	—	0.395	—	0.421	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.529	—	0.530	—	0.527	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM LPDDR Serial Data Speed		—	280	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	140	—	125	—	104	MHz
f_{LPDDR}	LPDDR Data Transfer Rate		0	280	0	250	0	208	Mbps
DDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.350	—	0.387	—	0.414	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.545	—	0.538	—	0.532	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	150	—	125	—	104	MHz
f_{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps
DDR2[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.360	—	0.378	—	0.406	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.555	—	0.549	—	0.542	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	150	—	125	—	104	MHz
f_{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\text{ ns})/2$.
7. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps (–6), 113 ps (–5), 120 ps (–4).
8. This number for general purpose usage. Duty cycle tolerance is +/– 10%.
9. Duty cycle is +/–5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32 QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	1.445	—	1.760	—	2.140	—	ns
t_{DVA}	Output Data Valid After CLK Output		1.445	—	1.760	—	2.140	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	—	0.270	—	0.300	—	0.330	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.270	—	0.300	—	0.330	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only	0.873	—	1.067	—	1.319	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.873	—	1.067	—	1.319	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[9, 12]									
t_{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.240	—	0.270	—	0.300	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.240	—	0.270	—	0.300	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	420	—	352	—	292	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	210	—	176	—	146	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	60	—	50	—	42	MHz

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.349	—	0.381	—	0.396	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.630	—	0.613	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM LPDDR Serial Data Speed		—	120	—	110	—	96	Mbps
f_{SCLK}	SCLK Frequency		—	60	—	55	—	48	MHz
f_{LPDDR}	LPDDR Data Transfer Rate		0	120	0	110	0	96	Mbps
DDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.347	—	0.374	—	0.393	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.637	—	0.616	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f_{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f_{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps
DDR2[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.372	—	0.394	—	0.410	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.690	—	0.658	—	0.618	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f_{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f_{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\text{ ns})/2$.
7. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 167 ps (–3), 182 ps (–2), 195 ps (–1).
8. This number for general purpose usage. Duty cycle tolerance is +/–10%.
9. Duty cycle is +/– 5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

Figure 3-5. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms

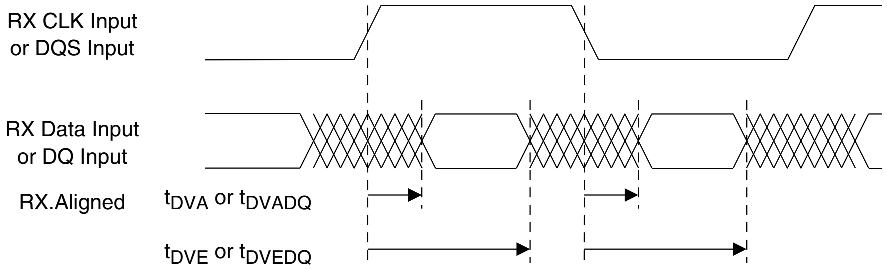


Figure 3-6. Receiver RX.CLK.Centered Waveforms

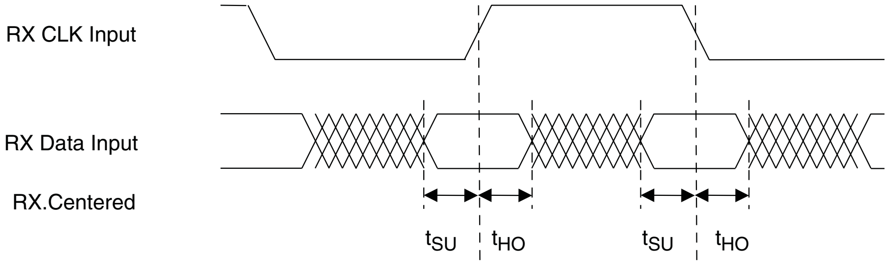


Figure 3-7. Transmitter TX.CLK.Aligned Waveforms

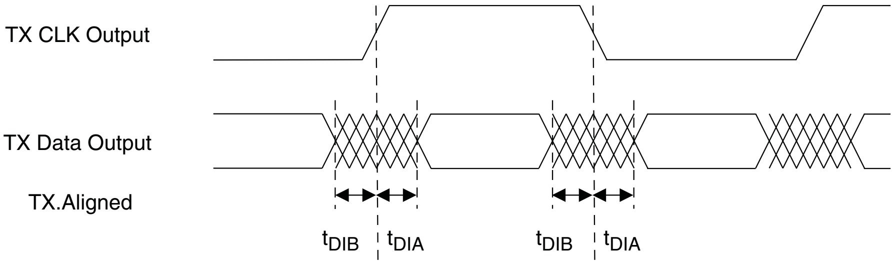
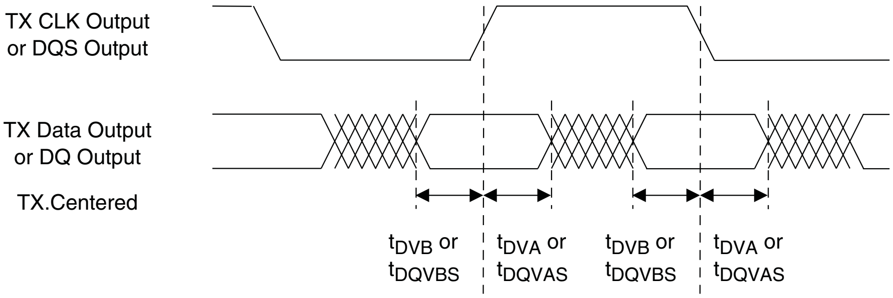


Figure 3-8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms



	MachXO2-2000						MachXO2-2000U
	49 WLCSP	100 TQFP	132 csBGA	144 TQFP	256 caBGA	256 ftBGA	484 ftBGA
General Purpose I/O per Bank							
Bank 0	19	18	25	27	50	50	70
Bank 1	0	21	26	28	52	52	68
Bank 2	13	20	28	28	52	52	72
Bank 3	0	6	7	8	16	16	24
Bank 4	0	6	8	10	16	16	16
Bank 5	6	8	10	10	20	20	28
Total General Purpose Single-Ended I/O	38	79	104	111	206	206	278
Differential I/O per Bank							
Bank 0	7	9	13	14	25	25	35
Bank 1	0	10	13	14	26	26	34
Bank 2	6	10	14	14	26	26	36
Bank 3	0	3	3	4	8	8	12
Bank 4	0	3	4	5	8	8	8
Bank 5	3	4	5	5	10	10	14
Total General Purpose Differential I/O	16	39	52	56	103	103	139
Dual Function I/O	24	31	33	33	33	33	37
High-speed Differential I/O							
Bank 0	5	4	8	9	14	14	18
Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	4	8	9	14	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	10	14	14	14	14	18
DQS Groups							
Bank 1	0	1	2	2	2	2	2
VCCIO Pins							
Bank 0	2	2	3	3	4	4	10
Bank 1	0	2	3	3	4	4	10
Bank 2	1	2	3	3	4	4	10
Bank 3	0	1	1	1	1	1	3
Bank 4	0	1	1	1	2	2	4
Bank 5	1	1	1	1	1	1	3
VCC	2	2	4	4	8	8	12
GND	4	8	10	12	24	24	48
NC	0	1	1	4	1	1	105
Reserved for Configuration	1	1	1	1	v	1	1
Total Count of Bonded Pins	39	100	132	144	256	256	484

	MachXO2-7000					
	144 TQFP	256 caBGA	256 ftBGA	332 caBGA	400 caBGA	484 fpBGA
General Purpose I/O per Bank						
Bank 0	27	50	50	68	83	82
Bank 1	29	52	52	70	84	84
Bank 2	29	52	52	70	84	84
Bank 3	9	16	16	24	28	28
Bank 4	10	16	16	16	24	24
Bank 5	10	20	20	30	32	32
Total General Purpose Single Ended I/O	114	206	206	278	335	334
Differential I/O per Bank						
Bank 0	14	25	25	34	42	41
Bank 1	14	26	26	35	42	42
Bank 2	14	26	26	35	42	42
Bank 3	4	8	8	12	14	14
Bank 4	5	8	8	8	12	12
Bank 5	5	10	10	15	16	16
Total General Purpose Differential I/O	56	103	103	139	168	167
Dual Function I/O	37	37	37	37	37	37
High-speed Differential I/O						
Bank 0	9	20	20	21	21	21
Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	9	20	20	21	21	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	14	20	20	21	21	21
DQS Groups						
Bank 1	2	2	2	2	2	2
VCCIO Pins						
Bank 0	3	4	4	4	5	10
Bank 1	3	4	4	4	5	10
Bank 2	3	4	4	4	5	10
Bank 3	1	1	1	2	2	3
Bank 4	1	2	2	1	2	4
Bank 5	1	1	1	2	2	3
VCC	4	8	8	8	10	12
GND	12	24	24	27	33	48
NC	1	1	1	1	0	49
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	144	256	256	332	400	484

For Further Information

For further information regarding logic signal connections for various packages please refer to the MachXO2 Device Pinout Files.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Users must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1198, Power Estimation and Management for MachXO2 Devices
- The Power Calculator tool is included with the Lattice design tools, or as a standalone download from www.latticesemi.com/software

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100IR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100IR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100IR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132IR1[1]	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132IR1[1]	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132IR1[1]	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144IR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144IR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144IR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200ZE-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

R1 Device Specifications

The LCMXO2-1200ZE/HC "R1" devices have the same specifications as their Standard (non-R1) counterparts except as listed below. For more details on the R1 to Standard migration refer to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard Non-R1) Devices.

- The User Flash Memory (UFM) cannot be programmed through the internal WISHBONE interface. It can still be programmed through the JTAG/SPI/I^{2}C ports.
- The on-chip differential input termination resistor value is higher than intended. It is approximately 200Ω as opposed to the intended 100Ω. It is recommended to use external termination resistors for differential inputs. The on-chip termination resistors can be disabled through Lattice design software.
- Soft Error Detection logic may not produce the correct result when it is run for the first time after configuration. To use this feature, discard the result from the first operation. Subsequent operations will produce the correct result.
- Under certain conditions, IIH exceeds data sheet specifications. The following table provides more details:

Condition	Clamp	Pad Rising IIH Max.	Pad Falling IIH Min.	Steady State Pad High IIH	Steady State Pad Low IIL
VPAD > VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD = VCCIO	ON	10 µA	–10 µA	10 µA	10 µA
VPAD = VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD < VCCIO	OFF	10 µA	–10 µA	10 µA	10 µA

- The user SPI interface does not operate correctly in some situations. During master read access and slave write access, the last byte received does not generate the RRDY interrupt.
- In GDDRX2, GDDRX4 and GDDR71 modes, ECLKSYNC may have a glitch in the output under certain conditions, leading to possible loss of synchronization.
- When using the hard I^{2}C IP core, the I^{2}C status registers I2C_1_SR and I2C_2_SR may not update correctly.
- PLL Lock signal will glitch high when coming out of standby. This glitch lasts for about 10 µsec before returning low.
- Dual boot only available on HC devices, requires tying VCC and VCCIO2 to the same 3.3 V or 2.5 V supply.

MachXO2 Family Data Sheet
Revision History

March 2017 **Data Sheet DS1035**

Date	Version	Section	Change Summary
March 2017	3.3	DC and Switching Characteristics	Updated the Absolute Maximum Ratings section. Added standards.
			Updated the sysIO Recommended Operating Conditions section. Added standards.
			Updated the sysIO Single-Ended DC Electrical Characteristics section. Added standards.
			Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and $D_{IA.}$ The parameter descriptions were also modified.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and $D_{IA.}$ The parameter descriptions were also modified.
			Updated the sysCONFIG Port Timing Specifications section. Corrected the t_{INITL} units from ns to µs.
		Pinout Information	Updated the Signal Descriptions section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals.
			Updated the Pinout Information Summary section. Added footnote to MachXO2-1200 32 QFN.
		Ordering Information	Updated the MachXO2 Part Number Description section. Corrected the MG184, BG256, FTG256 package information. Added “(0.8 mm Pitch)” to BG332.
			Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. — Updated LCMXO2-1200ZE-1UWG25ITR50 footnote. — Corrected footnote numbering typo. — Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2-2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s.