## E · ) ( Fattice Semiconductor Corporation - <u>LCMXO2-7000HC-5FTG256I Datasheet</u>



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	858
Number of Logic Elements/Cells	6864
Total RAM Bits	245760
Number of I/O	206
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-7000hc-5ftg256i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



## Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), preengineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I<sup>2</sup>C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external V<sub>CC</sub> supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V<sub>CC</sub> supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pulldown and bus-keeper features are controllable on a "per-pin" basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I<sup>2</sup>C port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE<sup>™</sup> modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.



## MachXO2 Family Data Sheet Architecture

#### March 2016

Data Sheet DS1035

## **Architecture Overview**

The MachXO2 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have sysCLOCK<sup>™</sup> PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.





Note: MachXO2-256, and MachXO2-640/U are similar to MachXO2-1200. MachXO2-256 has a lower LUT count and no PLL or EBR blocks. MachXO2-640 has no PLL, a lower LUT count and two EBR blocks. MachXO2-640U has a lower LUT count, one PLL and seven EBR blocks.

Figure 2-2. Top View of the MachXO2-4000 Device



Note: MachXO2-1200U, MachXO2-2000/U and MachXO2-7000 are similar to MachXO2-4000. MachXO2-1200U and MachXO2-2000 have a lower LUT count, one PLL, and eight EBR blocks. MachXO2-2000U has a lower LUT count, two PLLs, and 10 EBR blocks. MachXO2-7000 has a higher LUT count, two PLLs, and 26 EBR blocks.

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The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag "hard" control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysl/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2-640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO2 devices provide commonly used hardened functions such as SPI controller, I<sup>2</sup>C controller and timer/ counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I<sup>2</sup>C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

## **PFU Blocks**

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.



This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the  $t_{I,OCK}$  parameter has been satisfied.

The MachXO2 also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO2 PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the t<sub>LOCK</sub> parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

For more details on the PLL and the WISHBONE interface, see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.



### Figure 2-7. PLL Diagram

Table 2-4 provides signal descriptions of the PLL block.

Port Name	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	I	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	I	Dynamic Phase step – toggle shifts VCO phase adjust by one step.



#### Table 2-4. PLL Signal Descriptions (Continued)

Port Name	I/O	Description
CLKOP	0	Primary PLL output clock (with phase shift adjustment)
CLKOS	0	Secondary PLL output clock (with phase shift adjust)
CLKOS2	0	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	0	Secondary PLL output clock3 (with phase shift adjust)
LOCK	0	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feed- back signals.
DPHSRC	0	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset - includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	0	PLL data bus data output
PLLACK	0	PLL data bus acknowledge signal

## sysMEM Embedded Block RAM Memory

The MachXO2-640/U and larger devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

#### sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.



 Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

#### Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

#### **RAM Initialization and ROM Operation**

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO2 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

#### Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

#### Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.







## **Tri-state Register Block**

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

The tri-state register blocks on the right edge contain an additional register for DDR memory operation. In DDR memory mode, the register TS input is fed into another register that is clocked using the DQSW90 signal. The output of this register is used as a tri-state control.

## **Input Gearbox**

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

Table 2-9.	Input	Gearbox	Sianal List
14010 2 01	mpar	acaison	orginal Eloc

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3



More information on the input gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.

## **Output Gearbox**

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

#### Table 2-10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDRX4(8:1): D[7:0]		
GDDRX2(4:1)(IOL-A): D[3:0]		
GDDRX2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-17 shows the output gearbox block diagram.



Figure 2-18. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 Banks



Figure 2-19. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks





# MachXO2 Family Data Sheet DC and Switching Characteristics

#### March 2017

#### Data Sheet DS1035

## Absolute Maximum Ratings<sup>1, 2, 3</sup>

	MachXO2 ZE/HE (1.2 V)	MachXO2 HC (2.5 V / 3.3 V)
Supply Voltage V <sub>CC</sub>	–0.5 V to 1.32 V	0.5 V to 3.75 V
Output Supply Voltage V <sub>CCIO</sub>	–0.5 V to 3.75 V	0.5 V to 3.75 V
I/O Tri-state Voltage Applied <sup>4, 5</sup>	–0.5 V to 3.75 V	0.5 V to 3.75 V
Dedicated Input Voltage Applied <sup>4</sup>	–0.5 V to 3.75 V	0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature $(T_1)$	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

2. Compliance with the Lattice Thermal Management document is required.

3. All voltages referenced to GND.

4. Overshoot and undershoot of -2 V to (V<sub>IHMAX</sub> + 2) volts is permitted for a duration of <20 ns.

5. The dual function  $I^2C$  pins SCL and SDA are limited to -0.25 V to 3.75 V or to -0.3 V with a duration of <20 ns.

## **Recommended Operating Conditions**<sup>1</sup>

Symbol	Parameter	Min.	Max.	Units
V = = <sup>1</sup>	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
VCC	Core Supply Voltage for 2.5 V / 3.3 V Devices	2.375	3.6	V
V <sub>CCIO</sub> <sup>1, 2, 3</sup>	I/O Driver Supply Voltage	1.14	3.6	V
t <sub>JCOM</sub>	Junction Temperature Commercial Operation	0	85	°C
t <sub>JIND</sub>	Junction Temperature Industrial Operation	-40	100	°C

1. Like power supplies must be tied together. For example, if  $V_{CCIO}$  and  $V_{CC}$  are both the same voltage, they must also be the same supply.

2. See recommended voltages by I/O standard in subsequent table.

3. V<sub>CCIO</sub> pins of unused I/O banks should be connected to the V<sub>CC</sub> power supply on boards.

## Power Supply Ramp Rates<sup>1</sup>

Symbol	Parameter	Min.	Тур.	Max.	Units
t <sub>RAMP</sub>	Power supply ramp rates for all power supplies.	0.01		100	V/ms

1. Assumes monotonic ramp rates.

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## sysIO Single-Ended DC Electrical Characteristics<sup>1, 2</sup>

Input/Output	V <sub>IL</sub>		v <sub>i</sub>	н	Vo. Max.	Vou Min.	lo₁ Max. <sup>4</sup>	lo⊔ Max.⁴
Standard	Min. (V) <sup>3</sup>	Max. (V)	Min. (V)	Max. (V)	(V)	(V)	(mA)	(mA)
							4	-4
LVCMOS 3.3							8	-8
	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	12	-12
LVTTL	-0.0	0.0	2.0	0.0			16	-16
							24	-24
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
							4	-4
					04	$V_{000} = 0.4$	8	-8
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	VCCI0 0.4	12	-12
							16	-16
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
							4	-4
	0.2	0.25\/	0.651/	0.0	0.4	$V_{CCIO} - 0.4$	8	-8
	-0.3	0.33 v CCIO	0.03 A CCIO	3.0			12	-12
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
	-0.3	0.35V <sub>CCIO</sub>	0.65V <sub>CCIO</sub>	3.6	0.4	V <sub>CCIO</sub> - 0.4	4	-4
LVCMOS 1.5					0.4		8	-8
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
	-0.3	0.35V <sub>CCIO</sub>	0.65V <sub>CCIO</sub>	3.6	0.4	V <sub>CCIO</sub> - 0.4	4	-2
LVCMOS 1.2							8	-6
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
PCI	-0.3	0.3V <sub>CCIO</sub>	0.5V <sub>CCIO</sub>	3.6	0.1V <sub>CCIO</sub>	0.9V <sub>CCIO</sub>	1.5	-0.5
SSTL25 Class I	-0.3	V <sub>REF</sub> - 0.18	V <sub>REF</sub> + 0.18	3.6	0.54	V <sub>CCIO</sub> - 0.62	8	8
SSTL25 Class II	-0.3	V <sub>REF</sub> - 0.18	V <sub>REF</sub> + 0.18	3.6	NA	NA	NA	NA
SSTL18 Class I	-0.3	V <sub>REF</sub> – 0.125	V <sub>REF</sub> + 0.125	3.6	0.40	V <sub>CCIO</sub> - 0.40	8	8
SSTL18 Class II	-0.3	V <sub>REF</sub> – 0.125	V <sub>REF</sub> + 0.125	3.6	NA	NA	NA	NA
HSTL18 Class I	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	0.40	V <sub>CCIO</sub> - 0.40	8	8
HSTL18 Class II	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	NA	NA	NA	NA
LVCMOS25R33	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R33	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R25	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R33	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R25	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	NA	NA	NA	NA
LVCMOS12R33	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	-0.3	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain



## Typical Building Block Function Performance – HC/HE Devices<sup>1</sup>

## Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	-6 Timing	Units
Basic Functions		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

## **Register-to-Register Performance**

Function	-6 Timing	Units
Basic Functions	·	
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
Embedded Memory Functions	•	
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

 The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.



## Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
LVDS25	400	MHz
LVDS25E	150	MHz
RSDS25	150	MHz
RSDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
SSTL25_I	150	MHz
SSTL25_II	150	MHz
SSTL25D_I	150	MHz
SSTL25D_II	150	MHz
SSTL18_I	150	MHz
SSTL18_II	150	MHz
SSTL18D_I	150	MHz
SSTL18D_II	150	MHz
HSTL18_I	150	MHz
HSTL18_II	150	MHz
HSTL18D_I	150	MHz
HSTL18D_II	150	MHz
PCI33	134	MHz
LVTTL33	150	MHz
LVTTL33D	150	MHz
LVCMOS33	150	MHz
LVCMOS33D	150	MHz
LVCMOS25	150	MHz
LVCMOS25D	150	MHz
LVCMOS25R33	150	MHz
LVCMOS18	150	MHz
LVCMOS18D	150	MHz
LVCMOS18R33	150	MHz
LVCMOS18R25	150	MHz
LVCMOS15	150	MHz
LVCMOS15D	150	MHz
LVCMOS15R33	150	MHz
LVCMOS15R25	150	MHz
LVCMOS12	91	MHz
LVCMOS12D	91	MHz



Parameter         Description         Device         Min.         Max.         Max. <th></th>	
$t_{SU\_DEL} = t_{A\_DEL} = t_{A\_DE} = t_$	Jnits
$t_{SU\_DEL} = t_{A\_DEL} \begin{bmatrix} Clock to Data Setup - PIO Input Register with Data Input Delay \\ Clock to Data Setup - PIO Input Register with Data Input Delay \\ Delay \\ \hline \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ $	ns
$ t_{SU_DEL} \begin{bmatrix} Clock to Data Setup - PIO Input Register with Data Input Delay \\ Leven below \\ Leven$	ns
$ \frac{1}{1} SU_{DEL} = 1 \\ \frac{1}{1} SU_{DE} = 1 \\ 1$	ns
$\frac{MachXO2-4000ZE}{MachXO2-7000ZE} \begin{array}{c} 2.39 \\ \hline - \end{array} \begin{array}{c} 2.60 \\ - \end{array} \begin{array}{c} - 2.76 \\ - \end{array} \begin{array}{c} - n \\ n \\ \hline - n \\ - n \\ \hline - n \\ \hline - n \\ \hline - n \\ - n \\$	ns
MachXO2-7000ZE         2.17         —         2.33         —         2.43         —         n           MachXO2-200ZE         2.17         —         2.33         —         2.43         —         n           MachXO2-200ZE         -0.44         —         -0.44         —         -0.44         —         n           MachXO2-266ZE         -0.43         —         -0.43         —         -0.43         —         n           MachXO2-640ZE         -0.43         —         -0.43         —         -0.43         —         n           MachXO2-1200ZE         -0.28         —         -0.28         —         -0.28         —         n           MachXO2-2000ZE         -0.31         —         -0.31         —         n         n           MachXO2-2000ZE         -0.31         —         -0.34         —         -0.34         —         n           MachXO2-4000ZE         -0.34         —         -0.21         —         -0.21         —         n	ns
$t_{H\_DEL} = \begin{bmatrix} MachXO2-256ZE & -0.44 & - & -0.44 & - & -0.44 & - & n \\ MachXO2-640ZE & -0.43 & - & -0.43 & - & -0.43 & - & n \\ MachXO2-1200ZE & -0.28 & - & -0.28 & - & -0.28 & - & n \\ MachXO2-2000ZE & -0.31 & - & -0.31 & - & -0.31 & - & n \\ MachXO2-4000ZE & -0.34 & - & -0.34 & - & -0.34 & - & n \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & n \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & n \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & n \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & n \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 & - & n \\ \end{bmatrix}$	ns
$t_{H\_DEL} = \begin{bmatrix} Clock to Data Hold - PIO Input \\ Register with Input Data Delay \end{bmatrix} \begin{bmatrix} MachXO2-640ZE & -0.43 & - & -0.43 & - & -0.43 & - & n \\ MachXO2-1200ZE & -0.28 & - & -0.28 & - & -0.28 & - & n \\ MachXO2-2000ZE & -0.31 & - & -0.31 & - & -0.31 & - & n \\ MachXO2-4000ZE & -0.34 & - & -0.34 & - & -0.34 & - & n \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & n \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & n \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & n \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & n \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -0.21 & - & -0.21 & - & - & -0.21 \\ MachXO2-7000ZE & -0.21 & - & -& -0.21 & - & - & -& -& -& -& -& -& -& -& -& -&$	ns
$ \begin{array}{c} \mbox{th} L_{\rm H_DEL} \end{array} \begin{array}{c} \mbox{Clock to Data Hold - PIO Input} \\ \mbox{Register with Input Data Delay} \end{array} \begin{array}{c} \mbox{MachXO2-1200ZE} & -0.28 & - & -0.28 & - & -0.28 & - & n \\ \mbox{MachXO2-2000ZE} & -0.31 & - & -0.31 & - & -0.31 & - & n \\ \mbox{MachXO2-4000ZE} & -0.34 & - & -0.34 & - & -0.34 & - & n \\ \mbox{MachXO2-7000ZE} & -0.21 & - & -0.21 & - & -0.21 & - & n \\ \mbox{MachXO2-7000ZE} & -0.21 & - & -0.21 & - & -0.21 & - & n \\ \mbox{MachXO2-7000ZE} & -0.21 & - & -0.21 & - & -0.21 & - & n \\ \mbox{MachXO2-7000ZE} & -0.21 & - & -0.21 & - & -0.21 & - & n \\ \end{tabular} $	ns
IH_DEL         Register with Input Data Delay         MachXO2-2000ZE         -0.31         -         -0.31         -         n           MachXO2-4000ZE         -0.34         -         -0.34         -         -0.34         -         n           MachXO2-7000ZE         -0.21         -         -0.21         -         -0.21         -         n	ns
MachXO2-4000ZE         -0.34         -         -0.34         -         n           MachXO2-7000ZE         -0.21         -         -0.21         -         -         n	ns
MachXO2-7000ZE -0.210.21 - n	ns
	ns
If_MAX_IO     Clock Frequency of I/O and PFU Register     All MachXO2 devices     —     150     —     125     —     104     MH	ИНz
General I/O Pin Parameters (Using Edge Clock without PLL)	
MachXO2-1200ZE — 11.10 — 11.51 — 11.91 n	ns
Clock to Output – PIO Output MachXO2-2000ZE – 11.10 – 11.51 – 11.91 n	ns
<sup>I</sup> COE Register MachXO2-4000ZE — 10.89 — 11.28 — 11.67 n	ns
MachXO2-7000ZE — 11.10 — 11.51 — 11.91 n	ns
MachXO2-1200ZE -0.230.23 - n	ns
Clock to Data Setup - PIO MachXO2-2000ZE -0.230.230.23 - n	ns
<sup>t</sup> SUE Input Register MachXO2-4000ZE -0.150.15 - n	ns
MachXO2-7000ZE -0.230.230.23 - n	ns
MachXO2-1200ZE 3.81 — 4.11 — 4.52 — n	ns
Clock to Data Hold - PIO Input MachXO2-2000ZE 3.81 - 4.11 - 4.52 - n	ns
t <sub>HE</sub> Register MachXO2-4000ZE 3.60 — 3.89 — 4.28 — n	ns
MachXO2-7000ZE 3.81 — 4.11 — 4.52 — n	ns
MachXO2-1200ZE 2.78 — 3.11 — 3.40 — n	ns
Clock to Data Setup - PIO MachXO2-2000ZE 2.78 - 3.11 - 3.40 - n	ns
Input Register with Data Input MachXO2-4000ZE 3.11 — 3.48 — 3.79 — n	ns
MachXO2-7000ZE 2.94 — 3.30 — 3.60 — n	ns
MachXO2-1200ZE0.29	ns
Clock to Data Hold - PIO Input MachXO2-2000ZE -0.290.290.290.290.29	ns
tH_DELE Register with Input Data Delay MachXO2-4000ZE -0.460.460.46 - n	ns
MachXO2-7000ZE -0.370.37 - n	ns
General I/O Pin Parameters (Using Primary Clock with PLL)	
MachXO2-1200ZE — 7.95 — 8.07 — 8.19 n	ns
Clock to Output – PIO Output MachXO2-2000ZE – 7.97 – 8.10 – 8.22 n	ns
ICOPLL         Register         MachXO2-4000ZE         —         7.98         —         8.10         —         8.23         n	ns
MachXO2-7000ZE — 8.02 — 8.14 — 8.26 n	ns
MachXO2-1200ZE 0.85 — 0.85 — 0.89 — n	ns
Clock to Data Setup - PIO MachXO2-2000ZE 0.84 - 0.84 - 0.86 - n	ns
Input Register         MachXO2-4000ZE         0.84         0.84         0.85         n	ns
MachXO2-7000ZE 0.83 — 0.83 — 0.81 — n	ns



#### Figure 3-9. GDDR71 Video Timing Waveforms



Figure 3-10. Receiver GDDR71\_RX. Waveforms



Figure 3-11. Transmitter GDDR71\_TX. Waveforms





## sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min.	Max.	Units
f <sub>IN</sub>	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
fout	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)		1.5625	400	MHz
f <sub>OUT2</sub>	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f <sub>VCO</sub>	PLL VCO Frequency		200	800	MHz
f <sub>PFD</sub>	Phase Detector Input Frequency		7	400	MHz
AC Characteri	stics				
t <sub>DT</sub>	Output Clock Duty Cycle	Without duty trim selected <sup>3</sup>	45	55	%
t <sub>DT_TRIM</sub> <sup>7</sup>	Edge Duty Trim Accuracy		-75	75	%
t <sub>PH</sub> <sup>4</sup>	Output Phase Accuracy		-6	6	%
	Output Cleak Pariad littar	f <sub>OUT</sub> > 100 MHz	—	150	ps p-p
		f <sub>OUT</sub> < 100 MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	f <sub>OUT</sub> > 100 MHz	—	180	ps p-p
		f <sub>OUT</sub> < 100 MHz	—	0.009	UIPP
t <sub>opjit</sub> 1,8	Output Clock Phase litter	f <sub>PFD</sub> > 100 MHz	—	160	ps p-p
	Output Clock Phase Jitter	f <sub>PFD</sub> < 100 MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	f <sub>OUT</sub> > 100 MHz	—	230	ps p-p
		f <sub>OUT</sub> < 100 MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter	f <sub>OUT</sub> > 100 MHz	—	230	ps p-p
	(Fractional-N)	f <sub>OUT</sub> < 100 MHz	—	0.12	UIPP
t <sub>SPO</sub>	Static Phase Offset	Divider ratio = integer	-120	120	ps
t <sub>W</sub>	Output Clock Pulse Width	At 90% or 10% <sup>3</sup>	0.9		ns
tLOCK <sup>2, 5</sup>	PLL Lock-in Time		—	15	ms
t <sub>UNLOCK</sub>	PLL Unlock Time		—	50	ns
+ 6	Input Clock Pariod litter	f <sub>PFD</sub> ≥ 20 MHz	—	1,000	ps p-p
ЧРЈІТ		f <sub>PFD</sub> < 20 MHz	—	0.02	UIPP
t <sub>HI</sub>	Input Clock High Time	90% to 90%	0.5	_	ns
t <sub>LO</sub>	Input Clock Low Time	10% to 10%	0.5	_	ns
t <sub>STABLE</sub> ⁵	STANDBY High to PLL Stable		—	15	ms
t <sub>RST</sub>	RST/RESETM Pulse Width		1		ns
t <sub>RSTREC</sub>	RST Recovery Time		1	—	ns
t <sub>RST_DIV</sub>	RESETC/D Pulse Width		10	—	ns
t <sub>RSTREC_DIV</sub>	RESETC/D Recovery Time		1	—	ns
t <sub>ROTATE</sub> -SETUP	PHASESTEP Setup Time		10	—	ns

## **Over Recommended Operating Conditions**



	MachXO2-2000					MachXO2-2000U	
	49 WLCSP	100 TQFP	132 csBGA	144 TQFP	256 caBGA	256 ftBGA	484 ftBGA
General Purpose I/O per Bank			1				
Bank 0	19	18	25	27	50	50	70
Bank 1	0	21	26	28	52	52	68
Bank 2	13	20	28	28	52	52	72
Bank 3	0	6	7	8	16	16	24
Bank 4	0	6	8	10	16	16	16
Bank 5	6	8	10	10	20	20	28
Total General Purpose Single-Ended I/O	38	79	104	111	206	206	278
Differential I/O per Bank							
Bank 0	7	9	13	14	25	25	35
Bank 1	0	10	13	14	26	26	34
Bank 2	6	10	14	14	26	26	36
Bank 3	0	3	3	4	8	8	12
Bank 4	0	3	4	5	8	8	8
Bank 5	3	4	5	5	10	10	14
Total General Purpose Differential I/O	16	39	52	56	103	103	139
	-		-				
Dual Function I/O	24	31	33	33	33	33	37
High-speed Differential I/O			1				
Bank 0	5	4	8	9	14	14	18
Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	4	8	9	14	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	10	14	14	14	14	18
DQS Groups			1				
Bank 1	0	1	2	2	2	2	2
VCCIO Pins							
Bank 0	2	2	3	3	4	4	10
Bank 1	0	2	3	3	4	4	10
Bank 2	1	2	3	3	4	4	10
Bank 3	0	1	1	1	1	1	3
Bank 4	0	1	1	1	2	2	4
Bank 5	1	1	1	1	1	1	3
		_					
VCC	2	2	4	4	8	8	12
GND	4	8	10	12	24	24	48
NC	0	1	1	4	1	1	105
Reserved for Configuration	1	1	1	1	v	1	1
Total Count of Bonded Pins	39	100	132	144	256	256	484



# High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100C	2112	1.2 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-5TG100C	2112	1.2 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-6TG100C	2112	1.2 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-4TG144C	2112	1.2 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-5TG144C	2112	1.2 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-6TG144C	2112	1.2 V	-6	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-4MG132C	2112	1.2 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-5MG132C	2112	1.2 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-6MG132C	2112	1.2 V	-6	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-4BG256C	2112	1.2 V	-4	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-5BG256C	2112	1.2 V	-5	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-6BG256C	2112	1.2 V	-6	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-4FTG256C	2112	1.2 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-5FTG256C	2112	1.2 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-6FTG256C	2112	1.2 V	-6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484C	2112	1.2 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-5FG484C	2112	1.2 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-6FG484C	2112	1.2 V	-6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4TG144C	4320	1.2 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-5TG144C	4320	1.2 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-6TG144C	4320	1.2 V	-6	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-4MG132C	4320	1.2 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-5MG132C	4320	1.2 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-6MG132C	4320	1.2 V	-6	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-4BG256C	4320	1.2 V	-4	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4MG184C	4320	1.2 V	-4	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5MG184C	4320	1.2 V	-5	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-6MG184C	4320	1.2 V	-6	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5BG256C	4320	1.2 V	-5	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-6BG256C	4320	1.2 V	-6	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4FTG256C	4320	1.2 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-5FTG256C	4320	1.2 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-6FTG256C	4320	1.2 V	-6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-4BG332C	4320	1.2 V	-4	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-5BG332C	4320	1.2 V	-5	Halogen-Free caBGA	332	COM



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32I	1280	2.5 V / 3.3 V	-4	Halogen-Free QFN	32	IND
LCMXO2-1200HC-5SG32I	1280	2.5 V / 3.3 V	-5	Halogen-Free QFN	32	IND
LCMXO2-1200HC-6SG32I	1280	2.5 V / 3.3 V	-6	Halogen-Free QFN	32	IND
LCMXO2-1200HC-4TG100I	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100I	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100I	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132I	1280	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132I	1280	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132I	1280	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144I	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144I	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144I	1280	2.5 V/ 3.3 V	-6	Halogen-Free TQFP	144	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256I	1280	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-5FTG256I	1280	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-6FTG256I	1280	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100I	2112	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-5TG100I	2112	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-6TG100I	2112	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-4MG132I	2112	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-5MG132I	2112	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-6MG132I	2112	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-4TG144I	2112	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-5TG144I	2112	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-6TG144I	2112	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-4BG256I	2112	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-5BG256I	2112	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-6BG256I	2112	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-4FTG256I	2112	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-5FTG256I	2112	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-6FTG256I	2112	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484I	2112	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-5FG484I	2112	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-6FG484I	2112	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	IND



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100IR11	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100IR11	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100IR11	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132IR11	1280	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132IR1 <sup>1</sup>	1280	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132IR11	1280	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144IR1 <sup>1</sup>	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144IR1 <sup>1</sup>	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144IR11	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND

1. Specifications for the "LCMXO2-1200HC-speed package IR1" are the same as the "LCMXO2-1200ZE-speed package I" devices respectively, except as specified in the R1 Device Specifications section of this data sheet.