# E · ) C Fatt ce Semiconductor Corporation - <u>LCMXO2-7000HE-4BG256C Datasheet</u>



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	858
Number of Logic Elements/Cells	6864
Total RAM Bits	245760
Number of I/O	206
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-CABGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-7000he-4bg256c

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# Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), preengineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I<sup>2</sup>C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external V<sub>CC</sub> supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V<sub>CC</sub> supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pulldown and bus-keeper features are controllable on a "per-pin" basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I<sup>2</sup>C port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE<sup>™</sup> modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.



### Figure 2-3. PFU Block Diagram



#### Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

	PFU	Block
Slice	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Table 2-1. Resources and Modes Available per Slice

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.



#### Figure 2-9. Memory Core Reset



For further information on the sysMEM EBR block, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

#### EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

#### Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram

Reset	
Clock	
Clock	

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of 1/f<sub>MAX</sub> (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-10. The reset timing rules apply to the RPReset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For more details refer to TN1201, Memory Usage Guide for MachXO2 Devices.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.



### PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Table 2-8.	ΡΙΟ	Signal	List
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Pin Name	I/О Туре	Description
CE	Input	Clock Enable
D	Input	Pin input from sysIO buffer.
INDD	Output	Register bypassed input.
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysIO Buffer
TQ	Output	Tri-state output signals to sysIO Buffer
DQSR901	Input	DQS shift 90-degree read clock
DQSW90 <sup>1</sup>	Input	DQS shift 90-degree write clock
DDRCLKPOL <sup>1</sup>	Input	DDR input register polarity control signal from DQS
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

1. Available in PIO on right edge only.

#### Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition to this functionality, the input register blocks for the PIOs on the right edge include built-in logic to interface to DDR memory.

Figure 2-12 shows the input register block for the PIOs located on the left, top and bottom edges. Figure 2-13 shows the input register block for the PIOs on the right edge.

#### Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.



More information on the input gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.

## **Output Gearbox**

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

#### Table 2-10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDRX4(8:1): D[7:0]		
GDDRX2(4:1)(IOL-A): D[3:0]		
GDDRX2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-17 shows the output gearbox block diagram.



Figure 2-18. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 Banks



Figure 2-19. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks





When implementing background programming of the on-chip Flash, care must be taken for the operation of the PLL. For devices that have two PLLs (XO2-2000U, -4000 and -7000), the system must put the RPLL (Right-side PLL) in reset state during the background Flash programming. More detailed description can be found in TN1204, MachXO2 Programming and Configuration Usage Guide.

#### Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO2 devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile Flash memory spaces. The device can be in one of two modes:

- 1. Unlocked Readback of the SRAM configuration and non-volatile Flash memory spaces is allowed.
- 2. Permanently Locked The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

#### Dual Boot

MachXO2 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the on-chip Flash. The golden image MUST reside in an external SPI Flash. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

#### Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1206, MachXO2 Soft Error Detection Usage Guide.

### TraceID

Each MachXO2 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I<sup>2</sup>C, or JTAG interfaces.

### **Density Shifting**

The MachXO2 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO2 migration files.



# MachXO2 Family Data Sheet DC and Switching Characteristics

#### March 2017

#### Data Sheet DS1035

# Absolute Maximum Ratings<sup>1, 2, 3</sup>

	MachXO2 ZE/HE (1.2 V)	MachXO2 HC (2.5 V / 3.3 V)
Supply Voltage V <sub>CC</sub>	–0.5 V to 1.32 V	0.5 V to 3.75 V
Output Supply Voltage V <sub>CCIO</sub>	–0.5 V to 3.75 V	0.5 V to 3.75 V
I/O Tri-state Voltage Applied <sup>4, 5</sup>	–0.5 V to 3.75 V	0.5 V to 3.75 V
Dedicated Input Voltage Applied <sup>4</sup>	–0.5 V to 3.75 V	0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature $(T_1)$	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

2. Compliance with the Lattice Thermal Management document is required.

3. All voltages referenced to GND.

4. Overshoot and undershoot of -2 V to (V<sub>IHMAX</sub> + 2) volts is permitted for a duration of <20 ns.

5. The dual function  $I^2C$  pins SCL and SDA are limited to -0.25 V to 3.75 V or to -0.3 V with a duration of <20 ns.

# **Recommended Operating Conditions**<sup>1</sup>

Symbol	Parameter	Min.	Max.	Units
V <sub>CC</sub> <sup>1</sup>	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V / 3.3 V Devices	2.375	3.6	V
V <sub>CCIO</sub> <sup>1, 2, 3</sup>	I/O Driver Supply Voltage	1.14	3.6	V
t <sub>JCOM</sub>	Junction Temperature Commercial Operation	0	85	°C
t <sub>JIND</sub>	Junction Temperature Industrial Operation	-40	100	°C

1. Like power supplies must be tied together. For example, if  $V_{CCIO}$  and  $V_{CC}$  are both the same voltage, they must also be the same supply.

2. See recommended voltages by I/O standard in subsequent table.

3. V<sub>CCIO</sub> pins of unused I/O banks should be connected to the V<sub>CC</sub> power supply on boards.

# Power Supply Ramp Rates<sup>1</sup>

Symbol	Parameter	Min.	Тур.	Max.	Units
t <sub>RAMP</sub>	Power supply ramp rates for all power supplies.	0.01		100	V/ms

1. Assumes monotonic ramp rates.

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# MachXO2 External Switching Characteristics – HC/HE Devices<sup>1, 2, 3, 4, 5, 6, 7</sup>

			-6 -5		-5	-4			
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Clocks	•			1	1				1
Primary Clo	ocks								
f <sub>MAX_PRI</sub> <sup>8</sup>	Frequency for Primary Clock Tree	All MachXO2 devices	_	388	_	323	_	269	MHz
t <sub>W_PRI</sub>	Clock Pulse Width for Primary Clock	All MachXO2 devices	0.5	_	0.6	_	0.7		ns
		MachXO2-256HC-HE	—	912		939	—	975	ps
		MachXO2-640HC-HE	_	844	—	871	—	908	ps
	Primary Clock Skew Within a	MachXO2-1200HC-HE	_	868	—	902	—	951	ps
<sup>I</sup> SKEW_PRI	Device	MachXO2-2000HC-HE	_	867	—	897	—	941	ps
		MachXO2-4000HC-HE	_	865	—	892	—	931	ps
		MachXO2-7000HC-HE	_	902	—	942	—	989	ps
Edge Clock		•							
f <sub>MAX_EDGE</sub> <sup>8</sup>	Frequency for Edge Clock	MachXO2-1200 and larger devices	_	400	_	333	_	278	MHz
Pin-LUT-Pin	Propagation Delay								
t <sub>PD</sub>	Best case propagation delay through one LUT-4	All MachXO2 devices	_	6.72	_	6.96		7.24	ns
General I/O	Pin Parameters (Using Primar	y Clock without PLL)		1				1	
		MachXO2-256HC-HE	_	7.13		7.30	_	7.57	ns
		MachXO2-640HC-HE	_	7.15		7.30	—	7.57	ns
	Clock to Output – PIO Output	MachXO2-1200HC-HE	_	7.44		7.64	—	7.94	ns
<sup>I</sup> CO	Register	MachXO2-2000HC-HE	_	7.46	—	7.66	—	7.96	ns
		MachXO2-4000HC-HE	_	7.51		7.71	—	8.01	ns
		MachXO2-7000HC-HE	_	7.54	—	7.75	—	8.06	ns
		MachXO2-256HC-HE	-0.06	—	-0.06	—	-0.06	—	ns
		MachXO2-640HC-HE	-0.06	—	-0.06	-	-0.06	—	ns
+	Clock to Data Setup – PIO	MachXO2-1200HC-HE	-0.17	—	-0.17	—	-0.17	—	ns
ISU	Input Register	MachXO2-2000HC-HE	-0.20	—	-0.20	—	-0.20	—	ns
		MachXO2-4000HC-HE	-0.23	—	-0.23	-	-0.23	—	ns
		MachXO2-7000HC-HE	-0.23	—	-0.23	—	-0.23	—	ns
		MachXO2-256HC-HE	1.75	—	1.95	—	2.16	—	ns
		MachXO2-640HC-HE	1.75	—	1.95	—	2.16	—	ns
+	Clock to Data Hold - PIO Input	MachXO2-1200HC-HE	1.88	—	2.12	—	2.36	—	ns
Ч	Register	MachXO2-2000HC-HE	1.89		2.13	—	2.37	—	ns
		MachXO2-4000HC-HE	1.94		2.18	—	2.43	—	ns
		MachXO2-7000HC-HE	1.98		2.23	_	2.49		ns

**Over Recommended Operating Conditions** 



		-6		-	-5 -4		4		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Generic DDF	R4 Inputs with Clock and Data A	Aligned at Pin Using PC	LK Pin f	or Clock	Input –	GDDRX	4_RX.E	CLK.Ali	gned <sup>9, 12</sup>
t <sub>DVA</sub>	Input Data Valid After ECLK		_	0.290	_	0.320	—	0.345	UI
t <sub>DVE</sub>	Input Data Hold After ECLK	MachXO2-640U,	0.739	—	0.699	—	0.703	—	UI
f <sub>DATA</sub>	DDRX4 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	756	_	630	_	524	Mbps
f <sub>DDRX4</sub>	DDRX4 ECLK Frequency	bottom side only."	—	378		315	—	262	MHz
f <sub>SCLK</sub>	SCLK Frequency			95	_	79	—	66	MHz
Generic DDF	R4 Inputs with Clock and Data Co	entered at Pin Using PCI	LK Pin fo	or Clock	Input –	GDDRX4	4_RX.EC	LK.Cen	tered <sup>9, 12</sup>
t <sub>SU</sub>	Input Data Setup Before ECLK		0.233	—	0.219	—	0.198		ns
t <sub>HO</sub>	Input Data Hold After ECLK	MachXO2-640U,	0.287	—	0.287	—	0.344	—	ns
f <sub>DATA</sub>	DDRX4 Serial Input Data Speed	MachXO2-1200/U and larger devices, bottom side only. <sup>11</sup>	_	756	_	630	_	524	Mbps
f <sub>DDRX4</sub>	DDRX4 ECLK Frequency	bottom side only.11	_	378	_	315	—	262	MHz
f <sub>SCLK</sub>	SCLK Frequency	-		95	_	79	—	66	MHz
7:1 LVDS In	puts (GDDR71_RX.ECLK.7:1) <sup>9,</sup>	12	1						L
t <sub>DVA</sub>	Input Data Valid After ECLK			0.290		0.320	—	0.345	UI
t <sub>DVE</sub>	Input Data Hold After ECLK	-	0.739	—	0.699	—	0.703	—	UI
f <sub>DATA</sub>	DDR71 Serial Input Data Speed	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only. <sup>11</sup>		756		630		524	Mbps
f <sub>DDR71</sub>	DDR71 ECLK Frequency			378		315	—	262	MHz
f <sub>CLKIN</sub>	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		_	108	_	90	_	75	MHz
Generic DDF	R Outputs with Clock and Data	Aligned at Pin Using PC	LK Pin f	for Clock	c Input –	GDDR	(1_TX.S	CLK.Ali	gned <sup>9, 12</sup>
t <sub>DIA</sub>	Output Data Invalid After CLK Output		_	0.520	_	0.550	_	0.580	ns
t <sub>DIB</sub>	Output Data Invalid Before CLK Output	All MachXO2 devices, all sides.	_	0.520	_	0.550	_	0.580	ns
f <sub>DATA</sub>	DDRX1 Output Data Speed		_	300	_	250		208	Mbps
f <sub>DDBX1</sub>	DDRX1 SCLK frequency			150	_	125		104	MHz
Generic DDF	Outputs with Clock and Data C	entered at Pin Using PC	LK Pin f	or Clock	Input –	GDDRX	1_TX.SC	LK.Cen	tered <sup>9, 12</sup>
t <sub>DVB</sub>	Output Data Valid Before CLK Output		1.210	_	1.510	_	1.870	_	ns
t <sub>DVA</sub>	Output Data Valid After CLK Output	All MachXO2 devices,	1.210	_	1.510	_	1.870	_	ns
f <sub>DATA</sub>	DDRX1 Output Data Speed	all sides.		300		250	—	208	Mbps
f <sub>DDRX1</sub>	DDRX1 SCLK Frequency (minimum limited by PLL)		_	150	_	125	_	104	MHz
Generic DDF	X2 Outputs with Clock and Data	Aligned at Pin Using P	CLK Pin	for Cloc	k Input	GDDR	X2_TX.E	CLK.Ali	gned <sup>9, 12</sup>
t <sub>DIA</sub>	Output Data Invalid After CLK Output		_	0.200	_	0.215		0.230	ns
t <sub>DIB</sub>	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/LL and		0.200		0.215		0.230	ns
f <sub>DATA</sub>	DDRX2 Serial Output Data Speed	larger devices, top side only.	_	664	_	554	_	462	Mbps
f <sub>DDRX2</sub>	DDRX2 ECLK frequency		—	332		277	—	231	MHz
f <sub>SCLK</sub>	SCLK Frequency	1	—	166	_	139	—	116	MHz



# MachXO2 External Switching Characteristics – ZE Devices<sup>1, 2, 3, 4, 5, 6, 7</sup>

			-	-3	-	-2	-	1	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Clocks			1						
Primary Cloo	cks								
f <sub>MAX_PRI</sub> <sup>8</sup>	Frequency for Primary Clock Tree	All MachXO2 devices	_	150	_	125	_	104	MHz
t <sub>W_PRI</sub>	Clock Pulse Width for Primary Clock	All MachXO2 devices	1.00	_	1.20	_	1.40	_	ns
		MachXO2-256ZE	_	1250	—	1272		1296	ps
		MachXO2-640ZE		1161		1183		1206	ps
	Primary Clock Skew Within a	MachXO2-1200ZE	_	1213		1267		1322	ps
<sup>t</sup> SKEW_PRI	Device	MachXO2-2000ZE		1204		1250		1296	ps
		MachXO2-4000ZE		1195		1233		1269	ps
		MachXO2-7000ZE		1243		1268		1296	ps
Edge Clock									
f <sub>MAX_EDGE</sub> <sup>8</sup>	Frequency for Edge Clock	MachXO2-1200 and larger devices	_	210	_	175	_	146	MHz
Pin-LUT-Pin	Propagation Delay	-	1		1			1	
t <sub>PD</sub>	Best case propagation delay through one LUT-4	All MachXO2 devices	_	9.35	_	9.78	_	10.21	ns
General I/O	Pin Parameters (Using Primary	Clock without PLL)	I	I	I	I	I		
		MachXO2-256ZE		10.46	—	10.86	—	11.25	ns
		MachXO2-640ZE	_	10.52	—	10.92		11.32	ns
	Clock to Output – PIO Output	MachXO2-1200ZE	_	11.24		11.68		12.12	ns
<sup>t</sup> CO	Register	MachXO2-2000ZE	_	11.27		11.71		12.16	ns
		MachXO2-4000ZE	_	11.28		11.78		12.28	ns
		MachXO2-7000ZE		11.22		11.76		12.30	ns
		MachXO2-256ZE	-0.21		-0.21		-0.21		ns
		MachXO2-640ZE	-0.22		-0.22		-0.22	—	ns
	Clock to Data Setup – PIO	MachXO2-1200ZE	-0.25	—	-0.25	—	-0.25	_	ns
t <sub>SU</sub>	Input Register	MachXO2-2000ZE	-0.27		-0.27		-0.27	_	ns
		MachXO2-4000ZE	-0.31		-0.31		-0.31	_	ns
		MachXO2-7000ZE	-0.33		-0.33		-0.33	_	ns
		MachXO2-256ZE	3.96	—	4.25	—	4.65	—	ns
		MachXO2-640ZE	4.01		4.31		4.71	_	ns
+	Clock to Data Hold – PIO Input	MachXO2-1200ZE	3.95		4.29	_	4.73	—	ns
Ч	Register	MachXO2-2000ZE	3.94		4.29		4.74	_	ns
		MachXO2-4000ZE	3.96		4.36		4.87	_	ns
		MachXO2-7000ZE	3.93	_	4.37	_	4.91		ns

**Over Recommended Operating Conditions** 



			-3		-2		-1		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Generic DDR	(2 Outputs with Clock and Data C	Centered at Pin Using P	CLK Pin	for Cloc	k Input –	GDDRX	2_TX.EC	CLK.Cen	tered <sup>9, 12</sup>
t <sub>DVB</sub>	Output Data Valid Before CLK Output		1.445	_	1.760	_	2.140	_	ns
t <sub>DVA</sub>	Output Data Valid After CLK Output	MachXO2-640U,	1.445	_	1.760	_	2.140	_	ns
f <sub>DATA</sub>	DDRX2 Serial Output Data Speed	MachXO2-1200/U and larger devices, top side only	_	280	_	234	_	194	Mbps
f <sub>DDRX2</sub>	DDRX2 ECLK Frequency (minimum limited by PLL)		_	140	_	117	_	97	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	70	—	59	_	49	MHz
Generic DDR	X4 Outputs with Clock and Data	Aligned at Pin Using P	CLK Pin	for Cloc	k Input	- GDDR	X4_TX.E	CLK.Ali	gned <sup>9, 12</sup>
t <sub>DIA</sub>	Output Data Invalid After CLK Output		_	0.270	_	0.300	_	0.330	ns
t <sub>DIB</sub>	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U	_	0.270	_	0.300	_	0.330	ns
f <sub>DATA</sub>	DDRX4 Serial Output Data Speed	and larger devices, top side only		420	_	352	_	292	Mbps
f <sub>DDRX4</sub>	DDRX4 ECLK Frequency		_	210	—	176	—	146	MHz
f <sub>SCLK</sub>	SCLK Frequency		_	53		44		37	MHz
Generic DDR	(4 Outputs with Clock and Data (	Centered at Pin Using P	CLK Pin	for Cloc	k Input –	GDDRX	4_TX.EC	CLK.Cen	tered <sup>9, 12</sup>
t <sub>DVB</sub>	Output Data Valid Before CLK Output		0.873	_	1.067	_	1.319	_	ns
t <sub>DVA</sub>	Output Data Valid After CLK Output	MachXO2-640U,	0.873	_	1.067	_	1.319	_	ns
f <sub>DATA</sub>	DDRX4 Serial Output Data Speed	and larger devices,	_	420	_	352	_	292	Mbps
f <sub>DDRX4</sub>	DDRX4 ECLK Frequency (minimum limited by PLL)		_	210	_	176	_	146	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	53	—	44	_	37	MHz
7:1 LVDS Ou	tputs – GDDR71_TX.ECLK.7:1	9, 12							
t <sub>DIB</sub>	Output Data Invalid Before CLK Output		_	0.240	—	0.270	_	0.300	ns
t <sub>DIA</sub>	Output Data Invalid After CLK Output	MachXO2-640U.	_	0.240	_	0.270	_	0.300	ns
f <sub>DATA</sub>	DDR71 Serial Output Data Speed	MachXO2-1200/U and larger devices,	_	420	_	352	_	292	Mbps
f <sub>DDR71</sub>	DDR71 ECLK Frequency	top side only.	—	210	—	176	—	146	MHz
fclkout	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		_	60	_	50	_	42	MHz









				MachX	02-4000			
	84 QFN	132 csBGA	144 TQFP	184 csBGA	256 caBGA	256 ftBGA	332 caBGA	484 fpBGA
General Purpose I/O per Bank								
Bank 0	27	25	27	37	50	50	68	70
Bank 1	10	26	29	37	52	52	68	68
Bank 2	22	28	29	39	52	52	70	72
Bank 3	0	7	9	10	16	16	24	24
Bank 4	9	8	10	12	16	16	16	16
Bank 5	0	10	10	15	20	20	28	28
Total General Purpose Single Ended I/O	68	104	114	150	206	206	274	278
Differential I/O per Bank								
Bank 0	13	13	14	18	25	25	34	35
Bank 1	4	13	14	18	26	26	34	34
Bank 2	11	14	14	19	26	26	35	36
Bank 3	0	3	4	4	8	8	12	12
Bank 4	4	4	5	6	8	8	8	8
Bank 5	0	5	5	7	10	10	14	14
Total General Purpose Differential I/O	32	52	56	72	103	103	137	139
Dual Function I/O	28	37	37	37	37	37	37	37
High-speed Differential I/O								
Bank 0	8	8	9	8	18	18	18	18
Gearboxes					-			-
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	8	8	9	9	18	18	18	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	11	14	14	12	18	18	18	18
DQS Groups								
Bank 1	1	2	2	2	2	2	2	2
VCCIO Pins								
Bank 0	3	3	3	3	4	4	4	10
Bank 1	1	3	3	3	4	4	4	10
Bank 2	2	3	3	3	4	4	4	10
Bank 3	1	1	1	1	1	1	2	3
Bank 4	1	1	1	1	2	2	1	4
Bank 5	1	1	1	1	1	1	2	3
		1						
VCC	4	4	4	4	8	8	8	12
GND	4	10	12	16	24	24	27	48
NC	1	1	1	1	1	1	5	105
Reserved for configuration	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	84	132	144	184	256	256	332	484





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	MachXO2-7000					
	144 TQFP	256 caBGA	256 ftBGA	332 caBGA	400 caBGA	484 fpBGA
General Purpose I/O per Bank						
Bank 0	27	50	50	68	83	82
Bank 1	29	52	52	70	84	84
Bank 2	29	52	52	70	84	84
Bank 3	9	16	16	24	28	28
Bank 4	10	16	16	16	24	24
Bank 5	10	20	20	30	32	32
Total General Purpose Single Ended I/O	114	206	206	278	335	334
Differential I/O per Bank						
Bank 0	14	25	25	34	42	41
Bank 1	14	26	26	35	42	42
Bank 2	14	26	26	35	42	42
Bank 3	4	8	8	12	14	14
Bank 4	5	8	8	8	12	12
Bank 5	5	10	10	15	16	16
Total General Purpose Differential I/O	56	103	103	139	168	167
Dual Function I/O	37	37	37	37	37	37
High-speed Differential I/O		•				
Bank 0	9	20	20	21	21	21
Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	9	20	20	21	21	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	14	20	20	21	21	21
DQS Groups						
Bank 1	2	2	2	2	2	2
VCCIO Pins						
Bank 0	3	4	4	4	5	10
Bank 1	3	4	4	4	5	10
Bank 2	3	4	4	4	5	10
Bank 3	1	1	1	2	2	3
Bank 4	1	2	2	1	2	4
Bank 5	1	1	1	2	2	3
VCC	4	8	8	8	10	12
GND	12	24	24	27	33	48
NC	1	1	1	1	0	49
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	144	256	256	332	400	484



# MachXO2 Family Data Sheet Ordering Information

March 2017

Data Sheet DS1035

# MachXO2 Part Number Description



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# High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32C	256	2.5 V / 3.3 V	-4	Halogen-Free QFN	32	COM
LCMXO2-256HC-5SG32C	256	2.5 V / 3.3 V	-5	Halogen-Free QFN	32	COM
LCMXO2-256HC-6SG32C	256	2.5 V / 3.3 V	-6	Halogen-Free QFN	32	COM
LCMXO2-256HC-4SG48C	256	2.5 V / 3.3 V	-4	Halogen-Free QFN	48	COM
LCMXO2-256HC-5SG48C	256	2.5 V / 3.3 V	-5	Halogen-Free QFN	48	COM
LCMXO2-256HC-6SG48C	256	2.5 V / 3.3 V	-6	Halogen-Free QFN	48	COM
LCMXO2-256HC-4UMG64C	256	2.5 V / 3.3 V	-4	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-5UMG64C	256	2.5 V / 3.3 V	-5	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-6UMG64C	256	2.5 V / 3.3 V	-6	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-4TG100C	256	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-256HC-5TG100C	256	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-256HC-6TG100C	256	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-256HC-4MG132C	256	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-256HC-5MG132C	256	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-256HC-6MG132C	256	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48C	640	2.5 V / 3.3 V	-4	Halogen-Free QFN	48	COM
LCMXO2-640HC-5SG48C	640	2.5 V / 3.3 V	-5	Halogen-Free QFN	48	COM
LCMXO2-640HC-6SG48C	640	2.5 V / 3.3 V	-6	Halogen-Free QFN	48	COM
LCMXO2-640HC-4TG100C	640	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-640HC-5TG100C	640	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-640HC-6TG100C	640	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-640HC-4MG132C	640	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-640HC-5MG132C	640	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-640HC-6MG132C	640	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144C	640	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-5TG144C	640	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-6TG144C	640	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	COM



### Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32I	256	1.2 V	-1	Halogen-Free QFN	32	IND
LCMXO2-256ZE-2SG32I	256	1.2 V	-2	Halogen-Free QFN	32	IND
LCMXO2-256ZE-3SG32I	256	1.2 V	-3	Halogen-Free QFN	32	IND
LCMXO2-256ZE-1UMG64I	256	1.2 V	-1	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-2UMG64I	256	1.2 V	-2	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-3UMG64I	256	1.2 V	-3	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-1TG100I	256	1.2 V	-1	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-2TG100I	256	1.2 V	-2	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-3TG100I	256	1.2 V	-3	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-1MG132I	256	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-2MG132I	256	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-3MG132I	256	1.2 V	-3	Halogen-Free csBGA	132	IND
						-
Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100I	640	1.2 V	-1	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-2TG100I	640	1.2 V	-2	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-3TG100I	640	1.2 V	-3	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-1MG132I	640	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-2MG132I	640	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-3MG132I	640	1.2 V	-3	Halogen-Free csBGA	132	IND
	-	- 1	r	1	1	1
Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1UWG25ITR <sup>1</sup>	1280	1.2 V	-1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR50	<sup>3</sup> 1280	1.2 V	-1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR1K	<sup>2</sup> 1280	1.2 V	-1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1SG32I	1280	1.2 V	-1	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-2SG32I	1280	1.2 V	-2	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-3SG32I	1280	1.2 V	-3	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-1TG100I	1280	1.2 V	-1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100I	1280	1.2 V	-2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100I	1280	1.2 V	-3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132I	1280	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132I	1280	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132I	1280	1.2 V	-3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144I	1280	1.2 V	-1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144I	1280	1.2 V	-2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144I	1280	1.2 V	-3	Halogen-Free TQFP	144	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.

2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.

3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4MG132I	4320	1.2 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-5MG132I	4320	1.2 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-6MG132I	4320	1.2 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-4TG144I	4320	1.2 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-5TG144I	4320	1.2 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-6TG144I	4320	1.2 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-4MG184I	4320	1.2 V	-4	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-5MG184I	4320	1.2 V	-5	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-6MG184I	4320	1.2 V	-6	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-4BG256I	4320	1.2 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-5BG256I	4320	1.2 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-6BG256I	4320	1.2 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-4FTG256I	4320	1.2 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-5FTG256I	4320	1.2 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-6FTG256I	4320	1.2 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-4BG332I	4320	1.2 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-5BG332I	4320	1.2 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-6BG332I	4320	1.2 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-4FG484I	4320	1.2 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-5FG484I	4320	1.2 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-6FG484I	4320	1.2 V	-6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144I	6864	1.2 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-5TG144I	6864	1.2 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-6TG144I	6864	1.2 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-4BG256I	6864	1.2 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-5BG256I	6864	1.2 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-6BG256I	6864	1.2 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-4FTG256I	6864	1.2 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-5FTG256I	6864	1.2 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-6FTG256I	6864	1.2 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-4BG332I	6864	1.2 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-5BG332I	6864	1.2 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-6BG332I	6864	1.2 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-4FG484I	6864	1.2 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-5FG484I	6864	1.2 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-6FG484I	6864	1.2 V	-6	Halogen-Free fpBGA	484	IND



Date	Version	Section	Change Summary
January 2013	02.0	Introduction	Updated the total number IOs to include JTAGENB.
		Architecture	Supported Output Standards table – Added 3.3 $\rm V_{\rm CCIO}$ (Typ.) to LVDS row.
			Changed SRAM CRC Error Detection to Soft Error Detection.
		DC and Switching Characteristics	Power Supply Ramp Rates table – Updated Units column for t <sub>RAMP</sub> symbol.
			Added new Maximum sysIO Buffer Performance table.
			sysCLOCK PLL Timing table – Updated Min. column values for $f_{IN}$ ,
			$f_{OUT},f_{OUT2}$ and $f_{PFD}$ parameters. Added $t_{SPO}$ parameter. Updated footnote 6.
			MachXO2 Oscillator Output Frequency table – Updated symbol name for t <sub>STABLEOSC</sub> .
			DC Electrical Characteristics table – Updated conditions for ${\rm I}_{\rm IL,}~{\rm I}_{\rm IH}$ symbols.
			Corrected parameters tDQVBS and tDQVAS
			Corrected MachXO2 ZE parameters tDVADQ and tDVEDQ
		Pinout Information	Included the MachXO2-4000HE 184 csBGA package.
		Ordering Information	Updated part number.
April 2012	01.9	Architecture	Removed references to TN1200.
		Ordering Information	Updated the Device Status portion of the MachXO2 Part Number Description to include the 50 parts per reel for the WLCSP package.
			Added new part number and footnote 2 for LCMXO2-1200ZE- 1UWG25ITR50.
			Updated footnote 1 for LCMXO2-1200ZE-1UWG25ITR.
		Supplemental Information	Removed references to TN1200.
March 2012	01.8	Introduction	Added 32 QFN packaging information to Features bullets and MachXO2 Family Selection Guide table.
		DC and Switching Characteristics	Changed 'STANDBY' to 'USERSTDBY' in Standby Mode timing dia- gram.
		Pinout Information	Removed footnote from Pin Information Summary tables.
			Added 32 QFN package to Pin Information Summary table.
		Ordering Information	Updated Part Number Description and Ordering Information tables for 32 QFN package.
			Updated topside mark diagram in the Ordering Information section.