# E · K Hat ice Semiconductor Corporation - <u>LCMXO2-7000HE-4BG332I Datasheet</u>



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	858
Number of Logic Elements/Cells	6864
Total RAM Bits	245760
Number of I/O	278
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	332-FBGA
Supplier Device Package	332-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-7000he-4bg332i

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# Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), preengineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I<sup>2</sup>C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external V<sub>CC</sub> supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V<sub>CC</sub> supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pulldown and bus-keeper features are controllable on a "per-pin" basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I<sup>2</sup>C port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE<sup>™</sup> modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.



## Figure 2-3. PFU Block Diagram



## Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

	PFU Block					
Slice	Resources	Modes				
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM				
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM				
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM				
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM				

Table 2-1. Resources and Modes Available per Slice

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.



## Figure 2-5. Primary Clocks for MachXO2 Devices



Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO2 External Switching Characteristics table.



 Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

#### Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

#### **RAM Initialization and ROM Operation**

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO2 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

#### Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

## Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.



#### Figure 2-8. sysMEM Memory Primitives



#### Table 2-6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE <sup>1</sup>	Output Clock Enable	Active High
RST	Reset	Active High
BE <sup>1</sup>	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	
DI	Data In	_
DO	Data Out	_
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	_
FF	FIFO RAM Full Flag	_
AEF	FIFO RAM Almost Empty Flag	_
EF	FIFO RAM Empty Flag	_
RPRST	FIFO RAM Read Pointer Reset	_

1. Optional signals.

2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.

3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.

4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).

5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.



# Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO2 devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO2 devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

The MachXO2-640U, MachXO2-1200/U and higher density devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these higher density devices have on-chip differential termination and also provide PCI support.



## Figure 2-17. Output Gearbox



More information on the output gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.



## Table 2-11. I/O Support Device by Device

	MachXO2-256, MachXO2-640	MachXO2-640U, MachXO2-1200	MachXO2-1200U MachXO2-2000/U, MachXO2-4000, MachXO2-7000
Number of I/O Banks	4	4	6
		Single-ended (all I/O banks)	Single-ended (all I/O banks)
Tupo of Input Pufforo	Single-ended (all I/O banks)	Differential Receivers (all I/O	Differential Receivers (all I/O
	Differential Receivers (all I/O banks)	Differential input termination (bottom side)	Differential input termination (bottom side)
Turses of Output Duffers	Single-ended buffers with	Single-ended buffers with complementary outputs (all I/O banks)	Single-ended buffers with complementary outputs (all I/O banks)
Types of Output Bullers	banks)	Differential buffers with true LVDS outputs (50% on top side)	Differential buffers with true LVDS outputs (50% on top side)
Differential Output Emulation Capability	All I/O banks	All I/O banks	All I/O banks
PCI Clamp Support	No	Clamp on bottom side only	Clamp on bottom side only

## Table 2-12. Supported Input Standards

		V	CCIO (Ty	p.)	
Input Standard	3.3 V	2.5 V	1.8 V	1.5	1.2 V
Single-Ended Interfaces					
LVTTL	✓	<b>√</b> <sup>2</sup>	<b>√</b> <sup>2</sup>	<b>√</b> <sup>2</sup>	
LVCMOS33	✓	<b>√</b> <sup>2</sup>	<b>√</b> <sup>2</sup>	<b>√</b> <sup>2</sup>	
LVCMOS25	<b>√</b> <sup>2</sup>	✓	<b>√</b> <sup>2</sup>	<b>√</b> <sup>2</sup>	
LVCMOS18	<b>√</b> <sup>2</sup>	<b>√</b> <sup>2</sup>	✓	<b>√</b> <sup>2</sup>	
LVCMOS15	<b>√</b> <sup>2</sup>	<b>√</b> <sup>2</sup>	<b>√</b> <sup>2</sup>	~	<b>√</b> <sup>2</sup>
LVCMOS12	<b>√</b> <sup>2</sup>	<b>√</b> <sup>2</sup>	<b>√</b> <sup>2</sup>	<b>√</b> <sup>2</sup>	✓
PCI <sup>1</sup>	✓				
SSTL18 (Class I, Class II)	✓	✓	✓		
SSTL25 (Class I, Class II)	✓	✓			
HSTL18 (Class I, Class II)	✓	✓	✓		
Differential Interfaces		•			
LVDS	✓	✓			
BLVDS, MVDS, LVPECL, RSDS	✓	✓			
MIPI <sup>3</sup>	✓	✓			
Differential SSTL18 Class I, II	✓	✓	✓		
Differential SSTL25 Class I, II	✓	✓			
Differential HSTL18 Class I, II	✓	~	✓		

1. Bottom banks of MachXO2-640U, MachXO2-1200/U and higher density devices only.

2. Reduced functionality. Refer to TN1202, MachXO2 sysIO Usage Guide for more detail.

3. These interfaces can be emulated with external resistors in all devices.



## Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  - Watchdog timer
  - Clear timer on compare match
  - Fast PWM
  - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- · Stand-alone mode with preloaded control registers and direct reset input

## Figure 2-23. Timer/Counter Block Diagram



Table 2-17. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	0	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	0	Timer counter output signal



# Static Supply Current – ZE Devices<sup>1, 2, 3, 6</sup>

Symbol	Parameter	Device	Typ.⁴	Units
	Core Power Supply	LCMXO2-256ZE	18	μΑ
		LCMXO2-640ZE	28	μΑ
I <sub>CC</sub>		LCMXO2-1200ZE	56	μΑ
		LCMXO2-2000ZE	80	μΑ
		LCMXO2-4000ZE	124	μΑ
		LCMXO2-7000ZE	189	μA
Iccio	Bank Power Supply⁵ V <sub>CCIO</sub> = 2.5 V	All devices	1	μΑ

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.

Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V<sub>CCIO</sub> or GND, on-chip oscillator is off, on-chip PLL is off. To estimate the impact of turning each of these items on, please refer to the following table or for more detail with your specific design use the Power Calculator tool.

3. Frequency = 0 MHz.

4.  $T_J = 25$  °C, power supplies at nominal voltage.

5. Does not include pull-up/pull-down.

6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

# Static Power Consumption Contribution of Different Components – ZE Devices

The table below can be used for approximating static power consumption. For a more accurate power analysis for your design please use the Power Calculator tool.

Symbol	Parameter	Тур.	Units
I <sub>DCBG</sub>	Bandgap DC power contribution	101	μΑ
IDCPOR	POR DC power contribution	38	μΑ
IDCIOBANKCONTROLLER	DC power contribution per I/O bank controller	143	μΑ



# Typical Building Block Function Performance – ZE Devices<sup>1</sup>

## Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–3 Timing	Units
Basic Functions		
16-bit decoder	13.9	ns
4:1 MUX	10.9	ns
16:1 MUX	12.0	ns

## **Register-to-Register Performance**

Function	–3 Timing	Units
Basic Functions		ŀ
16:1 MUX	191	MHz
16-bit adder	134	MHz
16-bit counter	148	MHz
64-bit counter	77	MHz
Embedded Memory Functions	·	
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	90	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	214	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

# **Derating Logic Timing**

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.





			_	6	_	5	_	4	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
		MachXO2-256HC-HE	1.42	_	1.59	_	1.96	_	ns
		MachXO2-640HC-HE	1.41	_	1.58	_	1.96	_	ns
	Clock to Data Setup – PIO	MachXO2-1200HC-HE	1.63	_	1.79	_	2.17	_	ns
<sup>I</sup> SU_DEL	Delav	MachXO2-2000HC-HE	1.61	_	1.76	_	2.13	_	ns
		MachXO2-4000HC-HE	1.66	_	1.81	_	2.19	_	ns
		MachXO2-7000HC-HE	1.53	_	1.67		2.03		ns
		MachXO2-256HC-HE	-0.24	_	-0.24		-0.24		ns
		MachXO2-640HC-HE	-0.23	_	-0.23	_	-0.23	_	ns
+	Clock to Data Hold – PIO Input	MachXO2-1200HC-HE	-0.24	_	-0.24	_	-0.24	_	ns
'H_DEL	Register with Input Data Delay	MachXO2-2000HC-HE	-0.23	_	-0.23		-0.23		ns
		MachXO2-4000HC-HE	-0.25	_	-0.25		-0.25		ns
		MachXO2-7000HC-HE	-0.21		-0.21		-0.21		ns
f <sub>MAX_IO</sub>	Clock Frequency of I/O and PFU Register	All MachXO2 devices		388	_	323	_	269	MHz
General I/O	Pin Parameters (Using Edge C	lock without PLL)							
		MachXO2-1200HC-HE	_	7.53		7.76		8.10	ns
+	Clock to Output – PIO Output	MachXO2-2000HC-HE		7.53		7.76		8.10	ns
COE	Register	MachXO2-4000HC-HE		7.45		7.68		8.00	ns
		MachXO2-7000HC-HE		7.53		7.76		8.10	ns
	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	-0.19	_	-0.19	_	-0.19	_	ns
		MachXO2-2000HC-HE	-0.19	_	-0.19	_	-0.19	_	ns
ISUE		MachXO2-4000HC-HE	-0.16	_	-0.16	_	-0.16	_	ns
		MachXO2-7000HC-HE	-0.19	_	-0.19		-0.19		ns
		MachXO2-1200HC-HE	1.97	_	2.24	_	2.52	_	ns
	Clock to Data Hold – PIO Input	MachXO2-2000HC-HE	1.97	_	2.24	_	2.52	_	ns
ΉE	Register	MachXO2-4000HC-HE	1.89	_	2.16	_	2.43	_	ns
		MachXO2-7000HC-HE	1.97	_	2.24	_	2.52	_	ns
		MachXO2-1200HC-HE	1.56	_	1.69	_	2.05	_	ns
	Clock to Data Setup – PIO	MachXO2-2000HC-HE	1.56	_	1.69	_	2.05	_	ns
<sup>I</sup> SU_DELE	Delay	MachXO2-4000HC-HE	1.74	_	1.88	_	2.25	_	ns
	Donay	MachXO2-7000HC-HE	1.66	_	1.81	_	2.17	_	ns
		MachXO2-1200HC-HE	-0.23	_	-0.23	_	-0.23	_	ns
+	Clock to Data Hold – PIO Input	MachXO2-2000HC-HE	-0.23	_	-0.23		-0.23		ns
'H_DELE	Register with Input Data Delay	MachXO2-4000HC-HE	-0.34	_	-0.34		-0.34		ns
		MachXO2-7000HC-HE	-0.29	_	-0.29		-0.29		ns
General I/O	Pin Parameters (Using Primary	y Clock with PLL)							
		MachXO2-1200HC-HE	—	5.97		6.00		6.13	ns
	Clock to Output – PIO Output	MachXO2-2000HC-HE		5.98		6.01		6.14	ns
COPLL	Register	MachXO2-4000HC-HE		5.99		6.02		6.16	ns
		MachXO2-7000HC-HE		6.02		6.06		6.20	ns
		MachXO2-1200HC-HE	0.36	—	0.36	—	0.65	—	ns
+.	Clock to Data Setup – PIO	MachXO2-2000HC-HE	0.36	—	0.36	—	0.63	—	ns
SUPLL	Input Register	MachXO2-4000HC-HE	0.35	—	0.35	—	0.62	—	ns
		MachXO2-7000HC-HE	0.34	_	0.34	—	0.59	—	ns
	1	•			•		•		



# MachXO2 Oscillator Output Frequency

Symbol	Parameter	Min.	Тур.	Max	Units
f	Oscillator Output Frequency (Commercial Grade Devices, 0 to 85°C)		133	140.315	MHz
MAX	Oscillator Output Frequency (Industrial Grade Devices, -40 °C to 100 °C)	124.355	133	141.645	MHz
t <sub>DT</sub>	Output Clock Duty Cycle	43	50	57	%
t <sub>OPJIT</sub> 1	Output Clock Period Jitter	0.01	0.012	0.02	UIPP
t <sub>STABLEOSC</sub>	STDBY Low to Oscillator Stable	0.01	0.05	0.1	μs

1. Output Clock Period Jitter specified at 133 MHz. The values for lower frequencies will be smaller UIPP. The typical value for 133 MHz is 95 ps and for 2.08 MHz the typical value is 1.54 ns.

# MachXO2 Standby Mode Timing – HC/HE Devices

Symbol	Parameter	Device	Min.	Тур.	Max	Units
t <sub>PWRDN</sub>	USERSTDBY High to Stop	All	_	—	9	ns
		LCMXO2-256		—		μs
		LCMXO2-640		—		μs
		LCMXO2-640U		—		μs
	USERSTDBY Low to Power Up	LCMXO2-1200	20	—	50	μs
t <sub>PWRUP</sub>		LCMXO2-1200U		—		μs
		LCMXO2-2000		—		μs
		LCMXO2-2000U		—		μs
		LCMXO2-4000		—		μs
		LCMXO2-7000		—		μs
t <sub>WSTDBY</sub>	USERSTDBY Pulse Width	All	18	_	—	ns



# MachXO2 Standby Mode Timing – ZE Devices

Symbol	Parameter	Device	Min.	Тур.	Max	Units
t <sub>PWRDN</sub>	USERSTDBY High to Stop	All	_		13	ns
		LCMXO2-256		_		μs
		LCMXO2-640		_		μs
t <sub>PWRUP</sub>	USERSTDBY Low to Power Up	LCMXO2-1200	20	_	50	μs
		LCMXO2-2000		_		μs
		LCMXO2-4000		_		μs
		LCMXO2-7000		_		μs
t <sub>WSTDBY</sub>	USERSTDBY Pulse Width	All	19	_	_	ns
t <sub>BNDGAPSTBL</sub>	USERSTDBY High to Bandgap Stable	All			15	ns



# sysCONFIG Port Timing Specifications

Symbol	Pa	irameter	Min.	Max.	Units
All Configuration Modes	1				
t <sub>PRGM</sub>	PROGRAMN low p	ulse accept	55		ns
t <sub>PRGMJ</sub>	PROGRAMN low p	ulse rejection	—	25	ns
t <sub>INITL</sub>	INITN low time	LCMXO2-256	—	30	μs
		LCMXO2-640	—	35	μs
		LCMXO2-640U/ LCMXO2-1200	_	55	μs
		LCMXO2-1200U/ LCMXO2-2000	—	70	μs
		LCMXO2-2000U/ LCMXO2-4000	—	105	μs
		LCMXO2-7000	—	130	μs
t <sub>DPPINIT</sub>	PROGRAMN low to	D INITN Iow	—	150	ns
t <sub>DPPDONE</sub>	PROGRAMN low to	DONE low	—	150	ns
t <sub>IODISS</sub>	PROGRAMN low to	o I/O disable	—	120	ns
Slave SPI	·				
f <sub>MAX</sub>	CCLK clock frequency		—	66	MHz
t <sub>ССLКН</sub>	CCLK clock pulse width high		7.5	—	ns
t <sub>CCLKL</sub>	CCLK clock pulse v	width low	7.5	_	ns
t <sub>STSU</sub>	CCLK setup time		2	—	ns
t <sub>STH</sub>	CCLK hold time		0	—	ns
t <sub>STCO</sub>	CCLK falling edge	to valid output	—	10	ns
t <sub>STOZ</sub>	CCLK falling edge	to valid disable	—	10	ns
t <sub>STOV</sub>	CCLK falling edge	to valid enable	—	10	ns
t <sub>SCS</sub>	Chip select high tim	ne	25	—	ns
t <sub>SCSS</sub>	Chip select setup ti	me	3	—	ns
t <sub>SCSH</sub>	Chip select hold tim	ne	3	—	ns
Master SPI					
f <sub>MAX</sub>	MCLK clock freque	ncy	—	133	MHz
t <sub>MCLKH</sub>	MCLK clock pulse v	MCLK clock pulse width high		—	ns
t <sub>MCLKL</sub>	MCLK clock pulse v	width low	3.75	—	ns
t <sub>STSU</sub>	MCLK setup time		5		ns
t <sub>STH</sub>	MCLK hold time		1		ns
t <sub>CSSPI</sub>	INITN high to chip	select low	100	200	ns
t <sub>MCLK</sub>	INITN high to first N	MCLK edge	0.75	1	μs



	MachXO2-2000						MachXO2-2000U
	49 WLCSP	100 TQFP	132 csBGA	144 TQFP	256 caBGA	256 ftBGA	484 ftBGA
General Purpose I/O per Bank			1				
Bank 0	19	18	25	27	50	50	70
Bank 1	0	21	26	28	52	52	68
Bank 2	13	20	28	28	52	52	72
Bank 3	0	6	7	8	16	16	24
Bank 4	0	6	8	10	16	16	16
Bank 5	6	8	10	10	20	20	28
Total General Purpose Single-Ended I/O	38	79	104	111	206	206	278
Differential I/O per Bank							
Bank 0	7	9	13	14	25	25	35
Bank 1	0	10	13	14	26	26	34
Bank 2	6	10	14	14	26	26	36
Bank 3	0	3	3	4	8	8	12
Bank 4	0	3	4	5	8	8	8
Bank 5	3	4	5	5	10	10	14
Total General Purpose Differential I/O	16	39	52	56	103	103	139
	-		_				
Dual Function I/O	24	31	33	33	33	33	37
High-speed Differential I/O	•	•	•			•	
Bank 0	5	4	8	9	14	14	18
Gearboxes						•	
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	4	8	9	14	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	10	14	14	14	14	18
DQS Groups			1				
Bank 1	0	1	2	2	2	2	2
VCCIO Pins							
Bank 0	2	2	3	3	4	4	10
Bank 1	0	2	3	3	4	4	10
Bank 2	1	2	3	3	4	4	10
Bank 3	0	1	1	1	1	1	3
Bank 4	0	1	1	1	2	2	4
Bank 5	1	1	1	1	1	1	3
VCC	2	2	4	4	8	8	12
GND	4	8	10	12	24	24	48
NC	0	1	1	4	1	1	105
Reserved for Configuration	1	1	1	1	v	1	1
Total Count of Bonded Pins	39	100	132	144	256	256	484



# **Ordering Information**

MachXO2 devices have top-side markings, for commercial and industrial grades, as shown below:



Notes:

- 1. Markings are abbreviated for small packages.
- 2. See PCN 05A-12 for information regarding a change to the top-side mark logo.



## Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32I	256	1.2 V	-1	Halogen-Free QFN	32	IND
LCMXO2-256ZE-2SG32I	256	1.2 V	-2	Halogen-Free QFN	32	IND
LCMXO2-256ZE-3SG32I	256	1.2 V	-3	Halogen-Free QFN	32	IND
LCMXO2-256ZE-1UMG64I	256	1.2 V	-1	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-2UMG64I	256	1.2 V	-2	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-3UMG64I	256	1.2 V	-3	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-1TG100I	256	1.2 V	-1	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-2TG100I	256	1.2 V	-2	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-3TG100I	256	1.2 V	-3	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-1MG132I	256	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-2MG132I	256	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-3MG132I	256	1.2 V	-3	Halogen-Free csBGA	132	IND
						-
Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100I	640	1.2 V	-1	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-2TG100I	640	1.2 V	-2	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-3TG100I	640	1.2 V	-3	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-1MG132I	640	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-2MG132I	640	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-3MG132I	640	1.2 V	-3	Halogen-Free csBGA	132	IND
	-	- 1	r	1	1	1
Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1UWG25ITR <sup>1</sup>	1280	1.2 V	-1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR50	<sup>3</sup> 1280	1.2 V	-1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR1K	<sup>2</sup> 1280	1.2 V	-1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1SG32I	1280	1.2 V	-1	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-2SG32I	1280	1.2 V	-2	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-3SG32I	1280	1.2 V	-3	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-1TG100I	1280	1.2 V	-1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100I	1280	1.2 V	-2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100I	1280	1.2 V	-3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132I	1280	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132I	1280	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132I	1280	1.2 V	-3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144I	1280	1.2 V	-1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144I	1280	1.2 V	-2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144I	1280	1.2 V	-3	Halogen-Free TQFP	144	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.

2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.

3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.



# High Performance Industrial Grade Devices Without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100I	2112	1.2 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-5TG100I	2112	1.2 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-6TG100I	2112	1.2 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-2000HE-4MG132I	2112	1.2 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-5MG132I	2112	1.2 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-6MG132I	2112	1.2 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-2000HE-4TG144I	2112	1.2 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-5TG144I	2112	1.2 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-6TG144I	2112	1.2 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-2000HE-4BG256I	2112	1.2 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-5BG256I	2112	1.2 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-6BG256I	2112	1.2 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-2000HE-4FTG256I	2112	1.2 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-5FTG256I	2112	1.2 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HE-6FTG256I	2112	1.2 V	-6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484I	2112	1.2 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-5FG484I	2112	1.2 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHE-6FG484I	2112	1.2 V	-6	Halogen-Free fpBGA	484	IND



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4MG132I	4320	1.2 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-5MG132I	4320	1.2 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-6MG132I	4320	1.2 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-4TG144I	4320	1.2 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-5TG144I	4320	1.2 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-6TG144I	4320	1.2 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-4MG184I	4320	1.2 V	-4	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-5MG184I	4320	1.2 V	-5	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-6MG184I	4320	1.2 V	-6	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-4BG256I	4320	1.2 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-5BG256I	4320	1.2 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-6BG256I	4320	1.2 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-4FTG256I	4320	1.2 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-5FTG256I	4320	1.2 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-6FTG256I	4320	1.2 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-4BG332I	4320	1.2 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-5BG332I	4320	1.2 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-6BG332I	4320	1.2 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-4FG484I	4320	1.2 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-5FG484I	4320	1.2 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-6FG484I	4320	1.2 V	-6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144I	6864	1.2 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-5TG144I	6864	1.2 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-6TG144I	6864	1.2 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-4BG256I	6864	1.2 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-5BG256I	6864	1.2 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-6BG256I	6864	1.2 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-4FTG256I	6864	1.2 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-5FTG256I	6864	1.2 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-6FTG256I	6864	1.2 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-4BG332I	6864	1.2 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-5BG332I	6864	1.2 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-6BG332I	6864	1.2 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-4FG484I	6864	1.2 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-5FG484I	6864	1.2 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-6FG484I	6864	1.2 V	-6	Halogen-Free fpBGA	484	IND



Date	Version	Section	Change Summary
February 2012	01.7	All	Updated document with new corporate logo.
	01.6	—	Data sheet status changed from preliminary to final.
		Introduction	MachXO2 Family Selection Guide table – Removed references to 49-ball WLCSP.
		DC and Switching Characteristics	Updated Flash Download Time table.
			Modified Storage Temperature in the Absolute Maximum Ratings section.
			Updated I <sub>DK</sub> max in Hot Socket Specifications table.
			Modified Static Supply Current tables for ZE and HC/HE devices.
			Updated Power Supply Ramp Rates table.
			Updated Programming and Erase Supply Current tables.
			Updated data in the External Switching Characteristics table.
			Corrected Absolute Maximum Ratings for Dedicated Input Voltage Applied for LCMXO2 HC.
			DC Electrical Characteristics table – Minor corrections to conditions for $\mathbf{I}_{IL},  \mathbf{I}_{IH.}$
		Pinout Information	Removed references to 49-ball WLCSP.
			Signal Descriptions table – Updated description for GND, VCC, and VCCIOx.
			Updated Pin Information Summary table – Number of VCCIOs, GNDs, VCCs, and Total Count of Bonded Pins for MachXO2-256, 640, and 640U and Dual Function I/O for MachXO2-4000 332caBGA.
		Ordering Information	Removed references to 49-ball WLCSP
August 2011	01.5	DC and Switching Characteristics	Updated ESD information.
		Ordering Information	Updated footnote for ordering WLCSP devices.
	01.4	Architecture	Updated information in Clock/Control Distribution Network and sys- CLOCK Phase Locked Loops (PLLs).
		DC and Switching Characteristics	Updated ${\rm I}_{\rm IL}$ and ${\rm I}_{\rm IH}$ conditions in the DC Electrical Characteristics table.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Updated Pin Information Summary table: Dual Function I/O, DQS Groups Bank 1, Total General Purpose Single-Ended I/O, Differential I/O Per Bank, Total Count of Bonded Pins, Gearboxes.
			Added column of data for MachXO2-2000 49 WLCSP.
		Ordering Information	Updated R1 Device Specifications text section with information on migration from MachXO2-1200-R1 to Standard (non-R1) devices.
			Corrected Supply Voltage typo for part numbers: LCMX02-2000UHE- 4FG484I, LCMX02-2000UHE-5FG484I, LCMX02-2000UHE- 6FG484I.
			Added footnote for WLCSP package parts.
		Supplemental Information	Removed reference to Stand-alone Power Calculator for MachXO2 Devices. Added reference to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices.