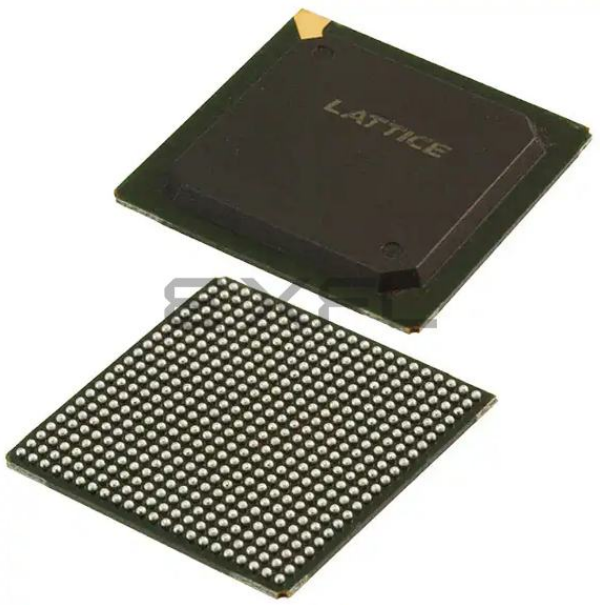
# Lattice Semiconductor Corporation - LCMXO2-7000HE-5FG484I Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 858 |
| Number of Logic Elements/Cells | 6864 |
| Total RAM Bits | 245760 |
| Number of I/O | 334 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-7000he-5fg484i |

# MachXO2 Family Data Sheet Introduction

May 2016 Data Sheet DS1035

## Features

- **Flexible Logic Architecture**
  - Six devices with 256 to 6864 LUT4s and 18 to 334 I/Os
- **Ultra Low Power Devices**
  - Advanced 65 nm low power process
  - As low as 22 µW standby power
  - Programmable low swing differential I/Os
  - Stand-by mode and other power saving options
- **Embedded and Distributed Memory**
  - Up to 240 kbits sysMEM™ Embedded Block RAM
  - Up to 54 kbits Distributed RAM
  - Dedicated FIFO control logic
- **On-Chip User Flash Memory**
  - Up to 256 kbits of User Flash Memory
  - 100,000 write cycles
  - Accessible through WISHBONE, SPI, $I^2C$ and JTAG interfaces
  - Can be used as soft processor PROM or as Flash memory
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated gearing logic
  - 7:1 Gearing for Display I/Os
  - Generic DDR, DDRX2, DDRX4
  - Dedicated DDR/DDR2/LPDDR memory with DQS support
- **High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - PCI
    - LVDS, Bus-LVDS, MLVDS, RSDS, LVPECL
    - SSTL 25/18
    - HSTL 18
    - Schmitt trigger inputs, up to 0.5 V hysteresis
  - I/Os support hot socketing
  - On-chip differential termination
  - Programmable pull-up or pull-down mode
- **Flexible On-Chip Clocking**
  - Eight primary clocks
  - Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
  - Up to two analog PLLs per device with fractional-n frequency synthesis
    - Wide input frequency range (7 MHz to 400 MHz)
- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - Single-chip, secure solution
  - Programmable through JTAG, SPI or $I^2C$
  - Supports background programming of non-volatile memory
  - Optional dual boot with external SPI memory
- **TransFR™ Reconfiguration**
  - In-field logic update while system operates
- **Enhanced System Level Support**
  - On-chip hardened functions: SPI, $I^2C$, timer/counter
  - On-chip oscillator with 5.5% accuracy
  - Unique TraceID for system tracking
  - One Time Programmable (OTP) mode
  - Single power supply with extended operating range
  - IEEE Standard 1149.1 boundary scan
  - IEEE 1532 compliant in-system programming
- **Broad Range of Package Options**
  - TQFP, WLCSP, ucBGA, csBGA, caBGA, ftBGA, fpBGA, QFN package options
  - Small footprint package options
    - As small as 2.5 mm x 2.5 mm
  - Density migration supported
  - Advanced halogen-free packaging

# Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, $I^2C$ controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external $V_{CC}$ supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external $V_{CC}$ supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the $I^2C$ port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2-640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

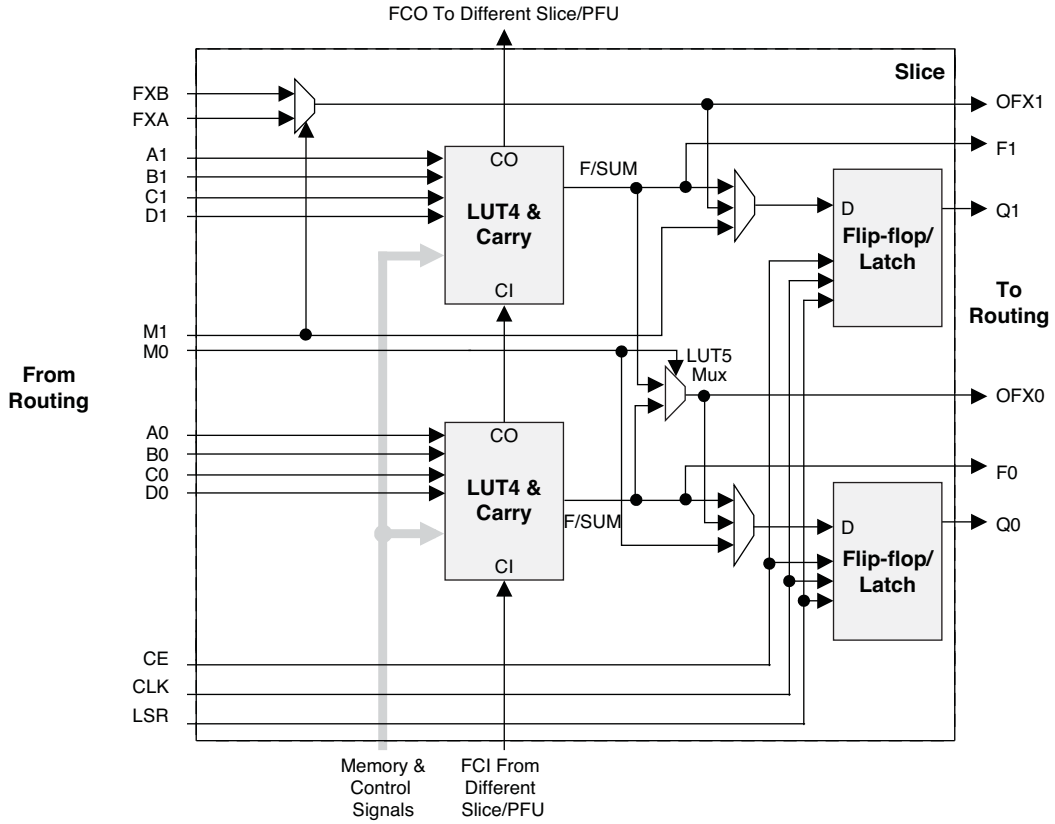
MachXO2 devices provide commonly used hardened functions such as SPI controller, $I^2C$ controller and timer/counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, $I^2C$ and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

## PFU Blocks

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

*Figure 2-4. Slice Diagram*




For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

*Table 2-2. Slice Signal Descriptions*

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0/M1 | Multi-purpose input |
| Input | Control signal | CE | Clock enable |
| Input | Control signal | LSR | Local set/reset |
| Input | Control signal | CLK | System clock |
| Input | Inter-PFU signal | FCIN | Fast carry in[1] |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register outputs |
| Output | Data signals | OFX0 | Output of a LUT5 MUX |
| Output | Data signals | OFX1 | Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice |
| Output | Inter-PFU signal | FCO | Fast carry out[1] |

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

### ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1201, Memory Usage Guide for MachXO2 Devices.

## Routing

There are many resources provided in the MachXO2 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

## Clock/Control Distribution Network

Each MachXO2 device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO2 architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO2-640U, MachXO2-1200/U and higher density devices have two edge clocks each on the top and bottom edges. Lower density devices have no edge clocks. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO2 devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO2 External Switching Characteristics table.

The primary clock signals for the MachXO2-256 and MachXO2-640 are generated from eight 17:1 muxes The available clock sources include eight I/O sources and 9 routing inputs. Primary clock signals for the MachXO2-640U, MachXO2-1200/U and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.

## Programmable I/O Cells (PIC)

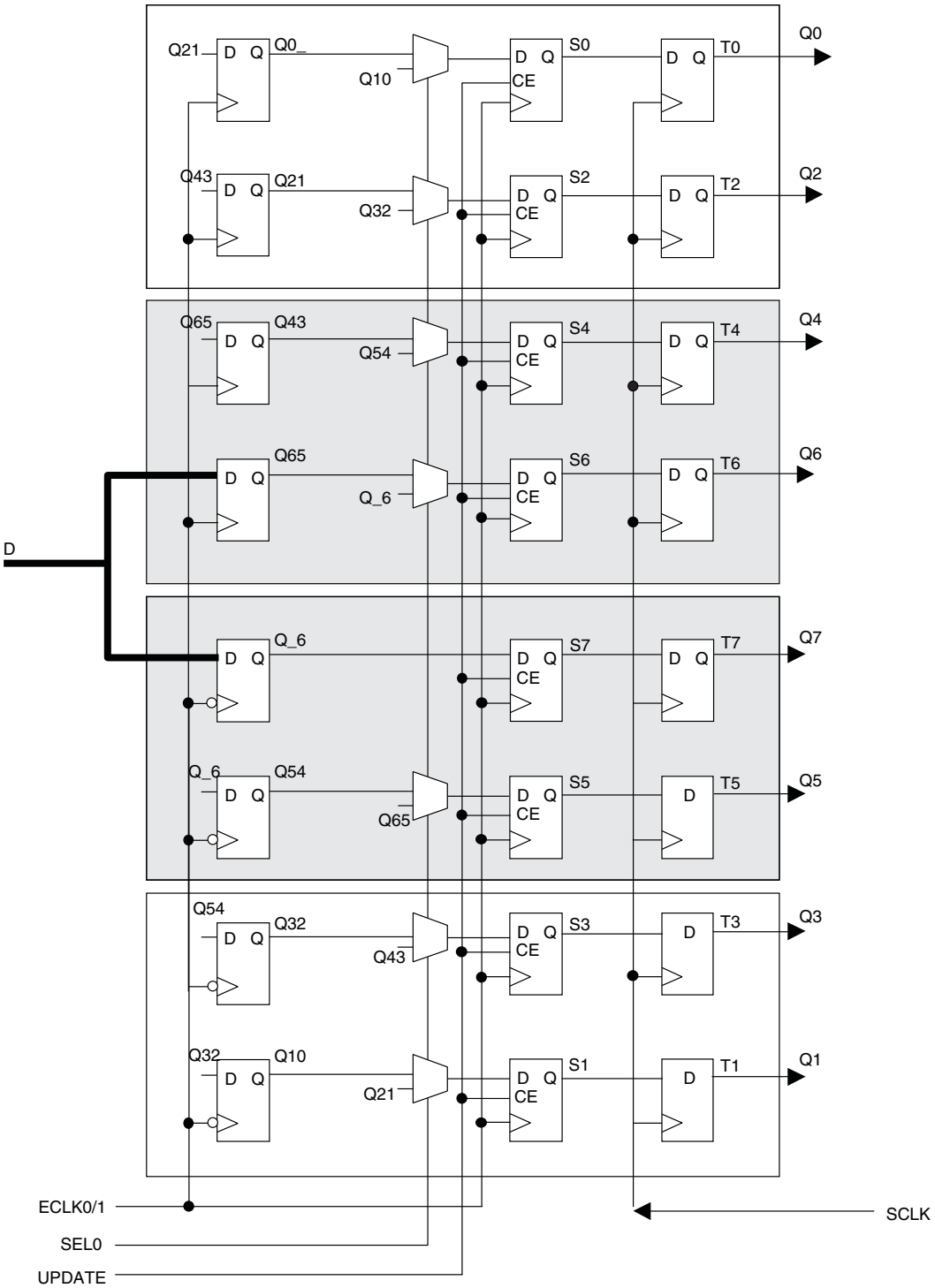
The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO2 devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO2 devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

The MachXO2-640U, MachXO2-1200/U and higher density devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these higher density devices have on-chip differential termination and also provide PCI support.

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-16 shows a block diagram of the input gearbox.

***Figure 2-16. Input Gearbox***



MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 devices contain three types of sysIO buffer pairs.

1. **Left and Right sysIO Buffer Pairs**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential and referenced input buffers.

2. **Bottom sysIO Buffer Pairs**
   The sysIO buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential and referenced input buffers. Only the I/Os on the bottom banks have programmable PCI clamps and differential input termination. The PCI clamp is enabled after $V_{CC}$ and $V_{CCIO}$ are at valid operating levels and the device has been configured.

3. **Top sysIO Buffer Pairs**
   The sysIO buffer pairs in the top bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential and referenced I/O buffers. Half of the sysIO buffer pairs on the top edge have true differential outputs. The sysIO buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver. The referenced input buffer can also be configured as a differential input buffer.

## Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when $V_{CC}$ and $V_{CCIO0}$ have reached $V_{PORUP}$ level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-down to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to $V_{CCIO}$ as the default functionality). The I/O pins will maintain the blank configuration until $V_{CC}$ and $V_{CCIO}$ (for I/O banks containing configuration I/Os) have reached $V_{PORUP}$ levels at which time the I/Os will take on the user-configured settings only after a proper download/configuration.

## Supported Standards

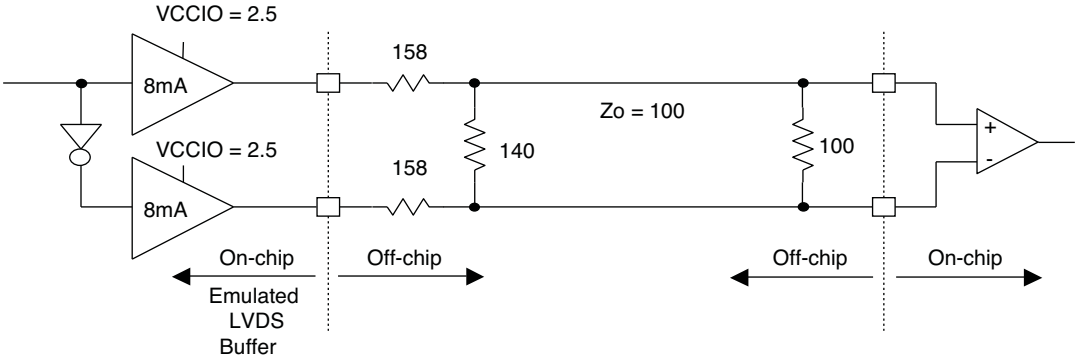
The MachXO2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL, and PCI. The buffer supports the LVTTL, PCI, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO2-640U, MachXO2-1200/U and higher devices support on-chip LVDS output buffers on approximately 50% of the I/Os on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO2 devices. PCI support is provided in the bottom bank of theMachXO2-640U, MachXO2-1200/U and higher density devices. Table 2-11 summarizes the I/O characteristics of the MachXO2 PLDs.

Tables 2-11 and 2-12 show the I/O standards (together with their supply and reference voltages) supported by the MachXO2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1202, MachXO2 sysIO Usage Guide.

## LVDS Emulation

MachXO2 devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

***Figure 3-1. LVDS Using External Resistors (LVDS25E)***



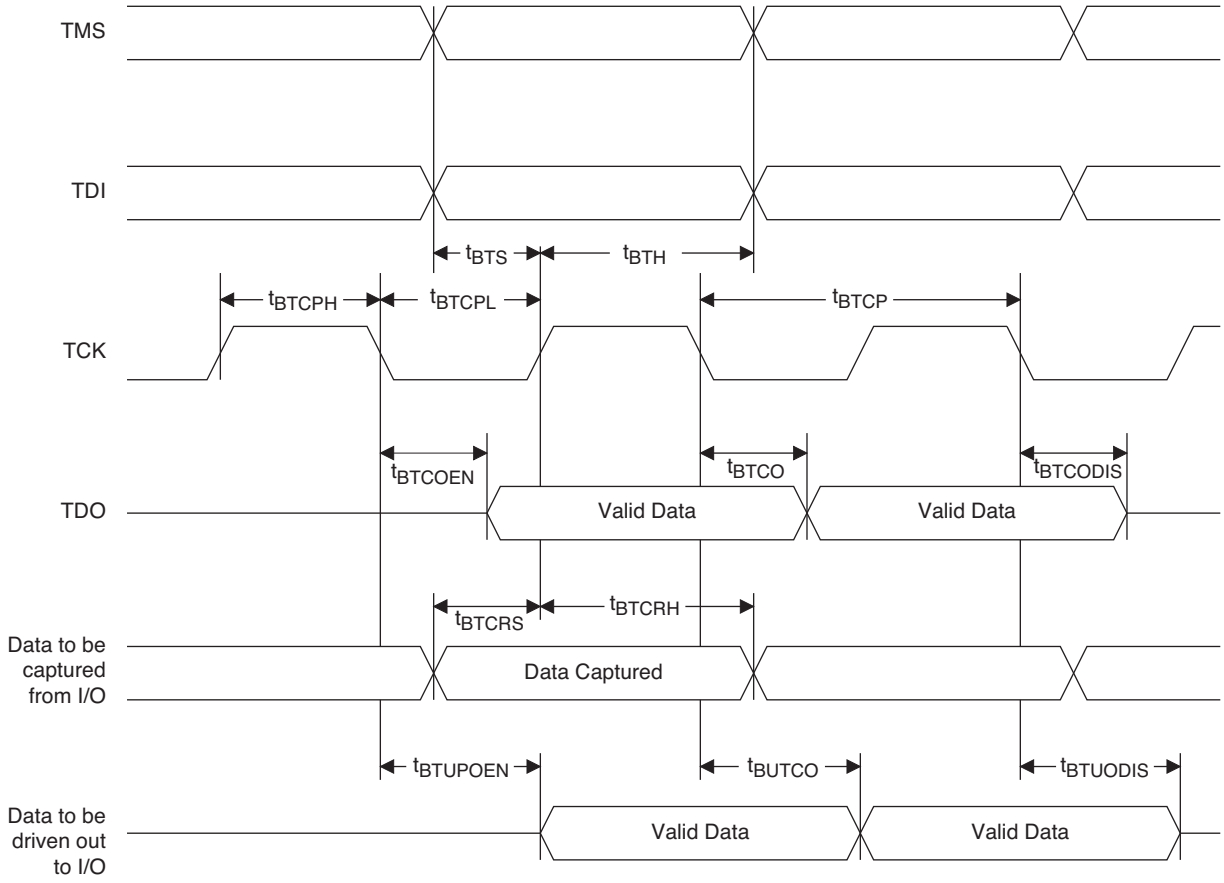

Note: All resistors are ±1%.

***Table 3-1. LVDS25E DC Conditions***

**Over Recommended Operating Conditions**

| Parameter | Description | Typ. | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ohms |
| $R_S$ | Driver series resistor | 158 | Ohms |
| $R_P$ | Driver parallel resistor | 140 | Ohms |
| $R_T$ | Receiver termination | 100 | Ohms |
| $V_{OH}$ | Output high voltage | 1.43 | V |
| $V_{OL}$ | Output low voltage | 1.07 | V |
| $V_{OD}$ | Output differential voltage | 0.35 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 100.5 | Ohms |
| $I_{DC}$ | DC output current | 6.03 | mA |

*Figure 3-12. JTAG Port Timing Waveforms*



# MachXO2 Family Data Sheet Pinout Information



## Signal Descriptions

| Signal Name | I/O | Descriptions |
|---|---|---|
| **General Purpose** | | |
| P[Edge] [Row/Column Number]_[A/B/C/D] | I/O | [Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).<br>[Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.<br>[A/B/C/D] indicates the PIO within the group to which the pad is connected.<br>Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic.<br>During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased. |
| NC | — | No connect. |
| GND | — | GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.<br>For QFN 48 package, the exposed die pad is the device ground. |
| VCC | — | $V_{CC}$ – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply. |
| VCCIOx | — | VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply. |
| **PLL and Clock Functions** (Used as user-programmable I/O pins when not used for PLL or clock pins) | | |
| [LOC]_GPLL[T, C]_IN | — | Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement. |
| [LOC]_GPLL[T, C]_FB | — | Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement. |
| PCLK [n]_[2:0] | — | Primary Clock pads. One to three clock pads per side. |
| **Test and Programming** (Dual function pins used for test access port and during sysCONFIG™) | | |
| TMS | I | Test Mode Select input pin, used to control the 1149.1 state machine. |
| TCK | I | Test Clock input pin, used to clock the 1149.1 state machine. |
| TDI | I | Test Data input pin, used to load data into the device using an 1149.1 state machine. |
| TDO | O | Output pin – Test Data output pin used to shift data out of the device using 1149.1. |
| JTAGENB | I | Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then:<br>If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O.<br>If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.<br>For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide. |
| **Configuration** (Dual function pins used during sysCONFIG) | | |
| PROGRAMN | I | Initiates configuration sequence when asserted low. During configuration, or when reserved as PROGRAMN in user mode, this pin always has an active pull-up. |

## For Further Information

For further information regarding logic signal connections for various packages please refer to the MachXO2 Device Pinout Files.

## Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Users must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

### For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1198, Power Estimation and Management for MachXO2 Devices
- The Power Calculator tool is included with the Lattice design tools, or as a standalone download from www.latticesemi.com/software

## Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-256ZE-1SG32C | 256 | 1.2 V | –1 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256ZE-2SG32C | 256 | 1.2 V | –2 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256ZE-3SG32C | 256 | 1.2 V | –3 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256ZE-1UMG64C | 256 | 1.2 V | –1 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256ZE-2UMG64C | 256 | 1.2 V | –2 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256ZE-3UMG64C | 256 | 1.2 V | –3 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256ZE-1TG100C | 256 | 1.2 V | –1 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256ZE-2TG100C | 256 | 1.2 V | –2 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256ZE-3TG100C | 256 | 1.2 V | –3 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256ZE-1MG132C | 256 | 1.2 V | –1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-256ZE-2MG132C | 256 | 1.2 V | –2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-256ZE-3MG132C | 256 | 1.2 V | –3 | Halogen-Free csBGA | 132 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640ZE-1TG100C | 640 | 1.2 V | –1 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640ZE-2TG100C | 640 | 1.2 V | –2 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640ZE-3TG100C | 640 | 1.2 V | –3 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640ZE-1MG132C | 640 | 1.2 V | –1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-640ZE-2MG132C | 640 | 1.2 V | –2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-640ZE-3MG132C | 640 | 1.2 V | –3 | Halogen-Free csBGA | 132 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-1200ZE-1SG32C | 1280 | 1.2 V | –1 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200ZE-2SG32C | 1280 | 1.2 V | –2 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200ZE-3SG32C | 1280 | 1.2 V | –3 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200ZE-1TG100C | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200ZE-2TG100C | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200ZE-3TG100C | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200ZE-1MG132C | 1280 | 1.2 V | –1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-2MG132C | 1280 | 1.2 V | –2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-3MG132C | 1280 | 1.2 V | –3 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-1TG144C | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200ZE-2TG144C | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200ZE-3TG144C | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 144 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000UHC-4FG484C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-2000UHC-5FG484C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-2000UHC-6FG484C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000HC-4QN84C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000HC-5QN84C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000HC-6QN84C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000HC-4MG132C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HC-5MG132C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HC-6MG132C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HC-4TG144C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HC-5TG144C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HC-6TG144C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HC-4BG256C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HC-5BG256C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HC-6BG256C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HC-4FTG256C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HC-5FTG256C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HC-6FTG256C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HC-4BG332C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HC-5BG332C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HC-6BG332C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HC-4FG484C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HC-5FG484C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HC-6FG484C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | COM |

## High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000HE-4TG100C | 2112 | 1.2 V | –4 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000HE-5TG100C | 2112 | 1.2 V | –5 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000HE-6TG100C | 2112 | 1.2 V | –6 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000HE-4TG144C | 2112 | 1.2 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000HE-5TG144C | 2112 | 1.2 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000HE-6TG144C | 2112 | 1.2 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000HE-4MG132C | 2112 | 1.2 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000HE-5MG132C | 2112 | 1.2 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000HE-6MG132C | 2112 | 1.2 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000HE-4BG256C | 2112 | 1.2 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000HE-5BG256C | 2112 | 1.2 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000HE-6BG256C | 2112 | 1.2 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000HE-4FTG256C | 2112 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000HE-5FTG256C | 2112 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000HE-6FTG256C | 2112 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000UHE-4FG484C | 2112 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-2000UHE-5FG484C | 2112 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-2000UHE-6FG484C | 2112 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000HE-4TG144C | 4320 | 1.2 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HE-5TG144C | 4320 | 1.2 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HE-6TG144C | 4320 | 1.2 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HE-4MG132C | 4320 | 1.2 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HE-5MG132C | 4320 | 1.2 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HE-6MG132C | 4320 | 1.2 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HE-4BG256C | 4320 | 1.2 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HE-4MG184C | 4320 | 1.2 V | –4 | Halogen-Free csBGA | 184 | COM |
| LCMXO2-4000HE-5MG184C | 4320 | 1.2 V | –5 | Halogen-Free csBGA | 184 | COM |
| LCMXO2-4000HE-6MG184C | 4320 | 1.2 V | –6 | Halogen-Free csBGA | 184 | COM |
| LCMXO2-4000HE-5BG256C | 4320 | 1.2 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HE-6BG256C | 4320 | 1.2 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HE-4FTG256C | 4320 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HE-5FTG256C | 4320 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HE-6FTG256C | 4320 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HE-4BG332C | 4320 | 1.2 V | –4 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HE-5BG332C | 4320 | 1.2 V | –5 | Halogen-Free caBGA | 332 | COM |

## High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-256HC-4SG32I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256HC-5SG32I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256HC-6SG32I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256HC-4SG48I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 48 | IND |
| LCMXO2-256HC-5SG48I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 48 | IND |
| LCMXO2-256HC-6SG48I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 48 | IND |
| LCMXO2-256HC-4UMG64I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256HC-5UMG64I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256HC-6UMG64I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256HC-4TG100I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256HC-5TG100I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256HC-6TG100I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256HC-4MG132I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256HC-5MG132I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256HC-6MG132I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640HC-4SG48I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 48 | IND |
| LCMXO2-640HC-5SG48I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 48 | IND |
| LCMXO2-640HC-6SG48I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 48 | IND |
| LCMXO2-640HC-4TG100I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640HC-5TG100I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640HC-6TG100I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640HC-4MG132I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640HC-5MG132I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640HC-6MG132I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640UHC-4TG144I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-640UHC-5TG144I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-640UHC-6TG144I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000HC-4QN84I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000HC-5QN84I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000HC-6QN84I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000HC-4TG144I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HC-5TG144I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HC-6TG144I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HC-4MG132I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HC-5MG132I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HC-6MG132I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HC-4BG256I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HC-5BG256I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HC-6BG256I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HC-4FTG256I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HC-5FTG256I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HC-6FTG256I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HC-4BG332I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HC-5BG332I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HC-6BG332I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HC-4FG484I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HC-5FG484I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HC-6FG484I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000HC-4TG144I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HC-5TG144I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HC-6TG144I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HC-4BG256I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HC-5BG256I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HC-6BG256I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HC-4FTG256I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HC-5FTG256I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HC-6FTG256I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HC-4BG332I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HC-5BG332I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HC-6BG332I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HC-4FG400I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 400 | IND |
| LCMXO2-7000HC-5FG400I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 400 | IND |
| LCMXO2-7000HC-6FG400I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 400 | IND |
| LCMXO2-7000HC-4FG484I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HC-5FG484I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HC-6FG484I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000HE-4MG132I | 4320 | 1.2 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HE-5MG132I | 4320 | 1.2 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HE-6MG132I | 4320 | 1.2 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HE-4TG144I | 4320 | 1.2 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HE-5TG144I | 4320 | 1.2 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HE-6TG144I | 4320 | 1.2 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HE-4MG184I | 4320 | 1.2 V | –4 | Halogen-Free csBGA | 184 | IND |
| LCMXO2-4000HE-5MG184I | 4320 | 1.2 V | –5 | Halogen-Free csBGA | 184 | IND |
| LCMXO2-4000HE-6MG184I | 4320 | 1.2 V | –6 | Halogen-Free csBGA | 184 | IND |
| LCMXO2-4000HE-4BG256I | 4320 | 1.2 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HE-5BG256I | 4320 | 1.2 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HE-6BG256I | 4320 | 1.2 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HE-4FTG256I | 4320 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HE-5FTG256I | 4320 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HE-6FTG256I | 4320 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HE-4BG332I | 4320 | 1.2 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HE-5BG332I | 4320 | 1.2 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HE-6BG332I | 4320 | 1.2 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HE-4FG484I | 4320 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HE-5FG484I | 4320 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HE-6FG484I | 4320 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000HE-4TG144I | 6864 | 1.2 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HE-5TG144I | 6864 | 1.2 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HE-6TG144I | 6864 | 1.2 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HE-4BG256I | 6864 | 1.2 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HE-5BG256I | 6864 | 1.2 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HE-6BG256I | 6864 | 1.2 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HE-4FTG256I | 6864 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HE-5FTG256I | 6864 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HE-6FTG256I | 6864 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HE-4BG332I | 6864 | 1.2 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HE-5BG332I | 6864 | 1.2 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HE-6BG332I | 6864 | 1.2 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HE-4FG484I | 6864 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HE-5FG484I | 6864 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HE-6FG484I | 6864 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | IND |

## R1 Device Specifications

The LCMXO2-1200ZE/HC "R1" devices have the same specifications as their Standard (non-R1) counterparts except as listed below. For more details on the R1 to Standard migration refer to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard Non-R1) Devices.

- The User Flash Memory (UFM) cannot be programmed through the internal WISHBONE interface. It can still be programmed through the JTAG/SPI/$I^2C$ ports.
- The on-chip differential input termination resistor value is higher than intended. It is approximately 200Ω as opposed to the intended 100Ω. It is recommended to use external termination resistors for differential inputs. The on-chip termination resistors can be disabled through Lattice design software.
- Soft Error Detection logic may not produce the correct result when it is run for the first time after configuration. To use this feature, discard the result from the first operation. Subsequent operations will produce the correct result.
- Under certain conditions, IIH exceeds data sheet specifications. The following table provides more details:

| Condition | Clamp | Pad Rising IIH Max. | Pad Falling IIH Min. | Steady State Pad High IIH | Steady State Pad Low IIL |
|---|---|---|---|---|---|
| VPAD > VCCIO | OFF | 1 mA | –1 mA | 1 mA | 10 µA |
| VPAD = VCCIO | ON | 10 µA | –10 µA | 10 µA | 10 µA |
| VPAD = VCCIO | OFF | 1 mA | –1 mA | 1 mA | 10 µA |
| VPAD < VCCIO | OFF | 10 µA | –10 µA | 10 µA | 10 µA |

- The user SPI interface does not operate correctly in some situations. During master read access and slave write access, the last byte received does not generate the RRDY interrupt.
- In GDDRX2, GDDRX4 and GDDR71 modes, ECLKSYNC may have a glitch in the output under certain conditions, leading to possible loss of synchronization.
- When using the hard $I^2C$ IP core, the $I^2C$ status registers I2C_1_SR and I2C_2_SR may not update correctly.
- PLL Lock signal will glitch high when coming out of standby. This glitch lasts for about 10 µsec before returning low.
- Dual boot only available on HC devices, requires tying VCC and VCCIO2 to the same 3.3 V or 2.5 V supply.

# MachXO2 Family Data Sheet Supplemental Information



## For Further Information

A variety of technical notes for the MachXO2 family are available on the Lattice web site.

- TN1198, Power Estimation and Management for MachXO2 Devices
- TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide
- TN1201, Memory Usage Guide for MachXO2 Devices
- TN1202, MachXO2 sysIO Usage Guide
- TN1203, Implementing High-Speed Interfaces with MachXO2 Devices
- TN1204, MachXO2 Programming and Configuration Usage Guide
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices
- TN1206, MachXO2 SRAM CRC Error Detection Usage Guide
- TN1207, Using TraceID in MachXO2 Devices
- TN1074, PCB Layout Recommendations for BGA Packages
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices
- AN8066, Boundary Scan Testability with Lattice sysIO Capability
- MachXO2 Device Pinout Files
- Thermal Management document
- Lattice design tools

For further information on interface standards, refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, LVDS, DDR, DDR2, LPDDR): www.jedec.org
- PCI: www.pcisig.com