

Welcome to [E-XFL.COM](https://www.e-xfl.com)

## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Active
Number of LABs/CLBs	858
Number of Logic Elements/Cells	6864
Total RAM Bits	245760
Number of I/O	206
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (Tj)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-7000he-5ftg256i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-7000he-5ftg256i</a>

---

## Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I<sup>2</sup>C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external V<sub>CC</sub> supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V<sub>CC</sub> supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I<sup>2</sup>C port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

---

## ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1201, [Memory Usage Guide for MachXO2 Devices](#).

## Routing

There are many resources provided in the MachXO2 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

## Clock/Control Distribution Network

Each MachXO2 device has eight clock inputs (PCLK [T, C] [Banknum]\_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

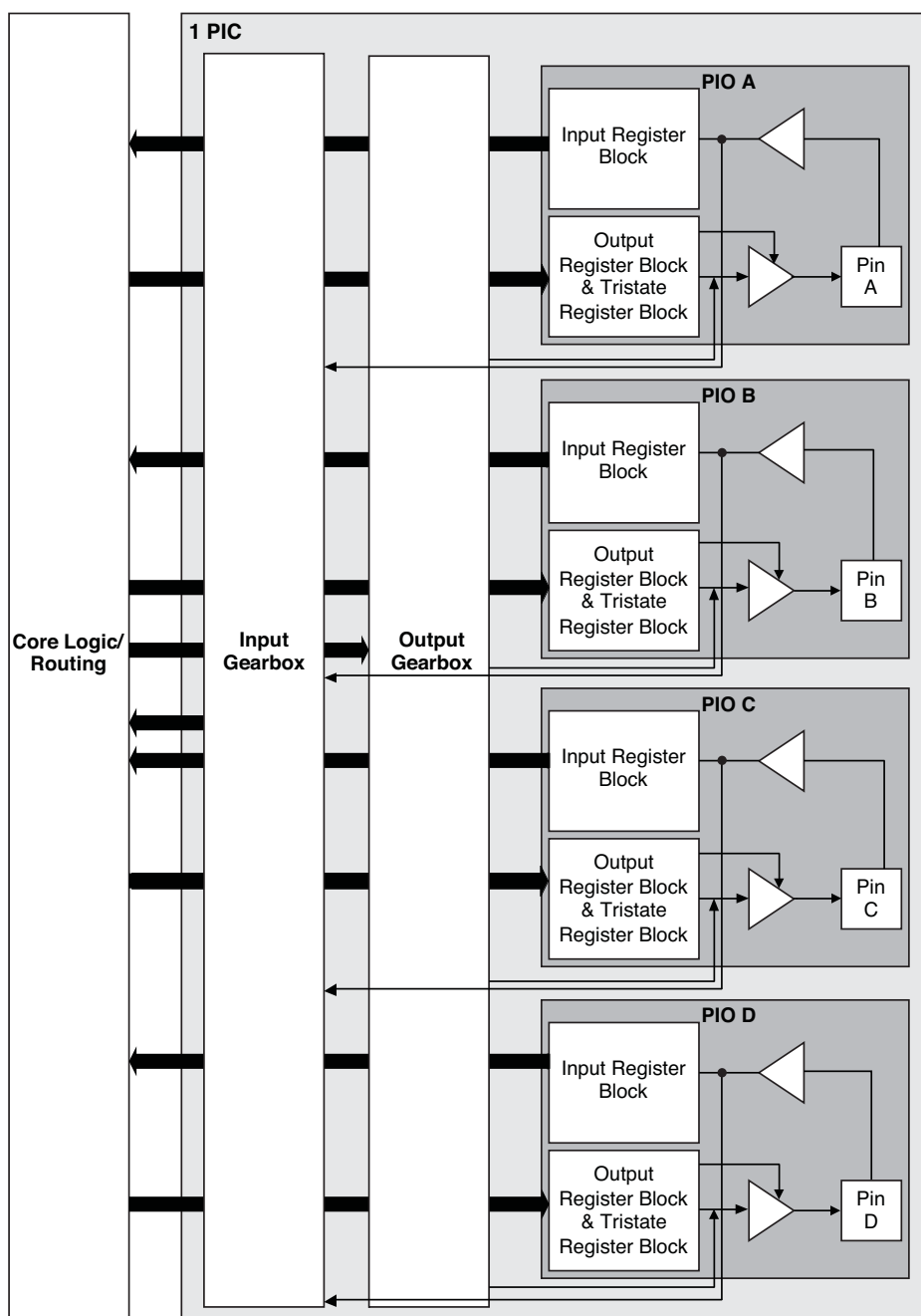
The MachXO2 architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO2-640U, MachXO2-1200/U and higher density devices have two edge clocks each on the top and bottom edges. Lower density devices have no edge clocks. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO2 devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO2 External Switching Characteristics table.

The primary clock signals for the MachXO2-256 and MachXO2-640 are generated from eight 17:1 muxes. The available clock sources include eight I/O sources and 9 routing inputs. Primary clock signals for the MachXO2-640U, MachXO2-1200/U and larger devices are generated from eight 27:1 muxes. The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.

**Figure 2-11. Group of Four Programmable I/O Cells**

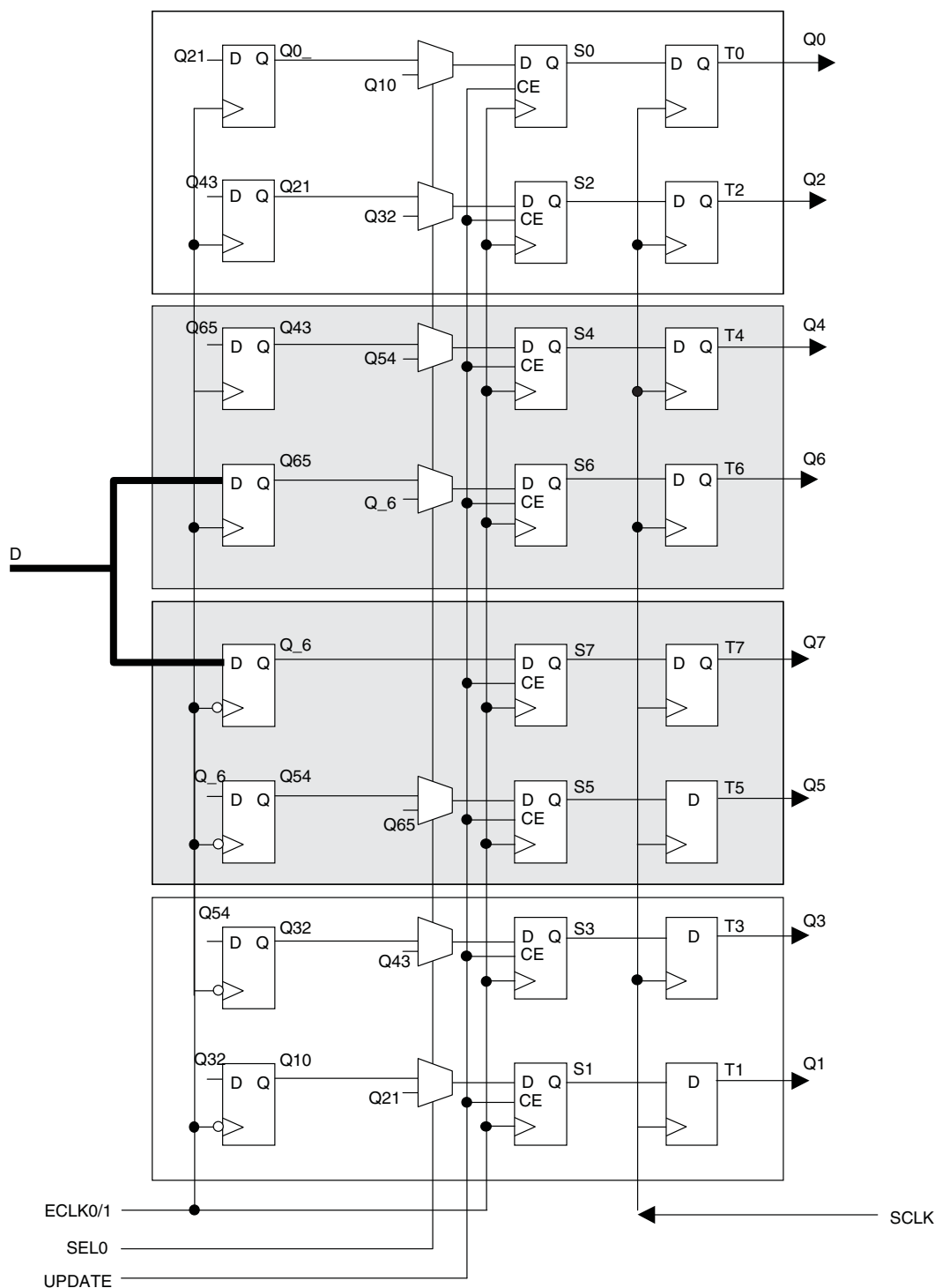


**Notes:**

1. Input gearbox is available only in PIC on the bottom edge of MachXO2-640U, MachXO2-1200/U and larger devices.
2. Output gearbox is available only in PIC on the top edge of MachXO2-640U, MachXO2-1200/U and larger devices.

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-16 shows a block diagram of the input gearbox.

**Figure 2-16. Input Gearbox**



More information on the input gearbox is available in TN1203, [Implementing High-Speed Interfaces with MachXO2 Devices](#).

## Output Gearbox

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDR4 (8:1) gearbox or as two ODDR2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

**Table 2-10. Output Gearbox Signal List**

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDR4(8:1): D[7:0]		
GDDR2(4:1)(IOL-A): D[3:0]		
GDDR2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-17 shows the output gearbox block diagram.

---

## Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

### IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with  $V_{CCIO}$  Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, [Boundary Scan Testability with Lattice sysIO Capability](#) and TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#).

### Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I<sup>2</sup>C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

1. Internal Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I<sup>2</sup>C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, [MachXO2 Programming and Configuration Usage Guide](#) for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

### TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#) for details.



# MachXO2 Family Data Sheet

## DC and Switching Characteristics

March 2017

Data Sheet DS1035

### Absolute Maximum Ratings<sup>1, 2, 3</sup>

	MachXO2 ZE/HE (1.2 V)	MachXO2 HC (2.5 V / 3.3 V)
Supply Voltage $V_{CC}$	–0.5 V to 1.32 V	–0.5 V to 3.75 V
Output Supply Voltage $V_{CCIO}$	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied <sup>4, 5</sup>	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied <sup>4</sup>	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature ( $T_J$ )	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to ( $V_{IHMAX} + 2$ ) volts is permitted for a duration of <20 ns.
5. The dual function I<sup>2</sup>C pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.

### Recommended Operating Conditions<sup>1</sup>

Symbol	Parameter	Min.	Max.	Units
$V_{CC}^1$	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V / 3.3 V Devices	2.375	3.6	V
$V_{CCIO}^{1, 2, 3}$	I/O Driver Supply Voltage	1.14	3.6	V
$t_{JCOM}$	Junction Temperature Commercial Operation	0	85	°C
$t_{JIND}$	Junction Temperature Industrial Operation	–40	100	°C

1. Like power supplies must be tied together. For example, if  $V_{CCIO}$  and  $V_{CC}$  are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3.  $V_{CCIO}$  pins of unused I/O banks should be connected to the  $V_{CC}$  power supply on boards.

### Power Supply Ramp Rates<sup>1</sup>

Symbol	Parameter	Min.	Typ.	Max.	Units
$t_{RAMP}$	Power supply ramp rates for all power supplies.	0.01	—	100	V/ms

1. Assumes monotonic ramp rates.



**Programming and Erase Flash Supply Current – ZE Devices<sup>1, 2, 3, 4</sup>**

Symbol	Parameter	Device	Typ. <sup>5</sup>	Units
$I_{CC}$	Core Power Supply	LCMXO2-256ZE	13	mA
		LCMXO2-640ZE	14	mA
		LCMXO2-1200ZE	15	mA
		LCMXO2-2000ZE	17	mA
		LCMXO2-4000ZE	18	mA
		LCMXO2-7000ZE	20	mA
$I_{CCIO}$	Bank Power Supply <sup>6</sup>	All devices	0	mA

1. For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).

2. Assumes all inputs are held at  $V_{CCIO}$  or GND and all outputs are tri-stated.

3. Typical user pattern.

4. JTAG programming is at 25 MHz.

5.  $T_J = 25^\circ\text{C}$ , power supplies at nominal voltage.

6. Per bank.  $V_{CCIO} = 2.5\text{ V}$ . Does not include pull-up/pull-down.

## sysIO Recommended Operating Conditions

Standard	V <sub>CCIO</sub> (V)			V <sub>REF</sub> (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS 3.3	3.135	3.3	3.6	—	—	—
LVC MOS 2.5	2.375	2.5	2.625	—	—	—
LVC MOS 1.8	1.71	1.8	1.89	—	—	—
LVC MOS 1.5	1.425	1.5	1.575	—	—	—
LVC MOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.6	—	—	—
PCI <sup>3</sup>	3.135	3.3	3.6	—	—	—
SSTL25	2.375	2.5	2.625	1.15	1.25	1.35
SSTL18	1.71	1.8	1.89	0.833	0.9	0.969
HSTL18	1.71	1.8	1.89	0.816	0.9	1.08
LVC MOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVC MOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVC MOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVC MOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVC MOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVC MOS12R33 <sup>4</sup>	3.135	3.3	3.6	0.45	0.6	0.75
LVC MOS12R25 <sup>4</sup>	2.375	2.5	2.625	0.45	0.6	0.75
LVC MOS10R33 <sup>4</sup>	3.135	3.3	3.6	0.35	0.5	0.65
LVC MOS10R25 <sup>4</sup>	2.375	2.5	2.625	0.35	0.5	0.65
LVDS25 <sup>1, 2</sup>	2.375	2.5	2.625	—	—	—
LVDS33 <sup>1, 2</sup>	3.135	3.3	3.6	—	—	—
LVPECL <sup>1</sup>	3.135	3.3	3.6	—	—	—
BLVDS <sup>1</sup>	2.375	2.5	2.625	—	—	—
RSDS <sup>1</sup>	2.375	2.5	2.625	—	—	—
SSTL18D	1.71	1.8	1.89	—	—	—
SSTL25D	2.375	2.5	2.625	—	—	—
HSTL18D	1.71	1.8	1.89	—	—	—

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.

2. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.

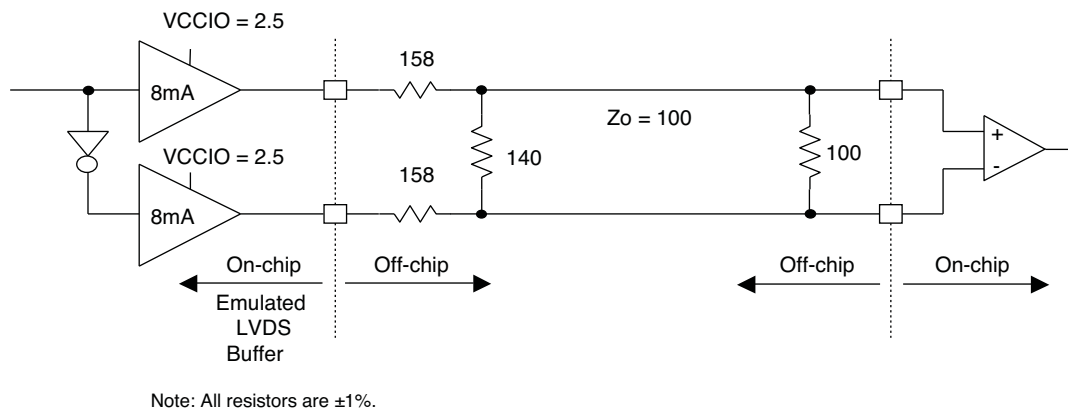
3. Input on the bottom bank of the MachXO2-640U, MachXO2-1200/U and larger devices only.

4. Supported only for inputs and BIDs for all ZE devices, and –6 speed grade for HE and HC devices.

### LVDS Emulation

MachXO2 devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

**Figure 3-1. LVDS Using External Resistors (LVDS25E)**



**Table 3-1. LVDS25E DC Conditions**

#### Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
$Z_{OUT}$	Output impedance	20	Ohms
$R_S$	Driver series resistor	158	Ohms
$R_P$	Driver parallel resistor	140	Ohms
$R_T$	Receiver termination	100	Ohms
$V_{OH}$	Output high voltage	1.43	V
$V_{OL}$	Output low voltage	1.07	V
$V_{OD}$	Output differential voltage	0.35	V
$V_{CM}$	Output common mode voltage	1.25	V
$Z_{BACK}$	Back impedance	100.5	Ohms
$I_{DC}$	DC output current	6.03	mA

Parameter	Description	Device	-6		-5		-4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>HPLL</sub>	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	0.41	—	0.48	—	0.55	—	ns
		MachXO2-2000HC-HE	0.42	—	0.49	—	0.56	—	ns
		MachXO2-4000HC-HE	0.43	—	0.50	—	0.58	—	ns
		MachXO2-7000HC-HE	0.46	—	0.54	—	0.62	—	ns
t <sub>SU_DELPLL</sub>	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	2.88	—	3.19	—	3.72	—	ns
		MachXO2-2000HC-HE	2.87	—	3.18	—	3.70	—	ns
		MachXO2-4000HC-HE	2.96	—	3.28	—	3.81	—	ns
		MachXO2-7000HC-HE	3.05	—	3.35	—	3.87	—	ns
t <sub>H_DELPLL</sub>	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-2000HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-4000HC-HE	–0.87	—	–0.87	—	–0.87	—	ns
		MachXO2-7000HC-HE	–0.91	—	–0.91	—	–0.91	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Aligned <sup>9, 12</sup>									
t <sub>DVA</sub>	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.317	—	0.344	—	0.368	UI
t <sub>DVE</sub>	Input Data Hold After CLK		0.742	—	0.702	—	0.668	—	UI
f <sub>DATA</sub>	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f <sub>DDRX1</sub>	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Centered <sup>9, 12</sup>									
t <sub>SU</sub>	Input Data Setup Before CLK	All MachXO2 devices, all sides	0.566	—	0.560	—	0.538	—	ns
t <sub>HO</sub>	Input Data Hold After CLK		0.778	—	0.879	—	1.090	—	ns
f <sub>DATA</sub>	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f <sub>DDRX1</sub>	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Aligned <sup>9, 12</sup>									
t <sub>DVA</sub>	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only <sup>11</sup>	—	0.316	—	0.342	—	0.364	UI
t <sub>DVE</sub>	Input Data Hold After CLK		0.710	—	0.675	—	0.679	—	UI
f <sub>DATA</sub>	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f <sub>DDRX2</sub>	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Centered <sup>9, 12</sup>									
t <sub>SU</sub>	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only <sup>11</sup>	0.233	—	0.219	—	0.198	—	ns
t <sub>HO</sub>	Input Data Hold After CLK		0.287	—	0.287	—	0.344	—	ns
f <sub>DATA</sub>	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f <sub>DDRX2</sub>	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	166	—	139	—	116	MHz

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered <sup>9, 12</sup>									
t <sub>DVB</sub>	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.535	—	0.670	—	0.830	—	ns
t <sub>DVA</sub>	Output Data Valid After CLK Output		0.535	—	0.670	—	0.830	—	ns
f <sub>DATA</sub>	DDRX2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f <sub>DDRX2</sub>	DDRX2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	—	231	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned <sup>9, 12</sup>									
t <sub>DIA</sub>	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t <sub>DIB</sub>	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f <sub>DATA</sub>	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f <sub>DDRX4</sub>	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered <sup>9, 12</sup>									
t <sub>DVB</sub>	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.455	—	0.570	—	0.710	—	ns
t <sub>DVA</sub>	Output Data Valid After CLK Output		0.455	—	0.570	—	0.710	—	ns
f <sub>DATA</sub>	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f <sub>DDRX4</sub>	DDRX4 ECLK Frequency (minimum limited by PLL)		—	378	—	315	—	262	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1 <sup>9, 12</sup>									
t <sub>DIB</sub>	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.160	—	0.180	—	0.200	ns
t <sub>DIA</sub>	Output Data Invalid After CLK Output		—	0.160	—	0.180	—	0.200	ns
f <sub>DATA</sub>	DDR71 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f <sub>DDR71</sub>	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f <sub>CLKOUT</sub>	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz

Parameter	Description	Device	-6		-5		-4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR <sup>9, 12</sup>									
t <sub>DVADQ</sub>	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. <sup>13</sup>	—	0.369	—	0.395	—	0.421	UI
t <sub>DVEDQ</sub>	Input Data Hold After DQS Input		0.529	—	0.530	—	0.527	—	UI
t <sub>DQVBS</sub>	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t <sub>DQVAS</sub>	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f <sub>DATA</sub>	MEM LPDDR Serial Data Speed		—	280	—	250	—	208	Mbps
f <sub>SCLK</sub>	SCLK Frequency		—	140	—	125	—	104	MHz
f <sub>LPDDR</sub>	LPDDR Data Transfer Rate		0	280	0	250	0	208	Mbps
DDR <sup>9, 12</sup>									
t <sub>DVADQ</sub>	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. <sup>13</sup>	—	0.350	—	0.387	—	0.414	UI
t <sub>DVEDQ</sub>	Input Data Hold After DQS Input		0.545	—	0.538	—	0.532	—	UI
t <sub>DQVBS</sub>	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t <sub>DQVAS</sub>	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f <sub>DATA</sub>	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f <sub>SCLK</sub>	SCLK Frequency		—	150	—	125	—	104	MHz
f <sub>MEM_DDR</sub>	MEM DDR Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps
DDR2 <sup>9, 12</sup>									
t <sub>DVADQ</sub>	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. <sup>13</sup>	—	0.360	—	0.378	—	0.406	UI
t <sub>DVEDQ</sub>	Input Data Hold After DQS Input		0.555	—	0.549	—	0.542	—	UI
t <sub>DQVBS</sub>	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t <sub>DQVAS</sub>	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f <sub>DATA</sub>	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f <sub>SCLK</sub>	SCLK Frequency		—	150	—	125	—	104	MHz
f <sub>MEM_DDR2</sub>	MEM DDR2 Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps

- Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
- General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
- Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
- DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
- 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
- For Generic DDRX1 mode  $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$ .
- The  $t_{SU\_DEL}$  and  $t_{H\_DEL}$  values use the SCLK\_ZERHOLD default step size. Each step is 105 ps (–6), 113 ps (–5), 120 ps (–4).
- This number for general purpose usage. Duty cycle tolerance is +/- 10%.
- Duty cycle is +/-5% for system usage.
- The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
- High-speed DDR and LVDS not supported in SG32 (32 QFN) packages.
- Advance information for MachXO2 devices in 48 QFN packages.
- DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

Parameter	Description	Device	-3		-2		-1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>HPLL</sub>	Clock to Data Hold – PIO Input Register	MachXO2-1200ZE	0.66	—	0.68	—	0.80	—	ns
		MachXO2-2000ZE	0.68	—	0.70	—	0.83	—	ns
		MachXO2-4000ZE	0.68	—	0.71	—	0.84	—	ns
		MachXO2-7000ZE	0.73	—	0.74	—	0.87	—	ns
t <sub>SU_DELPLL</sub>	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200ZE	5.14	—	5.69	—	6.20	—	ns
		MachXO2-2000ZE	5.11	—	5.67	—	6.17	—	ns
		MachXO2-4000ZE	5.27	—	5.84	—	6.35	—	ns
		MachXO2-7000ZE	5.15	—	5.71	—	6.23	—	ns
t <sub>H_DELPLL</sub>	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200ZE	–1.36	—	–1.36	—	–1.36	—	ns
		MachXO2-2000ZE	–1.35	—	–1.35	—	–1.35	—	ns
		MachXO2-4000ZE	–1.43	—	–1.43	—	–1.43	—	ns
		MachXO2-7000ZE	–1.41	—	–1.41	—	–1.41	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Aligned <sup>9, 12</sup>									
t <sub>DVA</sub>	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.382	—	0.401	—	0.417	UI
t <sub>DVE</sub>	Input Data Hold After CLK		0.670	—	0.684	—	0.693	—	UI
f <sub>DATA</sub>	DDR1 Input Data Speed		—	140	—	116	—	98	Mbps
f <sub>DDR1</sub>	DDR1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Centered <sup>9, 12</sup>									
t <sub>SU</sub>	Input Data Setup Before CLK	All MachXO2 devices, all sides	1.319	—	1.412	—	1.462	—	ns
t <sub>HO</sub>	Input Data Hold After CLK		0.717	—	1.010	—	1.340	—	ns
f <sub>DATA</sub>	DDR1 Input Data Speed		—	140	—	116	—	98	Mbps
f <sub>DDR1</sub>	DDR1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Aligned <sup>9, 12</sup>									
t <sub>DVA</sub>	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only <sup>11</sup>	—	0.361	—	0.346	—	0.334	UI
t <sub>DVE</sub>	Input Data Hold After CLK		0.602	—	0.625	—	0.648	—	UI
f <sub>DATA</sub>	DDR2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f <sub>DDR2</sub>	DDR2 ECLK Frequency		—	140	—	117	—	97	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Centered <sup>9, 12</sup>									
t <sub>SU</sub>	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only <sup>11</sup>	0.472	—	0.672	—	0.865	—	ns
t <sub>HO</sub>	Input Data Hold After CLK		0.363	—	0.501	—	0.743	—	ns
f <sub>DATA</sub>	DDR2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f <sub>DDR2</sub>	DDR2 ECLK Frequency		—	140	—	117	—	97	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input - GDDR4_RX.ECLK.Aligned <sup>9, 12</sup>									
t <sub>DVA</sub>	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only <sup>11</sup>	—	0.307	—	0.316	—	0.326	UI
t <sub>DVE</sub>	Input Data Hold After ECLK		0.662	—	0.650	—	0.649	—	UI
f <sub>DATA</sub>	DDR4 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f <sub>DDR4</sub>	DDR4 ECLK Frequency		—	210	—	176	—	146	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	53	—	44	—	37	MHz

	MachXO2-1200					MachXO2-1200U
	100 TQFP	132 csBGA	144 TQFP	25 WLCSP	32 QFN <sup>1</sup>	256 ftBGA
<b>General Purpose I/O per Bank</b>						
Bank 0	18	25	27	11	9	50
Bank 1	21	26	26	0	2	52
Bank 2	20	28	28	7	9	52
Bank 3	20	25	26	0	2	16
Bank 4	0	0	0	0	0	16
Bank 5	0	0	0	0	0	20
Total General Purpose Single Ended I/O	79	104	107	18	22	206
<b>Differential I/O per Bank</b>						
Bank 0	9	13	14	5	4	25
Bank 1	10	13	13	0	1	26
Bank 2	10	14	14	2	4	26
Bank 3	10	12	13	0	1	8
Bank 4	0	0	0	0	0	8
Bank 5	0	0	0	0	0	10
Total General Purpose Differential I/O	39	52	54	7	10	103
<b>Dual Function I/O</b>						
	31	33	33	18	22	33
<b>High-speed Differential I/O</b>						
Bank 0	4	7	7	0	0	14
<b>Gearboxes</b>						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	4	7	7	0	0	14
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	5	7	7	0	2	14
<b>DQS Groups</b>						
Bank 1	1	2	2	0	0	2
<b>VCCIO Pins</b>						
Bank 0	2	3	3	1	2	4
Bank 1	2	3	3	0	1	4
Bank 2	2	3	3	1	2	4
Bank 3	3	3	3	0	1	1
Bank 4	0	0	0	0	0	2
Bank 5	0	0	0	0	0	1
VCC	2	4	4	2	2	8
GND	8	10	12	2	2	24
NC	1	1	8	0	0	1
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	100	132	144	25	32	256

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-6BG332C	4320	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-4FG484C	4320	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-5FG484C	4320	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-6FG484C	4320	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144C	6864	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-5TG144C	6864	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-6TG144C	6864	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-4BG256C	6864	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-5BG256C	6864	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-6BG256C	6864	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-4FTG256C	6864	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-5FTG256C	6864	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-6FTG256C	6864	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-4BG332C	6864	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-5BG332C	6864	1.2 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-6BG332C	6864	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-4FG484C	6864	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-5FG484C	6864	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-6FG484C	6864	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100IR1 <sup>1</sup>	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100IR1 <sup>1</sup>	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100IR1 <sup>1</sup>	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132IR1 <sup>1</sup>	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132IR1 <sup>1</sup>	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132IR1 <sup>1</sup>	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144IR1 <sup>1</sup>	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144IR1 <sup>1</sup>	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144IR1 <sup>1</sup>	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200ZE-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

# MachXO2 Family Data Sheet

## Revision History

March 2017

Data Sheet DS1035

Date	Version	Section	Change Summary
March 2017	3.3	DC and Switching Characteristics	Updated the <a href="#">Absolute Maximum Ratings</a> section. Added standards.
			Updated the <a href="#">sysIO Recommended Operating Conditions</a> section. Added standards.
			Updated the <a href="#">sysIO Single-Ended DC Electrical Characteristics</a> section. Added standards.
			Updated the <a href="#">MachXO2 External Switching Characteristics – HC/HE Devices</a> section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the $D_{VB}$ and the $D_{VA}$ parameters were changed to $D_{IB}$ and $D_{IA}$ . The parameter descriptions were also modified.
			Updated the <a href="#">MachXO2 External Switching Characteristics – ZE Devices</a> section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the $D_{VB}$ and the $D_{VA}$ parameters were changed to $D_{IB}$ and $D_{IA}$ . The parameter descriptions were also modified.
			Updated the <a href="#">sysCONFIG Port Timing Specifications</a> section. Corrected the $t_{INITL}$ units from ns to $\mu$ s.
		Pinout Information	Updated the <a href="#">Signal Descriptions</a> section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals.
			Updated the <a href="#">Pinout Information Summary</a> section. Added footnote to MachXO2-1200 32 QFN.
		Ordering Information	Updated the <a href="#">MachXO2 Part Number Description</a> section. Corrected the MG184, BG256, FTG256 package information. Added “(0.8 mm Pitch)” to BG332.
			Updated the <a href="#">Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging</a> section. — Updated LCMXO2-1200ZE-1UWG25ITR50 footnote. — Corrected footnote numbering typo. — Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2-2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s.

Date	Version	Section	Change Summary
May 2016	3.2	All	Moved designation for 84 QFN package information from 'Advanced' to 'Final'.
		Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 'Advanced' 48 QFN package. — Revised footnote 6. — Added footnote 9.
		DC and Switching Characteristics	Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Added footnote 12.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Added footnote 12.
		Pinout Information	Updated the Signal Descriptions section. Added information on GND signal.
			Updated the Pinout Information Summary section. — Added 'Advanced' MachXO2-256 48 QFN values. — Added 'Advanced' MachXO2-640 48 QFN values. — Added footnote to GND. — Added footnotes 2 and 3.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added 'Advanced' SG48 package and revised footnote.
Updated the Ordering Information section. — Added part numbers for 'Advanced' QFN 48 package.			
March 2016	3.1	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 32 QFN value for XO2-1200. — Added 84 QFN (7 mm x 7 mm, 0.5 mm) package. — Modified package name to 100-pin TQFP. — Modified package name to 144-pin TQFP. — Added footnote.
		Architecture	Updated the Typical I/O Behavior During Power-up section. Removed reference to TN1202.
		DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications section. Revised t <sub>DPPDONE</sub> and t <sub>DPPINIT</sub> Max. values per PCN 03A-16, released March 2016.
		Pinout Information	Updated the Pinout Information Summary section. — Added MachXO2-1200 32 QFN values. — Added 'Advanced' MachXO2-4000 84 QFN values.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added 'Advanced' QN84 package and footnote.
			Updated the Ordering Information section. — Added part numbers for 1280 LUTs QFN 32 package. — Added part numbers for 4320 LUTs QFN 84 package.
		March 2015	3.0
Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.		

Date	Version	Section	Change Summary
February 2012	01.7	All	Updated document with new corporate logo.
		—	Data sheet status changed from preliminary to final.
	01.6	Introduction	MachXO2 Family Selection Guide table – Removed references to 49-ball WLCSP.
		DC and Switching Characteristics	Updated Flash Download Time table.
			Modified Storage Temperature in the Absolute Maximum Ratings section.
			Updated $I_{DK}$ max in Hot Socket Specifications table.
			Modified Static Supply Current tables for ZE and HC/HE devices.
			Updated Power Supply Ramp Rates table.
			Updated Programming and Erase Supply Current tables.
			Updated data in the External Switching Characteristics table.
			Corrected Absolute Maximum Ratings for Dedicated Input Voltage Applied for LCMXO2 HC.
			DC Electrical Characteristics table – Minor corrections to conditions for $I_{IL}$ , $I_{IH}$ .
		Pinout Information	Removed references to 49-ball WLCSP.
			Signal Descriptions table – Updated description for GND, VCC, and VCCIOx.
			Updated Pin Information Summary table – Number of VCCIOs, GNDs, VCCs, and Total Count of Bonded Pins for MachXO2-256, 640, and 640U and Dual Function I/O for MachXO2-4000 332caBGA.
		Ordering Information	Removed references to 49-ball WLCSP
August 2011	01.5	DC and Switching Characteristics	Updated ESD information.
		Ordering Information	Updated footnote for ordering WLCSP devices.
	01.4	Architecture	Updated information in Clock/Control Distribution Network and sys-CLOCK Phase Locked Loops (PLLs).
		DC and Switching Characteristics	Updated $I_{IL}$ and $I_{IH}$ conditions in the DC Electrical Characteristics table.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Updated Pin Information Summary table: Dual Function I/O, DQS Groups Bank 1, Total General Purpose Single-Ended I/O, Differential I/O Per Bank, Total Count of Bonded Pins, Gearboxes.
			Added column of data for MachXO2-2000 49 WLCSP.
		Ordering Information	Updated R1 Device Specifications text section with information on migration from MachXO2-1200-R1 to Standard (non-R1) devices.
			Corrected Supply Voltage typo for part numbers: LCMXO2-2000UHE-4FG484I, LCMXO2-2000UHE-5FG484I, LCMXO2-2000UHE-6FG484I.
			Added footnote for WLCSP package parts.
		Supplemental Information	Removed reference to Stand-alone Power Calculator for MachXO2 Devices. Added reference to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices.