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Details

Product Status	Active
Number of LABs/CLBs	858
Number of Logic Elements/Cells	6864
Total RAM Bits	245760
Number of I/O	114
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-7000he-5tg144c

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MachXO2 Family Data Sheet Architecture

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Data Sheet DS1035

Architecture Overview

The MachXO2 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have sysCLOCK[™] PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.





Note: MachXO2-256, and MachXO2-640/U are similar to MachXO2-1200. MachXO2-256 has a lower LUT count and no PLL or EBR blocks. MachXO2-640 has no PLL, a lower LUT count and two EBR blocks. MachXO2-640U has a lower LUT count, one PLL and seven EBR blocks.

Figure 2-2. Top View of the MachXO2-4000 Device



Note: MachXO2-1200U, MachXO2-2000/U and MachXO2-7000 are similar to MachXO2-4000. MachXO2-1200U and MachXO2-2000 have a lower LUT count, one PLL, and eight EBR blocks. MachXO2-2000U has a lower LUT count, two PLLs, and 10 EBR blocks. MachXO2-7000 has a higher LUT count, two PLLs, and 26 EBR blocks.

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The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag "hard" control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysl/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2-640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO2 devices provide commonly used hardened functions such as SPI controller, I²C controller and timer/ counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I²C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

PFU Blocks

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.



Figure 2-3. PFU Block Diagram



Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

	PFU Block				
Slice	Resources	Modes			
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM			
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM			
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM			
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM			

Table 2-1. Resources and Modes Available per Slice

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.



Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO2 devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO2 devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

The MachXO2-640U, MachXO2-1200/U and higher density devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these higher density devices have on-chip differential termination and also provide PCI support.



Figure 2-17. Output Gearbox



More information on the output gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.



MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 devices contain three types of sysIO buffer pairs.

1. Left and Right sysIO Buffer Pairs

The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential and referenced input buffers.

2. Bottom sysIO Buffer Pairs

The sysIO buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential and referenced input buffers. Only the I/Os on the bottom banks have programmable PCI clamps and differential input termination. The PCI clamp is enabled after V_{CC} and V_{CCIO} are at valid operating levels and the device has been configured.

3. Top sysIO Buffer Pairs

The sysIO buffer pairs in the top bank of the device consist of two single-ended output drivers and two singleended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential and referenced I/O buffers. Half of the sysIO buffer pairs on the top edge have true differential outputs. The sysIO buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver. The referenced input buffer can also be configured as a differential input buffer.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCIO0} have reached V_{PORUP} level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pulldown to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to V_{CCIO} as the default functionality). The I/O pins will maintain the blank configuration until V_{CC} and V_{CCIO} (for I/O banks containing configuration I/Os) have reached V_{PORUP} levels at which time the I/Os will take on the user-configured settings only after a proper download/configuration.

Supported Standards

The MachXO2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL, and PCI. The buffer supports the LVTTL, PCI, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO2-640U, MachXO2-1200/U and higher devices support on-chip LVDS output buffers on approximately 50% of the I/Os on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO2 devices. PCI support is provided in the bottom bank of theMachXO2-640U, MachXO2-1200/U and higher density devices. Table 2-11 summarizes the I/O characteristics of the MachXO2 PLDs.

Tables 2-11 and 2-12 show the I/O standards (together with their supply and reference voltages) supported by the MachXO2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1202, MachXO2 sysIO Usage Guide.



Table 2-11. I/O Support Device by Device

	MachXO2-256, MachXO2-640	MachXO2-640U, MachXO2-1200	MachXO2-1200U MachXO2-2000/U, MachXO2-4000, MachXO2-7000
Number of I/O Banks	4	4	6
		Single-ended (all I/O banks)	Single-ended (all I/O banks)
Type of Input Buffers	Single-ended (all I/O banks)	Differential Receivers (all I/O	Differential Receivers (all I/O
	Differential Receivers (all I/O banks)	Differential input termination (bottom side)	Differential input termination (bottom side)
Turses of Output Duffers	Single-ended buffers with	Single-ended buffers with complementary outputs (all I/O banks)	Single-ended buffers with complementary outputs (all I/O banks)
Types of Output Bullers	banks)	Differential buffers with true LVDS outputs (50% on top side)	Differential buffers with true LVDS outputs (50% on top side)
Differential Output Emulation Capability	All I/O banks	All I/O banks	All I/O banks
PCI Clamp Support	No	Clamp on bottom side only	Clamp on bottom side only

Table 2-12. Supported Input Standards

	VCCIO (Typ.)					
Input Standard	3.3 V	2.5 V	1.8 V	1.5	1.2 V	
Single-Ended Interfaces						
LVTTL	✓	√ ²	√ ²	√ ²		
LVCMOS33	✓	√ ²	√ ²	√ ²		
LVCMOS25	√ ²	✓	√ ²	√ ²		
LVCMOS18	√ ²	√ ²	✓	√ ²		
LVCMOS15	√ ²	√ ²	√ ²	~	√ ²	
LVCMOS12	√ ²	√ ²	√ ²	√ ²	✓	
PCI ¹	✓					
SSTL18 (Class I, Class II)	✓	✓	✓			
SSTL25 (Class I, Class II)	✓	✓				
HSTL18 (Class I, Class II)	✓	✓	✓			
Differential Interfaces		•				
LVDS	✓	✓				
BLVDS, MVDS, LVPECL, RSDS	✓	✓				
MIPI ³	✓	✓				
Differential SSTL18 Class I, II	✓	✓	✓			
Differential SSTL25 Class I, II	✓	✓				
Differential HSTL18 Class I, II	✓	~	✓			

1. Bottom banks of MachXO2-640U, MachXO2-1200/U and higher density devices only.

2. Reduced functionality. Refer to TN1202, MachXO2 sysIO Usage Guide for more detail.

3. These interfaces can be emulated with external resistors in all devices.



There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology (Appendix B)
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices

Figure 2-22. SPI Core Block Diagram



Table 2-16 describes the signals interfacing with the SPI cores.

Table 2-16. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	0	Master	SPI master chip-select output
spi_csn[17]	0	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	0	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
ufm_sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the User Flash Memory (UFM).
cfg_stdby	0	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.
cfg_wake	0	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.



Static Supply Current – HC/HE Devices^{1, 2, 3, 6}

Symbol	Parameter	Device	Typ. ⁴	Units
		LCMXO2-256HC	1.15	mA
		LCMXO2-640HC	1.84	mA
		LCMXO2-640UHC	3.48	mA
		LCMXO2-1200HC	3.49	mA
I _{CC}	Core Power Supply	LCMXO2-1200UHC	4.80	mA
		LCMXO2-2000HC	4.80	mA
		LCMXO2-2000UHC	8.44	mA
		LCMXO2-4000HC	8.45	mA
		LCMXO2-7000HC	12.87	mA
		LCMXO2-2000HE	1.39	mA
		LCMXO2-4000HE	2.55	mA
		LCMXO2-7000HE	4.06	mA
I _{CCIO}	Bank Power Supply ⁵ $V_{CCIO} = 2.5 V$	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.

2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.

3. Frequency = 0 MHz.

4. $T_J = 25$ °C, power supplies at nominal voltage.

5. Does not include pull-up/pull-down.

6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Programming and Erase Flash Supply Current – HC/HE Devices^{1, 2, 3, 4}

Symbol	Parameter	Device	Typ.⁵	Units
		LCMXO2-256HC	14.6	mA
		LCMXO2-640HC	16.1	mA
		LCMXO2-640UHC	18.8	mA
		LCMXO2-1200HC	18.8	mA
I _{CC}		LCMXO2-1200UHC	22.1	mA
		LCMXO2-2000HC	22.1	mA
	Core Power Supply	LCMXO2-2000UHC	26.8	mA
		LCMXO2-4000HC	26.8	mA
		LCMXO2-7000HC	33.2	mA
		LCMXO2-2000HE	18.3	mA
		LCMXO2-2000UHE	20.4	mA
		LCMXO2-4000HE	20.4	mA
		LCMXO2-7000HE	23.9	mA
I _{CCIO}	Bank Power Supply ⁶	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.

2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.

3. Typical user pattern.

4. JTAG programming is at 25 MHz.

5. $T_J = 25$ °C, power supplies at nominal voltage.

6. Per bank. $V_{CCIO} = 2.5$ V. Does not include pull-up/pull-down.



sysIO Single-Ended DC Electrical Characteristics^{1, 2}

Input/Output	V	/IL	v _i	н	Vo. Max.	V _{OL} Max. V _{OH} Min.		lo⊔ Max.⁴
Standard	Min. (V) ³	Max. (V)	Min. (V)	Max. (V)	(V)	(V)	(mA)	(mA)
							4	-4
							8	-8
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	12	-12
LVTTL	-0.0	0.0	2.0	0.0			16	-16
							24	-24
					0.2	V _{CCIO} - 0.2	0.1	-0.1
							4	-4
					04	$V_{000} = 0.4$	8	-8
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	VCCI0 0.4	12	-12
						16	-16	
					0.2	V _{CCIO} - 0.2	0.1	-0.1
							4	-4
	0.2	0.25\/	0.651/	3.6	0.4	$V_{CCIO} - 0.4$	8	-8
	-0.3	0.33 v CCIO	0.03 A CCIO				12	-12
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
		0.4	V 04	4	-4			
LVCMOS 1.5 -0.	-0.3	0.35V _{CCIO}	0.65V _{CCIO}	3.6	0.4	V _{CCIO} – 0.4	8	-8
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
		-0.3 0.35V _{CCIO}	0.65V _{CCIO}	3.6	0.4	V 04	4	-2
LVCMOS 1.2	-0.3				0.4	VCCIO - 0.4	8	-6
					0.2	V _{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	0.3V _{CCIO}	0.5V _{CCIO}	3.6	0.1V _{CCIO}	0.9V _{CCIO}	1.5	-0.5
SSTL25 Class I	-0.3	V _{REF} - 0.18	V _{REF} + 0.18	3.6	0.54	V _{CCIO} - 0.62	8	8
SSTL25 Class II	-0.3	V _{REF} - 0.18	V _{REF} + 0.18	3.6	NA	NA	NA	NA
SSTL18 Class I	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	3.6	0.40	V _{CCIO} - 0.40	8	8
SSTL18 Class II	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	3.6	NA	NA	NA	NA
HSTL18 Class I	-0.3	V _{REF} – 0.1	V _{REF} + 0.1	3.6	0.40	V _{CCIO} - 0.40	8	8
HSTL18 Class II	-0.3	V _{REF} – 0.1	V _{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS25R33	-0.3	V _{REF} – 0.1	V _{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R33	-0.3	V _{REF} – 0.1	V _{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS18R25	-0.3	V _{REF} – 0.1	V _{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R33	-0.3	V _{REF} – 0.1	V _{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS15R25	-0.3	V _{REF} – 0.1	V _{REF} + 0.1	3.6	NA	NA	NA	NA
LVCMOS12R33	-0.3	V _{REF} – 0.1	V _{REF} + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	-0.3	V _{REF} – 0.1	V _{REF} + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	-0.3	V _{REF} – 0.1	V _{REF} + 0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain



LVDS Emulation

MachXO2 devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.





Note: All resistors are ±1%.

Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Тур.	Units
Z _{OUT}	Output impedance	20	Ohms
R _S	Driver series resistor	158	Ohms
R _P	Driver parallel resistor	140	Ohms
R _T	Receiver termination	100	Ohms
V _{OH}	Output high voltage	1.43	V
V _{OL}	Output low voltage	1.07	V
V _{OD}	Output differential voltage	0.35	V
V _{CM}	Output common mode voltage	1.25	V
Z _{BACK}	Back impedance	100.5	Ohms
I _{DC}	DC output current	6.03	mA



			-6		6 –		-5 -4		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Generic DDR	X2 Outputs with Clock and Data	Centered at Pin Using P	CLK Pin	for Cloc	k Input –	GDDRX	2_TX.EC	LK.Cen	tered ^{9, 12}
t _{DVB}	Output Data Valid Before CLK Output		0.535	_	0.670	_	0.830	_	ns
t _{DVA}	Output Data Valid After CLK Output	MachXO2-640U,	0.535	—	0.670	_	0.830	_	ns
f _{DATA}	DDRX2 Serial Output Data Speed	MacnXO2-1200/U and larger devices, top side	_	664	_	554	_	462	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		_	332	_	277	_	231	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139		116	MHz
Generic DDF	X4 Outputs with Clock and Data	a Aligned at Pin Using P	CLK Pin	for Cloc	k Input	- GDDR	X4_TX.E	CLK.Ali	gned ^{9, 12}
t _{DIA}	Output Data Invalid After CLK Output		_	0.200	_	0.215	_	0.230	ns
t _{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and	_	0.200	_	0.215	_	0.230	ns
f _{DATA}	DDRX4 Serial Output Data Speed	larger devices, top side only.	_	756	_	630	_	524	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency			378		315		262	MHz
f _{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDF	X4 Outputs with Clock and Data	Centered at Pin Using P	CLK Pin	for Cloc	k Input –	GDDRX	4_ TX.EC	LK.Cen	tered ^{9, 12}
t _{DVB}	Output Data Valid Before CLK Output		0.455	_	0.570	_	0.710	_	ns
t _{DVA}	Output Data Valid After CLK Output	MachXO2-640U,	0.455	_	0.570	_	0.710	_	ns
f _{DATA}	DDRX4 Serial Output Data Speed	larger devices, top side	_	756	_	630	_	524	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		_	378	_	315	_	262	MHz
f _{SCLK}	SCLK Frequency		_	95	—	79	—	66	MHz
7:1 LVDS Ou	utputs – GDDR71_TX.ECLK.7:	1 ^{9, 12}	•					•	
t _{DIB}	Output Data Invalid Before CLK Output		_	0.160	_	0.180	_	0.200	ns
t _{DIA}	Output Data Invalid After CLK Output	MachXO2-640U.	_	0.160	_	0.180	_	0.200	ns
f _{DATA}	DDR71 Serial Output Data Speed	MachXO2-1200/U and larger devices, top side	_	756	_	630	_	524	Mbps
f _{DDR71}	DDR71 ECLK Frequency	only.		378	—	315	_	262	MHz
fclkout	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		_	108	_	90	_	75	MHz



sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Modes			1		
t _{PRGM}	PROGRAMN low p	ulse accept	55		ns
t _{PRGMJ}	PROGRAMN low p	ulse rejection	—	25	ns
t _{INITL}	INITN low time	LCMXO2-256	—	30	μs
		LCMXO2-640	—	35	μs
		LCMXO2-640U/ LCMXO2-1200	_	55	μs
		LCMXO2-1200U/ LCMXO2-2000	—	70	μs
		LCMXO2-2000U/ LCMXO2-4000	—	105	μs
		LCMXO2-7000	—	130	μs
t _{DPPINIT}	PROGRAMN low to	D INITN Iow	—	150	ns
t _{DPPDONE}	PROGRAMN low to	DONE low	—	150	ns
t _{IODISS}	PROGRAMN low to I/O disable		—	120	ns
Slave SPI	·				
f _{MAX}	CCLK clock frequency		—	66	MHz
t _{ССLКН}	CCLK clock pulse v	CCLK clock pulse width high		—	ns
t _{CCLKL}	CCLK clock pulse v	CCLK clock pulse width low		_	ns
t _{STSU}	CCLK setup time		2	—	ns
t _{STH}	CCLK hold time		0	—	ns
t _{STCO}	CCLK falling edge	to valid output	—	10	ns
t _{STOZ}	CCLK falling edge	to valid disable	—	10	ns
t _{STOV}	CCLK falling edge	to valid enable	—	10	ns
t _{SCS}	Chip select high tim	ne	25	—	ns
t _{SCSS}	Chip select setup ti	me	3	—	ns
t _{SCSH}	Chip select hold tim	ne	3	—	ns
Master SPI					
f _{MAX}	MCLK clock freque	ncy	—	133	MHz
t _{MCLKH}	MCLK clock pulse v	width high	3.75	—	ns
t _{MCLKL}	MCLK clock pulse v	MCLK clock pulse width low		—	ns
t _{STSU}	MCLK setup time		5		ns
t _{STH}	MCLK hold time		1		ns
t _{CSSPI}	INITN high to chip	select low	100	200	ns
t _{MCLK}	INITN high to first N	MCLK edge	0.75	1	μs



MachXO2 Family Data Sheet Pinout Information

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Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
		[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).
		[Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.
		[A/B/C/D] indicates the PIO within the group to which the pad is connected.
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic.
		During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.
NC	—	No connect.
GND	_	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together. For QFN 48 package, the exposed die pad is the device ground.
VCC	_	V_{CC} – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIOx	_	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.
PLL and Clock Functi	ons (Us	ed as user-programmable I/O pins when not used for PLL or clock pins)
[LOC]_GPLL[T, C]_IN	_	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]		Primary Clock pads. One to three clock pads per side.
Test and Programming	g (Dual t	function pins used for test access port and during sysCONFIG™)
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
ТСК	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	0	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
		Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then:
JTAGENB	I	If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O.
		If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.
		For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.
Configuration (Dual fu	nction p	ins used during sysCONFIG)
PROGRAMN	I	Initiates configuration sequence when asserted low. During configuration, or when reserved as PROGRAMN in user mode, this pin always has an active pull-up.

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Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, or when reserved as INITn in user mode, this pin has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress. During configuration, or when reserved as DONE in user mode, this pin has an active pull-up.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.
SCL	I/O	Slave I ² C clock input and master I ² C clock output.
SDA	I/O	Slave I ² C data input and master I ² C data output.



Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32C	256	1.2 V	-1	Halogen-Free QFN	32	COM
LCMXO2-256ZE-2SG32C	256	1.2 V	-2	Halogen-Free QFN	32	COM
LCMXO2-256ZE-3SG32C	256	1.2 V	-3	Halogen-Free QFN	32	COM
LCMXO2-256ZE-1UMG64C	256	1.2 V	-1	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-2UMG64C	256	1.2 V	-2	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-3UMG64C	256	1.2 V	-3	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-1TG100C	256	1.2 V	-1	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-2TG100C	256	1.2 V	-2	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-3TG100C	256	1.2 V	-3	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-1MG132C	256	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-2MG132C	256	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-3MG132C	256	1.2 V	-3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100C	640	1.2 V	-1	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-2TG100C	640	1.2 V	-2	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-3TG100C	640	1.2 V	-3	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-1MG132C	640	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-2MG132C	640	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-3MG132C	640	1.2 V	-3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1SG32C	1280	1.2 V	-1	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-2SG32C	1280	1.2 V	-2	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-3SG32C	1280	1.2 V	-3	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-1TG100C	1280	1.2 V	-1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100C	1280	1.2 V	-2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100C	1280	1.2 V	-3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132C	1280	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132C	1280	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132C	1280	1.2 V	-3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144C	1280	1.2 V	-1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144C	1280	1.2 V	-2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144C	1280	1.2 V	-3	Halogen-Free TQFP	144	COM



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144C	6864	1.2 V	-1	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-2TG144C	6864	1.2 V	-2	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-3TG144C	6864	1.2 V	-3	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-1BG256C	6864	1.2 V	-1	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-2BG256C	6864	1.2 V	-2	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-3BG256C	6864	1.2 V	-3	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-1FTG256C	6864	1.2 V	-1	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-2FTG256C	6864	1.2 V	-2	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-3FTG256C	6864	1.2 V	-3	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-1BG332C	6864	1.2 V	-1	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-2BG332C	6864	1.2 V	-2	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-3BG332C	6864	1.2 V	-3	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-1FG484C	6864	1.2 V	-1	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-2FG484C	6864	1.2 V	-2	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-3FG484C	6864	1.2 V	-3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100CR11	1280	1.2 V	-1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100CR11	1280	1.2 V	-2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100CR11	1280	1.2 V	-3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132CR1 ¹	1280	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132CR11	1280	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132CR1 ¹	1280	1.2 V	-3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144CR1 ¹	1280	1.2 V	-1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144CR1 ¹	1280	1.2 V	-2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144CR1 ¹	1280	1.2 V	-3	Halogen-Free TQFP	144	COM

1. Specifications for the "LCMXO2-1200ZE-speed package CR1" are the same as the "LCMXO2-1200ZE-speed package C" devices respectively, except as specified in the R1 Device Specifications section of this data sheet.



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1UWG49ITR ¹	2112	1.2 V	-1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR50 ³	2112	1.2 V	-1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR1K ²	2112	1.2 V	-1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1TG100I	2112	1.2 V	-1	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-2TG100I	2112	1.2 V	-2	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-3TG100I	2112	1.2 V	-3	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-1MG132I	2112	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-2MG132I	2112	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-3MG132I	2112	1.2 V	-3	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-1TG144I	2112	1.2 V	-1	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-2TG144I	2112	1.2 V	-2	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-3TG144I	2112	1.2 V	-3	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-1BG256I	2112	1.2 V	-1	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-2BG256I	2112	1.2 V	-2	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-3BG256I	2112	1.2 V	-3	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-1FTG256I	2112	1.2 V	-1	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-2FTG256I	2112	1.2 V	-2	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-3FTG256I	2112	1.2 V	-3	Halogen-Free ftBGA	256	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.

2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.

3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4MG132I	4320	1.2 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-5MG132I	4320	1.2 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-6MG132I	4320	1.2 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-4TG144I	4320	1.2 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-5TG144I	4320	1.2 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-6TG144I	4320	1.2 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-4MG184I	4320	1.2 V	-4	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-5MG184I	4320	1.2 V	-5	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-6MG184I	4320	1.2 V	-6	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-4BG256I	4320	1.2 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-5BG256I	4320	1.2 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-6BG256I	4320	1.2 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-4FTG256I	4320	1.2 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-5FTG256I	4320	1.2 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-6FTG256I	4320	1.2 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-4BG332I	4320	1.2 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-5BG332I	4320	1.2 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-6BG332I	4320	1.2 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-4FG484I	4320	1.2 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-5FG484I	4320	1.2 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-6FG484I	4320	1.2 V	-6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144I	6864	1.2 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-5TG144I	6864	1.2 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-6TG144I	6864	1.2 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-4BG256I	6864	1.2 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-5BG256I	6864	1.2 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-6BG256I	6864	1.2 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-4FTG256I	6864	1.2 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-5FTG256I	6864	1.2 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-6FTG256I	6864	1.2 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-4BG332I	6864	1.2 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-5BG332I	6864	1.2 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-6BG332I	6864	1.2 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-4FG484I	6864	1.2 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-5FG484I	6864	1.2 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-6FG484I	6864	1.2 V	-6	Halogen-Free fpBGA	484	IND



MachXO2 Family Data Sheet Revision History

March 2017

Data Sheet DS1035

Date	Version	Section	Change Summary		
March 2017	1arch 2017 3.3	DC and Switching Characteristics	Updated the Absolute Maximum Ratings section. Added standards.		
			Updated the sysIO Recommended Operating Conditions section. Added standards.		
			Updated the sysIO Single-Ended DC Electrical Characteristics sec- tion. Added standards.		
			Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA} . The parameter descriptions were also modified.		
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA} . The parameter descriptions were also modified.		
				Updated the sysCONFIG Port Timing Specifications section. Corrected the t_{INITL} units from ns to μ s.	
		Pinout Information	Updated the Signal Descriptions section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals.		
					Updated the Pinout Information Summary section. Added footnote to MachXO2-1200 32 QFN.
	Ordering Informati		Ordering Information	Updated the MachXO2 Part Number Description section. Corrected the MG184, BG256, FTG256 package information. Added "(0.8 mm Pitch)" to BG332.	
			Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. — Updated LCMXO2-1200ZE-1UWG25ITR50 footnote. — Corrected footnote numbering typo. — Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2- 2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s.		

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