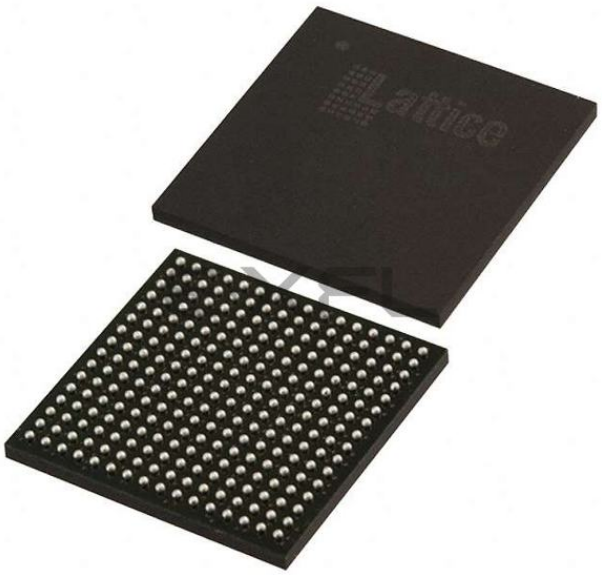
Lattice Semiconductor Corporation - LCMXO2-7000ZE-2FTG256C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

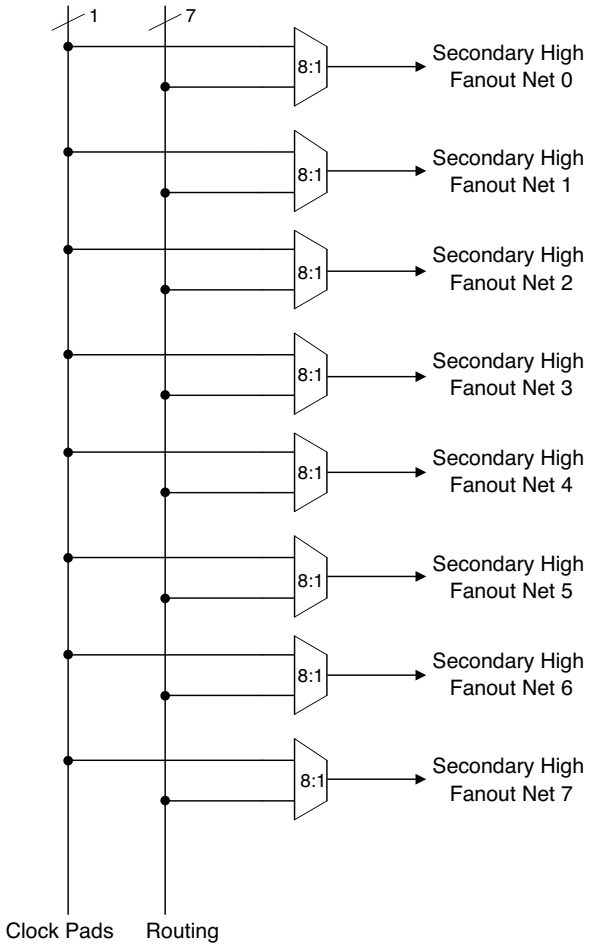
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	858
Number of Logic Elements/Cells	6864
Total RAM Bits	245760
Number of I/O	206
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-7000ze-2ftg256c

Figure 2-6. Secondary High Fanout Nets for MachXO2 Devices



sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The MachXO2-640U, MachXO2-1200/U and larger devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO2 sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO2 clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.

Figure 2-8. sysMEM Memory Primitives

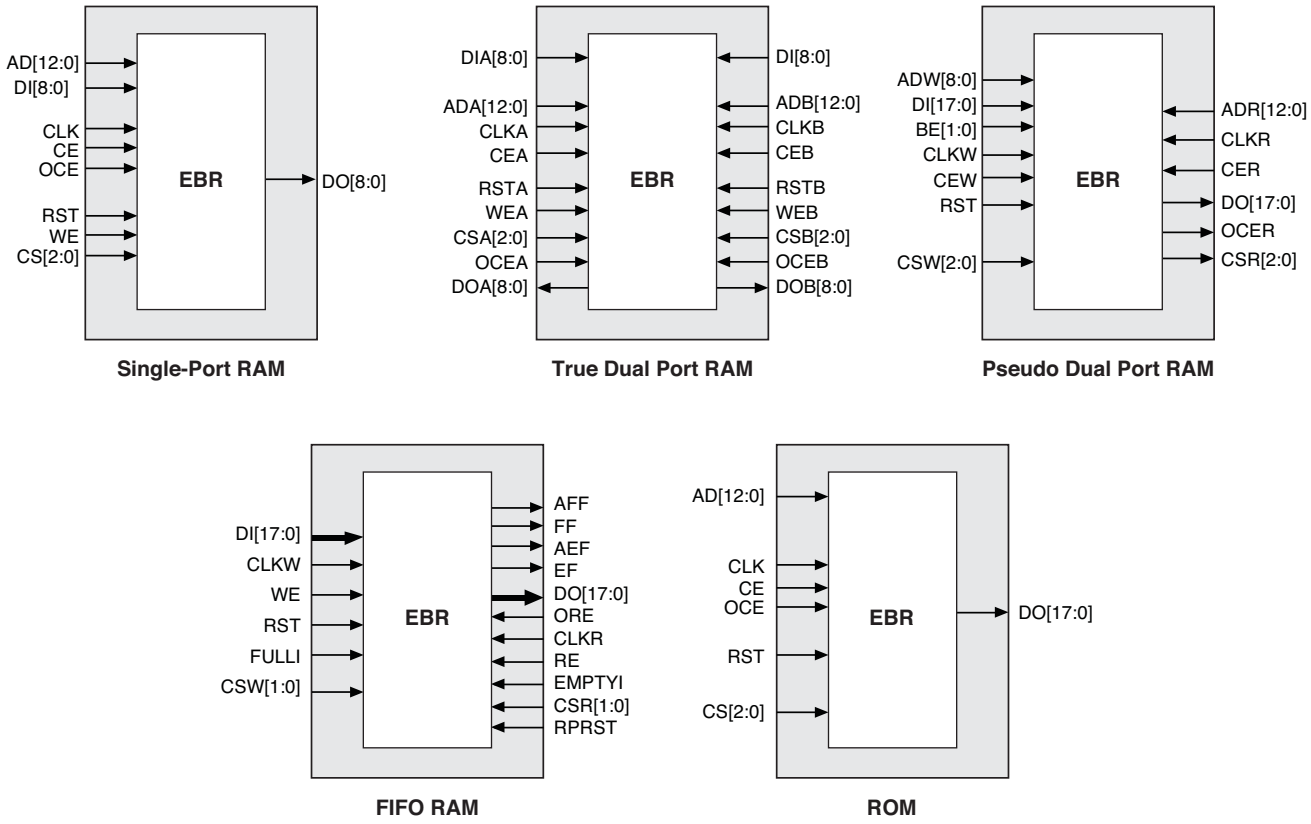


Table 2-6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE[1]	Output Clock Enable	Active High
RST	Reset	Active High
BE[1]	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	—
DI	Data In	—
DO	Data Out	—
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	—
FF	FIFO RAM Full Flag	—
AEF	FIFO RAM Almost Empty Flag	—
EF	FIFO RAM Empty Flag	—
RPRST	FIFO RAM Read Pointer Reset	—

1. Optional signals.
2. For dual port EBR primitives a trailing ‘A’ or ‘B’ in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing ‘R’ or ‘W’ in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

Table 2-13. Supported Output Standards

Output Standard	V_{CCIO} (Typ.)
Single-Ended Interfaces	
LVTTL	3.3
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8
LVCMOS15	1.5
LVCMOS12	1.2
LVCMOS33, Open Drain	—
LVCMOS25, Open Drain	—
LVCMOS18, Open Drain	—
LVCMOS15, Open Drain	—
LVCMOS12, Open Drain	—
PCI33	3.3
SSTL25 (Class I)	2.5
SSTL18 (Class I)	1.8
HSTL18(Class I)	1.8
Differential Interfaces	
LVDS[1, 2]	2.5, 3.3
BLVDS, MLVDS, RSDS [2]	2.5
LVPECL[2]	3.3
MIPI[2]	2.5
Differential SSTL18	1.8
Differential SSTL25	2.5
Differential HSTL18	1.8

1. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.

sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO2-1200U, MachXO2-2000/U and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO2-1200 and lower density devices have four banks (one bank per side). Figures 2-18 and 2-19 show the sysIO banks and their associated supplies for all devices.

Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  — Watchdog timer
  — Clear timer on compare match
  — Fast PWM
  — Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

Figure 2-23. Timer/Counter Block Diagram

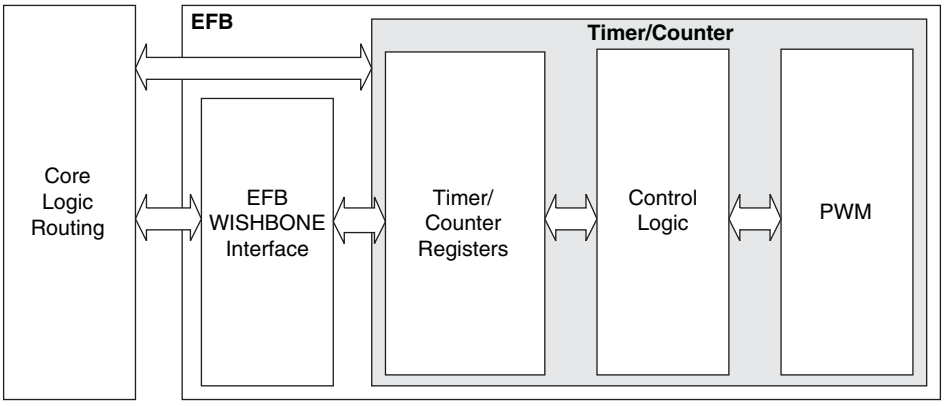


Table 2-17. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	O	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	O	Timer counter output signal

When implementing background programming of the on-chip Flash, care must be taken for the operation of the PLL. For devices that have two PLLs (XO2-2000U, -4000 and -7000), the system must put the RPLL (Right-side PLL) in reset state during the background Flash programming. More detailed description can be found in TN1204, MachXO2 Programming and Configuration Usage Guide.

Security and One-Time Programmable Mode (OTP)
For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO2 devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile Flash memory spaces. The device can be in one of two modes:

1. Unlocked – Readback of the SRAM configuration and non-volatile Flash memory spaces is allowed.

2. Permanently Locked – The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Dual Boot
MachXO2 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the on-chip Flash. The golden image MUST reside in an external SPI Flash. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Soft Error Detection
The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1206, MachXO2 Soft Error Detection Usage Guide.

TraceID

Each MachXO2 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I^2C, or JTAG interfaces.

Density Shifting

The MachXO2 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO2 migration files.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max.[4] (mA)	I_{OH} Max.[4] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS10R25	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain

1. MachXO2 devices allow LVCMOS inputs to be placed in I/O banks where V_{CCIO} is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO2 devices do not meet the relevant JEDEC specification are documented in the table below.
2. MachXO2 devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1202, MachXO2 sysIO Usage Guide.
3. The dual function I^2C pins SCL and SDA are limited to a V_{IL} min of –0.25 V or to –0.3 V with a duration of <10 ns.
4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive VCCIO or GND pad connections, or between the last VCCIO or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n * 8 mA. “n” is the number of I/O pads between the two consecutive bank VCCIO or GND connections or between the last VCCIO and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

Input Standard	V_{CCIO} (V)	V_{IL} Max. (V)
LVCMOS 33	1.5	0.685
LVCMOS 25	1.5	0.687
LVCMOS 18	1.5	0.655

sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of MachXO2-640U, MachXO2-1200/U and higher density devices in the MachXO2 PLD family.

LVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO} = 3.3 V	0	—	2.605	V
		V_{CCIO} = 2.5 V	0	—	2.05	V
V_{THD}	Differential Input Threshold		±100	—		mV
V_{CM}	Input Common Mode Voltage	V_{CCIO} = 3.3 V	0.05	—	2.6	V
		V_{CCIO} = 2.5 V	0.05	—	2.0	V
I_{IN}	Input current	Power on	—	—	±10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.375	—	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.90	1.025	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.395	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0 V driver outputs shorted	—	—	24	mA

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HPLL}	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	0.41	—	0.48	—	0.55	—	ns
		MachXO2-2000HC-HE	0.42	—	0.49	—	0.56	—	ns
		MachXO2-4000HC-HE	0.43	—	0.50	—	0.58	—	ns
		MachXO2-7000HC-HE	0.46	—	0.54	—	0.62	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	2.88	—	3.19	—	3.72	—	ns
		MachXO2-2000HC-HE	2.87	—	3.18	—	3.70	—	ns
		MachXO2-4000HC-HE	2.96	—	3.28	—	3.81	—	ns
		MachXO2-7000HC-HE	3.05	—	3.35	—	3.87	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-2000HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-4000HC-HE	–0.87	—	–0.87	—	–0.87	—	ns
		MachXO2-7000HC-HE	–0.91	—	–0.91	—	–0.91	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.317	—	0.344	—	0.368	UI
t_{DVE}	Input Data Hold After CLK		0.742	—	0.702	—	0.668	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	All MachXO2 devices, all sides	0.566	—	0.560	—	0.538	—	ns
t_{HO}	Input Data Hold After CLK		0.778	—	0.879	—	1.090	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.316	—	0.342	—	0.364	UI
t_{DVE}	Input Data Hold After CLK		0.710	—	0.675	—	0.679	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.233	—	0.219	—	0.198	—	ns
t_{HO}	Input Data Hold After CLK		0.287	—	0.287	—	0.344	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.535	—	0.670	—	0.830	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	0.830	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	—	231	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[9, 12]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[9, 12]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.455	—	0.570	—	0.710	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.455	—	0.570	—	0.710	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	378	—	315	—	262	MHz
f_{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[9, 12]									
t_{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.160	—	0.180	—	0.200	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.160	—	0.180	—	0.200	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HPLL}	Clock to Data Hold – PIO Input Register	MachXO2-1200ZE	0.66	—	0.68	—	0.80	—	ns
		MachXO2-2000ZE	0.68	—	0.70	—	0.83	—	ns
		MachXO2-4000ZE	0.68	—	0.71	—	0.84	—	ns
		MachXO2-7000ZE	0.73	—	0.74	—	0.87	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200ZE	5.14	—	5.69	—	6.20	—	ns
		MachXO2-2000ZE	5.11	—	5.67	—	6.17	—	ns
		MachXO2-4000ZE	5.27	—	5.84	—	6.35	—	ns
		MachXO2-7000ZE	5.15	—	5.71	—	6.23	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200ZE	–1.36	—	–1.36	—	–1.36	—	ns
		MachXO2-2000ZE	–1.35	—	–1.35	—	–1.35	—	ns
		MachXO2-4000ZE	–1.43	—	–1.43	—	–1.43	—	ns
		MachXO2-7000ZE	–1.41	—	–1.41	—	–1.41	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.382	—	0.401	—	0.417	UI
t_{DVE}	Input Data Hold After CLK		0.670	—	0.684	—	0.693	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	All MachXO2 devices, all sides	1.319	—	1.412	—	1.462	—	ns
t_{HO}	Input Data Hold After CLK		0.717	—	1.010	—	1.340	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	140	—	116	—	98	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.361	—	0.346	—	0.334	UI
t_{DVE}	Input Data Hold After CLK		0.602	—	0.625	—	0.648	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 12]									
t_{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	0.472	—	0.672	—	0.865	—	ns
t_{HO}	Input Data Hold After CLK		0.363	—	0.501	—	0.743	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	—	194	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	—	97	MHz
f_{SCLK}	SCLK Frequency		—	70	—	59	—	49	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input - GDDRX4_RX.ECLK.Aligned[9, 12]									
t_{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11]	—	0.307	—	0.316	—	0.326	UI
t_{DVE}	Input Data Hold After ECLK		0.662	—	0.650	—	0.649	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	420	—	352	—	292	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	210	—	176	—	146	MHz
f_{SCLK}	SCLK Frequency		—	53	—	44	—	37	MHz

Figure 3-5. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms

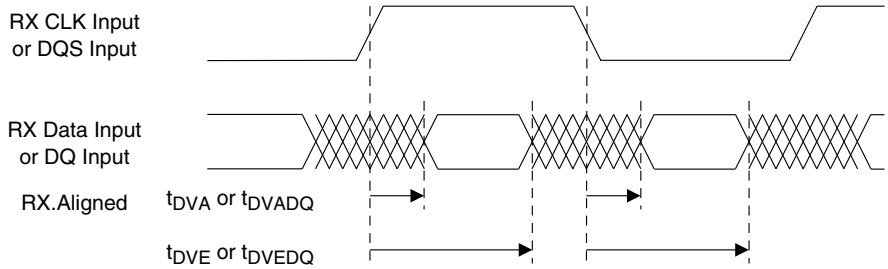


Figure 3-6. Receiver RX.CLK.Centered Waveforms

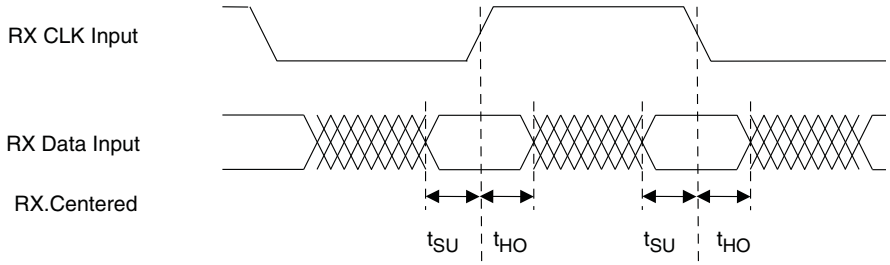


Figure 3-7. Transmitter TX.CLK.Aligned Waveforms

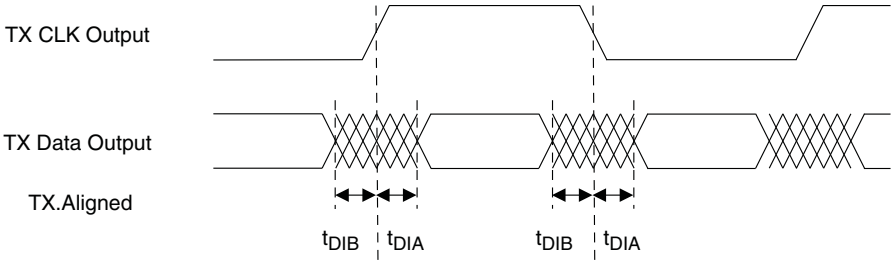
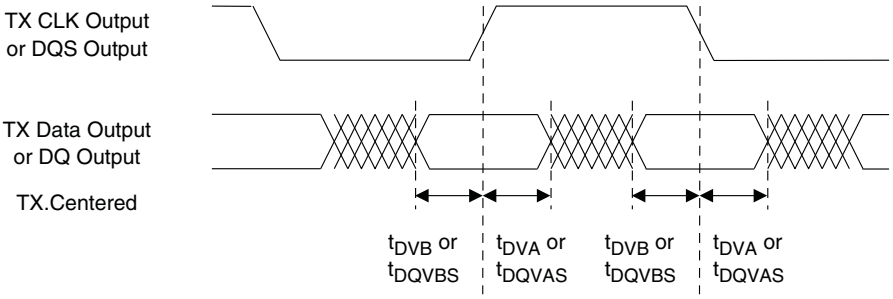


Figure 3-8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms



sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Modes					
t_{PRGM}	PROGRAMN low pulse accept		55	—	ns
t_{PRGMJ}	PROGRAMN low pulse rejection		—	25	ns
t_{INITL}	INITN low time	LCMXO2-256	—	30	µs
		LCMXO2-640	—	35	µs
		LCMXO2-640U/ LCMXO2-1200	—	55	µs
		LCMXO2-1200U/ LCMXO2-2000	—	70	µs
		LCMXO2-2000U/ LCMXO2-4000	—	105	µs
		LCMXO2-7000	—	130	µs
$t_{DPPINIT}$	PROGRAMN low to INITN low		—	150	ns
$t_{DPPDONE}$	PROGRAMN low to DONE low		—	150	ns
t_{IODISS}	PROGRAMN low to I/O disable		—	120	ns
Slave SPI					
f_{MAX}	CCLK clock frequency		—	66	MHz
t_{CCLKH}	CCLK clock pulse width high		7.5	—	ns
t_{CCLKL}	CCLK clock pulse width low		7.5	—	ns
t_{STSU}	CCLK setup time		2	—	ns
t_{STH}	CCLK hold time		0	—	ns
t_{STCO}	CCLK falling edge to valid output		—	10	ns
t_{STOZ}	CCLK falling edge to valid disable		—	10	ns
t_{STOV}	CCLK falling edge to valid enable		—	10	ns
t_{SCS}	Chip select high time		25	—	ns
t_{SCSS}	Chip select setup time		3	—	ns
t_{SCSH}	Chip select hold time		3	—	ns
Master SPI					
f_{MAX}	MCLK clock frequency		—	133	MHz
t_{MCLKH}	MCLK clock pulse width high		3.75	—	ns
t_{MCLKL}	MCLK clock pulse width low		3.75	—	ns
t_{STSU}	MCLK setup time		5	—	ns
t_{STH}	MCLK hold time		1	—	ns
t_{CSSPI}	INITN high to chip select low		100	200	ns
t_{MCLK}	INITN high to first MCLK edge		0.75	1	µs

	MachXO2-4000							
	84 QFN	132 csBGA	144 TQFP	184 csBGA	256 caBGA	256 ftBGA	332 caBGA	484 fpBGA
General Purpose I/O per Bank								
Bank 0	27	25	27	37	50	50	68	70
Bank 1	10	26	29	37	52	52	68	68
Bank 2	22	28	29	39	52	52	70	72
Bank 3	0	7	9	10	16	16	24	24
Bank 4	9	8	10	12	16	16	16	16
Bank 5	0	10	10	15	20	20	28	28
Total General Purpose Single Ended I/O	68	104	114	150	206	206	274	278
Differential I/O per Bank								
Bank 0	13	13	14	18	25	25	34	35
Bank 1	4	13	14	18	26	26	34	34
Bank 2	11	14	14	19	26	26	35	36
Bank 3	0	3	4	4	8	8	12	12
Bank 4	4	4	5	6	8	8	8	8
Bank 5	0	5	5	7	10	10	14	14
Total General Purpose Differential I/O	32	52	56	72	103	103	137	139
Dual Function I/O	28	37	37	37	37	37	37	37
High-speed Differential I/O								
Bank 0	8	8	9	8	18	18	18	18
Gearboxes								
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	8	8	9	9	18	18	18	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	11	14	14	12	18	18	18	18
DQS Groups								
Bank 1	1	2	2	2	2	2	2	2
VCCIO Pins								
Bank 0	3	3	3	3	4	4	4	10
Bank 1	1	3	3	3	4	4	4	10
Bank 2	2	3	3	3	4	4	4	10
Bank 3	1	1	1	1	1	1	2	3
Bank 4	1	1	1	1	2	2	1	4
Bank 5	1	1	1	1	1	1	2	3
VCC	4	4	4	4	8	8	8	12
GND	4	10	12	16	24	24	27	48
NC	1	1	1	1	1	1	5	105
Reserved for configuration	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	84	132	144	184	256	256	332	484

MachXO2 Family Data Sheet Ordering Information

MachXO2 Part Number Description

LCMXO2 – XXXX X X X – X XXXXXX X XX XX

Device Family
MachXO2 PLD

Logic Capacity
256 = 256 LUTs
640 = 640 LUTs
1200 = 1280 LUTs
2000 = 2112 LUTs
4000 = 4320 LUTs
7000 = 6864 LUTs

I/O Count
Blank = Standard Device
U = Ultra High I/O Device

Power/Performance
Z = Low Power
H = High Performance

Supply Voltage
C = 2.5 V / 3.3 V
E = 1.2 V

Speed
1 = Slowest
2
3 = Fastest
} Low Power

4 = Slowest
5
6 = Fastest
} High Performance

Device Status
Blank = Production Device
ES = Engineering Sample
R1 = Production Release 1 Device
1K = WLCSP Package, 1,000 parts per reel

Shipping Method
Blank = Trays
TR = Tape and Reel

Grade
C = Commercial
I = Industrial

Package
UWG25 = 25-Ball Halogen-Free WLCSP (0.4 mm Pitch)
SG32 = 32-Pin Halogen-Free QFN (0.5 mm Pitch)
SG48 = 48-Pin Halogen-Free QFN (0.5 mm Pitch)
UWG49 = 49-ball Halogen-Free WLCSP (0.4 mm Pitch)
UMG64 = 64-Ball Halogen-Free ucBGA (0.4 mm Pitch)
QN84 = 84-Pin Halogen-Free QFN (0.5 mm Pitch)
TG100 = 100-Pin Halogen-Free TQFP
TG144 = 144-Pin Halogen-Free TQFP
MG132 = 132-Ball Halogen-Free csBGA (0.5 mm Pitch)
MG184 = 184-Ball Halogen-Free csBGA (0.5 mm Pitch)
BG256 = 256-Ball Halogen-Free caBGA (0.8 mm Pitch)
FTG256 = 256-Ball Halogen-Free ftBGA (1.0 mm Pitch)
BG332 = 332-Ball Halogen-Free caBGA (0.8 mm Pitch)
FG484 = 484-Ball Halogen-Free fpBGA (1.0 mm Pitch)

* 48-pin QFN information is 'Advanced'.

Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32C	256	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-256ZE-2SG32C	256	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-256ZE-3SG32C	256	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-256ZE-1UMG64C	256	1.2 V	–1	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-2UMG64C	256	1.2 V	–2	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-3UMG64C	256	1.2 V	–3	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-1TG100C	256	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-2TG100C	256	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-3TG100C	256	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-1MG132C	256	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-2MG132C	256	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-3MG132C	256	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100C	640	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-2TG100C	640	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-3TG100C	640	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-1MG132C	640	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-2MG132C	640	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-3MG132C	640	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1SG32C	1280	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-2SG32C	1280	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-3SG32C	1280	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-1TG100C	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100C	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100C	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132C	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132C	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132C	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144C	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144C	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144C	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144C	6864	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-2TG144C	6864	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-3TG144C	6864	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-1BG256C	6864	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-2BG256C	6864	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-3BG256C	6864	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-1FTG256C	6864	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-2FTG256C	6864	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-3FTG256C	6864	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-1BG332C	6864	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-2BG332C	6864	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-3BG332C	6864	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-1FG484C	6864	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-2FG484C	6864	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-3FG484C	6864	1.2 V	–3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100CR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100CR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100CR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132CR1[1]	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132CR1[1]	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132CR1[1]	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144CR1[1]	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144CR1[1]	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144CR1[1]	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200ZE-speed package CR1” are the same as the “LCMXO2-1200ZE-speed package C” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-6BG332C	4320	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-4FG484C	4320	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-5FG484C	4320	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-6FG484C	4320	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144C	6864	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-5TG144C	6864	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-6TG144C	6864	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-4BG256C	6864	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-5BG256C	6864	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-6BG256C	6864	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-4FTG256C	6864	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-5FTG256C	6864	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-6FTG256C	6864	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-4BG332C	6864	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-5BG332C	6864	1.2 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-6BG332C	6864	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-4FG484C	6864	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-5FG484C	6864	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-6FG484C	6864	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000ZE-1QN84I	4320	1.2 V	–1	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-2QN84I	4320	1.2 V	–2	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-3QN84I	4320	1.2 V	–3	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-1MG132I	4320	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-2MG132I	4320	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-3MG132I	4320	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-1TG144I	4320	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-2TG144I	4320	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-3TG144I	4320	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-1BG256I	4320	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-2BG256I	4320	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-3BG256I	4320	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-1FTG256I	4320	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-2FTG256I	4320	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-3FTG256I	4320	1.2 V	–3	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-1BG332I	4320	1.2 V	–1	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-2BG332I	4320	1.2 V	–2	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-3BG332I	4320	1.2 V	–3	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-1FG484I	4320	1.2 V	–1	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-2FG484I	4320	1.2 V	–2	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-3FG484I	4320	1.2 V	–3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144I	6864	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-2TG144I	6864	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-3TG144I	6864	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-1BG256I	6864	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-2BG256I	6864	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-3BG256I	6864	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-1FTG256I	6864	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-2FTG256I	6864	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-3FTG256I	6864	1.2 V	–3	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-1BG332I	6864	1.2 V	–1	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-2BG332I	6864	1.2 V	–2	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-3BG332I	6864	1.2 V	–3	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-1FG484I	6864	1.2 V	–1	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-2FG484I	6864	1.2 V	–2	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-3FG484I	6864	1.2 V	–3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4MG132I	4320	1.2 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-5MG132I	4320	1.2 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-6MG132I	4320	1.2 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-4TG144I	4320	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-5TG144I	4320	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-6TG144I	4320	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-4MG184I	4320	1.2 V	–4	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-5MG184I	4320	1.2 V	–5	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-6MG184I	4320	1.2 V	–6	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-4BG256I	4320	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-5BG256I	4320	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-6BG256I	4320	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-4FTG256I	4320	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-5FTG256I	4320	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-6FTG256I	4320	1.2 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-4BG332I	4320	1.2 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-5BG332I	4320	1.2 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-6BG332I	4320	1.2 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-4FG484I	4320	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-5FG484I	4320	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-6FG484I	4320	1.2 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144I	6864	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-5TG144I	6864	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-6TG144I	6864	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-4BG256I	6864	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-5BG256I	6864	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-6BG256I	6864	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-4FTG256I	6864	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-5FTG256I	6864	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-6FTG256I	6864	1.2 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-4BG332I	6864	1.2 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-5BG332I	6864	1.2 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-6BG332I	6864	1.2 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-4FG484I	6864	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-5FG484I	6864	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-6FG484I	6864	1.2 V	–6	Halogen-Free fpBGA	484	IND

MachXO2 Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the MachXO2 family are available on the Lattice web site.

- TN1198, Power Estimation and Management for MachXO2 Devices
- TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide
- TN1201, Memory Usage Guide for MachXO2 Devices
- TN1202, MachXO2 sysIO Usage Guide
- TN1203, Implementing High-Speed Interfaces with MachXO2 Devices
- TN1204, MachXO2 Programming and Configuration Usage Guide
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices
- TN1206, MachXO2 SRAM CRC Error Detection Usage Guide
- TN1207, Using TraceID in MachXO2 Devices
- TN1074, PCB Layout Recommendations for BGA Packages
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices
- AN8066, Boundary Scan Testability with Lattice sysIO Capability
- MachXO2 Device Pinout Files
- Thermal Management document
- Lattice design tools

For further information on interface standards, refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, LVDS, DDR, DDR2, LPDDR): www.jedec.org
- PCI: www.pcisig.com

Date	Version	Section	Change Summary
February 2012	01.7	All	Updated document with new corporate logo.
	01.6	—	Data sheet status changed from preliminary to final.
		Introduction	MachXO2 Family Selection Guide table – Removed references to 49-ball WLCSP.
		DC and Switching Characteristics	Updated Flash Download Time table.
			Modified Storage Temperature in the Absolute Maximum Ratings section.
			Updated I_{DK} max in Hot Socket Specifications table.
			Modified Static Supply Current tables for ZE and HC/HE devices.
			Updated Power Supply Ramp Rates table.
			Updated Programming and Erase Supply Current tables.
			Updated data in the External Switching Characteristics table.
			Corrected Absolute Maximum Ratings for Dedicated Input Voltage Applied for LCMXO2 HC.
			DC Electrical Characteristics table – Minor corrections to conditions for I_{IL}, I_{IH}.
		Pinout Information	Removed references to 49-ball WLCSP.
			Signal Descriptions table – Updated description for GND, VCC, and VCCIOx.
			Updated Pin Information Summary table – Number of VCCIOs, GNDs, VCCs, and Total Count of Bonded Pins for MachXO2-256, 640, and 640U and Dual Function I/O for MachXO2-4000 332caBGA.
		Ordering Information	Removed references to 49-ball WLCSP
August 2011	01.5	DC and Switching Characteristics	Updated ESD information.
		Ordering Information	Updated footnote for ordering WLCSP devices.
	01.4	Architecture	Updated information in Clock/Control Distribution Network and sysCLOCK Phase Locked Loops (PLLs).
		DC and Switching Characteristics	Updated I_{IL} and I_{IH} conditions in the DC Electrical Characteristics table.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Updated Pin Information Summary table: Dual Function I/O, DQS Groups Bank 1, Total General Purpose Single-Ended I/O, Differential I/O Per Bank, Total Count of Bonded Pins, Gearboxes. Added column of data for MachXO2-2000 49 WLCSP.
		Ordering Information	Updated R1 Device Specifications text section with information on migration from MachXO2-1200-R1 to Standard (non-R1) devices.
			Corrected Supply Voltage typo for part numbers: LCMX02-2000UHE-4FG484I, LCMX02-2000UHE-5FG484I, LCMX02-2000UHE-6FG484I.
			Added footnote for WLCSP package parts.
		Supplemental Information	Removed reference to Stand-alone Power Calculator for MachXO2 Devices. Added reference to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices.