E. Semiconductor Corporation - LCMX02-7000ZE-2TG144I Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	858
Number of Logic Elements/Cells	6864
Total RAM Bits	245760
Number of I/O	114
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-7000ze-2tg144i

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Table 1-1. MachXO2™ Family Selection Guide

		XO2-256	XO2-640	XO2-640U ¹	XO2-1200	XO2-1200U ¹	XO2-2000	XO2-2000U1	XO2-4000	XO2-7000
LUTs		256	640	640	1280	1280	2112	2112	4320	6864
Distributed RAM (kbits)		2	5	5	10	10	16	16	34	54
EBR SRAM (kbits)		0	18	64	64	74	74	92	92	240
Number of EBR SR kbits/block)	AM Blocks (9	0	2	7	7	8	8	10	10	26
UFM (kbits)		0	24	64	64	80	80	96	96	256
Device Options:	HC ²	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	HE ³						Yes	Yes	Yes	Yes
	ZE ⁴	Yes	Yes		Yes		Yes		Yes	Yes
Number of PLLs		0	0	1	1	1	1	2	2	2
Hardened	I2C	2	2	2	2	2	2	2	2	2
Functions:	SPI	1	1	1	1	1	1	1	1	1
	Timer/Coun- ter	1	1	1	1	1	1	1	1	1
Packages	1					ю				
25-ball WLCSP⁵ (2.5 mm x 2.5 mm, 0.4 mm)					18					
32 QFN ⁶ (5 mm x 5 mm, 0.5 mm)		21			21					
48 QFN ^{8. 9} (7 mm x 7 mm, 0.5 mm)		40	40							
49-ball WLCSP⁵ (3.2 mm x 3.2 mm, 0.4 mm)							38			
64-ball ucBGA (4 mm x 4 mm, 0.4 mm)		44								
84 QFN ⁷ (7 mm x 7 mm, 0.5 mm)									68	
100-pin TQFP (14 mm x 14 mm)		55	78		79		79			
132-ball csBGA (8 mm x 8 mm, 0.5 mm)		55	79		104		104		104	
144-pin TQFP (20 mm x 20 mm)				107	107		111		114	114
184-ball csBGA ⁷ (8 mm x 8 mm, 0.5 mm)									150	
256-ball caBGA (14 mm x 14 mm, 0.8 mm)							206		206	206
256-ball ftBGA (17 mm x 17 mm, 1.0 mm)						206	206		206	206
332-ball caBGA (17 mm x 17 mm, 0	.8 mm)								274	278
484-ball ftBGA (23 mm x 23 mm, 1	.0 mm)							278	278	334

1. Ultra high I/O device.

2. High performance with regulator – VCC = 2.5 V, 3.3 V

3. High performance without regulator $-V_{CC} = 1.2 V$ 4. Low power without regulator $-V_{CC} = 1.2 V$ 5. WLCSP package only available for ZE devices.

6. 32 QFN package only available for HC and ZE devices.

7. 184 csBGA package only available for HE devices.

8. 48-pin QFN information is 'Advanced'.

9. 48 QFN package only available for HC devices.



Hot Socketing

The MachXO2 devices have been carefully designed to ensure predictable behavior during power-up and powerdown. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO2 ideal for many multiple power supply and hot-swap applications.

On-chip Oscillator

Every MachXO2 device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

- 1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
- 2. During configuration, users select a different master clock frequency.
- 3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
- 4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-14 lists all the available MCLK frequencies.

Table 2-14. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

Embedded Hardened IP Functions and User Flash Memory

All MachXO2 devices provide embedded hardened functions such as SPI, I²C and Timer/Counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2-20.



Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
 - Watchdog timer
 - Clear timer on compare match
 - Fast PWM
 - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- · Stand-alone mode with preloaded control registers and direct reset input

Figure 2-23. Timer/Counter Block Diagram



Table 2-17. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	0	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	0	Timer counter output signal



When implementing background programming of the on-chip Flash, care must be taken for the operation of the PLL. For devices that have two PLLs (XO2-2000U, -4000 and -7000), the system must put the RPLL (Right-side PLL) in reset state during the background Flash programming. More detailed description can be found in TN1204, MachXO2 Programming and Configuration Usage Guide.

Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO2 devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile Flash memory spaces. The device can be in one of two modes:

- 1. Unlocked Readback of the SRAM configuration and non-volatile Flash memory spaces is allowed.
- 2. Permanently Locked The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Dual Boot

MachXO2 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the on-chip Flash. The golden image MUST reside in an external SPI Flash. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1206, MachXO2 Soft Error Detection Usage Guide.

TraceID

Each MachXO2 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I²C, or JTAG interfaces.

Density Shifting

The MachXO2 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO2 migration files.



Power-On-Reset Voltage Levels^{1, 2, 3, 4, 5}

Symbol	Parameter	Min.	Тур.	Max.	Units
V _{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and $V_{CCIO0})$	0.9	_	1.06	V
V _{PORUPEXT}	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	_	2.1	V
V _{PORDNBG}	Power-On-Reset ramp down trip point (band gap based circuit monitoring $V_{CCINT})$	0.75	_	0.93	V
V _{PORDNBGEXT}	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	_	1.33	V
V _{PORDNSRAM}	Power-On-Reset ramp down trip point (SRAM based circuit monitoring $V_{\mbox{CCINT}}$)	-	0.6	_	V
V _{PORDNSRAMEXT}	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	_	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.

3. Note that V_{PORUP} (min.) and V_{PORDNBG} (max.) are in different process corners. For any given process corner V_{PORDNBG} (max.) is always 12.0 mV below V_{PORUP} (min.).

4. V_{PORUPEXT} is for HC devices only. In these devices a separate POR circuit monitors the external V_{CC} power supply.

5. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

Programming/Erase Specifications

Symbol	Parameter	Min.	Max. ¹	Units
	Flash Programming cycles per t _{RETENTION}	—	10,000	Cycles
PROGCYC	Flash functional programming cycles	—	100,000	Oycles
t	Data retention at 100 °C junction temperature	10	—	Voars
RETENTION	Data retention at 85 °C junction temperature	20	—	leais

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

Hot Socketing Specifications^{1, 2, 3}

I_{DK} Input or I/O leakage Current $0 < V_{IN} < V_{IH}$ (MAX) +/-1000 μ A	Symbol	Parameter	Condition	Max.	Units
	I _{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/-1000	μΑ

1. Insensitive to sequence of V_{CC} and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO} .

2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).

3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

ESD Performance

Please refer to the MachXO2 Product Family Qualification Summary for complete qualification data, including ESD performance.



Static Supply Current – ZE Devices^{1, 2, 3, 6}

Symbol	Parameter	Device	Typ.⁴	Units
		LCMXO2-256ZE	18	μΑ
		LCMXO2-640ZE	28	μΑ
1	Coro Power Supply	LCMXO2-1200ZE	56	μΑ
ICC	LCMXO2-640ZE 28 Core Power Supply LCMXO2-1200ZE 56 LCMXO2-2000ZE 80 LCMXO2-4000ZE 124 LCMXO2-7000ZE 189	LCMXO2-2000ZE	80	μΑ
		124	μΑ	
		LCMXO2-7000ZE	189	μA
Iccio	Bank Power Supply⁵ V _{CCIO} = 2.5 V	All devices	1	μΑ

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.

Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off. To estimate the impact of turning each of these items on, please refer to the following table or for more detail with your specific design use the Power Calculator tool.

3. Frequency = 0 MHz.

4. $T_J = 25$ °C, power supplies at nominal voltage.

5. Does not include pull-up/pull-down.

6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Static Power Consumption Contribution of Different Components – ZE Devices

The table below can be used for approximating static power consumption. For a more accurate power analysis for your design please use the Power Calculator tool.

Symbol	Parameter	Тур.	Units
I _{DCBG}	Bandgap DC power contribution	101	μΑ
IDCPOR	POR DC power contribution	38	μΑ
IDCIOBANKCONTROLLER	DC power contribution per I/O bank controller	143	μΑ



Programming and Erase Flash Supply Current – ZE Devices^{1, 2, 3, 4}

Symbol	Parameter	Device	Typ.⁵	Units
		LCMXO2-256ZE	13	mA
		LCMXO2-640ZE	14	mA
1	Core Power Supply	LCMXO2-1200ZE	15	mA
ICC		LCMXO2-2000ZE	17	mA
		LCMXO2-4000ZE	XO2-256ZE 13 n XO2-640ZE 14 n XO2-1200ZE 15 n XO2-2000ZE 17 n XO2-4000ZE 18 n XO2-7000ZE 20 n	mA
		LCMXO2-7000ZE	20	mA
I _{CCIO}	Bank Power Supply ⁶	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.

2. Assumes all inputs are held at $V_{\mbox{CCIO}}$ or GND and all outputs are tri-stated.

3. Typical user pattern.

4. JTAG programming is at 25 MHz.

5. TJ = 25 °C, power supplies at nominal voltage.

6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.



LVDS Emulation

MachXO2 devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.





Note: All resistors are ±1%.

Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Тур.	Units
Z _{OUT}	Output impedance	20	Ohms
R _S	Driver series resistor	158	Ohms
R _P	Driver parallel resistor	140	Ohms
R _T	Receiver termination	100	Ohms
V _{OH}	Output high voltage	1.43	V
V _{OL}	Output low voltage	1.07	V
V _{OD}	Output differential voltage	0.35	V
V _{CM}	Output common mode voltage	1.25	V
Z _{BACK}	Back impedance	100.5	Ohms
I _{DC}	DC output current	6.03	mA





			-6		-5		-4		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
		MachXO2-256HC-HE	1.42	_	1.59	_	1.96		ns
		MachXO2-640HC-HE	1.41	_	1.58	_	1.96	_	ns
^t su_del	Clock to Data Setup – PIO	MachXO2-1200HC-HE	1.63	_	1.79	_	2.17	_	ns
	Delav	MachXO2-2000HC-HE	1.61	_	1.76	_	2.13	_	ns
		MachXO2-4000HC-HE	1.66	_	1.81	_	2.19	_	ns
		MachXO2-7000HC-HE	1.53	_	1.67		2.03		ns
		MachXO2-256HC-HE	-0.24	_	-0.24		-0.24		ns
		MachXO2-640HC-HE	-0.23	_	-0.23	_	-0.23	_	ns
+	Clock to Data Hold – PIO Input	MachXO2-1200HC-HE	-0.24	_	-0.24	_	-0.24	_	ns
'H_DEL	Register with Input Data Delay	MachXO2-2000HC-HE	-0.23	_	-0.23		-0.23		ns
		MachXO2-4000HC-HE	-0.25	_	-0.25		-0.25		ns
		MachXO2-7000HC-HE	-0.21		-0.21		-0.21		ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices		388	_	323	_	269	MHz
General I/O	Pin Parameters (Using Edge C	lock without PLL)							
		MachXO2-1200HC-HE	_	7.53		7.76		8.10	ns
+	Clock to Output – PIO Output	MachXO2-2000HC-HE		7.53		7.76		8.10	ns
COE	Register	MachXO2-4000HC-HE		7.45		7.68		8.00	ns
		MachXO2-7000HC-HE		7.53		7.76		8.10	ns
	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	-0.19	_	-0.19	_	-0.19	_	ns
		MachXO2-2000HC-HE	-0.19	_	-0.19	_	-0.19	_	ns
t _{SUE}		MachXO2-4000HC-HE	-0.16	_	-0.16	_	-0.16	_	ns
		MachXO2-7000HC-HE	-0.19	_	-0.19		-0.19		ns
		MachXO2-1200HC-HE	1.97	_	2.24	_	2.52	_	ns
	Clock to Data Hold – PIO Input Register	MachXO2-2000HC-HE	1.97	_	2.24	_	2.52	_	ns
ΉE		MachXO2-4000HC-HE	1.89	_	2.16	_	2.43	_	ns
		MachXO2-7000HC-HE	1.97	_	2.24	_	2.52	_	ns
		MachXO2-1200HC-HE	1.56	_	1.69	_	2.05	_	ns
	Clock to Data Setup – PIO	MachXO2-2000HC-HE	1.56	_	1.69	_	2.05	_	ns
^I SU_DELE	Input Register with Data Input Delay	MachXO2-4000HC-HE	1.74	_	1.88	_	2.25	_	ns
		MachXO2-7000HC-HE	1.66	_	1.81	_	2.17		ns
		MachXO2-1200HC-HE	-0.23	_	-0.23	_	-0.23	_	ns
+	Clock to Data Hold – PIO Input	MachXO2-2000HC-HE	-0.23	_	-0.23		-0.23		ns
'H_DELE	Register with Input Data Delay	MachXO2-4000HC-HE	-0.34	_	-0.34		-0.34		ns
		MachXO2-7000HC-HE	-0.29	_	-0.29		-0.29		ns
General I/O	Pin Parameters (Using Primary	y Clock with PLL)							
		MachXO2-1200HC-HE	—	5.97		6.00		6.13	ns
	Clock to Output – PIO Output	MachXO2-2000HC-HE		5.98		6.01		6.14	ns
COPLL	Register	MachXO2-4000HC-HE		5.99		6.02		6.16	ns
		MachXO2-7000HC-HE		6.02		6.06		6.20	ns
		MachXO2-1200HC-HE	0.36	—	0.36	—	0.65	—	ns
+.	Clock to Data Setup – PIO	MachXO2-2000HC-HE	0.36	—	0.36	—	0.63	—	ns
SUPLL	Input Register	MachXO2-4000HC-HE	0.35	—	0.35	—	0.62	—	ns
		MachXO2-7000HC-HE	0.34	—	0.34	—	0.59	—	ns
	1	•			•		•		



			-6		_	-5		-4	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
		MachXO2-1200HC-HE	0.41		0.48		0.55	—	ns
1	Clock to Data Hold – PIO Input	MachXO2-2000HC-HE	0.42		0.49		0.56	—	ns
THPLL	Register	MachXO2-4000HC-HE	0.43		0.50		0.58	—	ns
		MachXO2-7000HC-HE	0.46		0.54		0.62	—	ns
		MachXO2-1200HC-HE	2.88		3.19		3.72	—	ns
	Clock to Data Setup – PIO	MachXO2-2000HC-HE	2.87	—	3.18	—	3.70	—	ns
^I SU_DELPLL	Delav	MachXO2-4000HC-HE	2.96		3.28		3.81	—	ns
	,	MachXO2-7000HC-HE	3.05		3.35	—	3.87	—	ns
		MachXO2-1200HC-HE	-0.83		-0.83		-0.83	—	ns
	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-2000HC-HE	-0.83		-0.83		-0.83	—	ns
^I H_DELPLL		MachXO2-4000HC-HE	-0.87		-0.87	—	-0.87	—	ns
		MachXO2-7000HC-HE	-0.91	—	-0.91	—	-0.91	—	ns
Generic DDF	RX1 Inputs with Clock and Data	Aligned at Pin Using PC	LK Pin	for Cloc	k Input -	GDDR	(1_RX.S	CLK.Ali	gned ^{9, 12}
t _{DVA}	Input Data Valid After CLK			0.317	—	0.344	—	0.368	UI
t _{DVE}	Input Data Hold After CLK	All MachXO2 devices,	0.742	—	0.702	—	0.668	—	UI
f _{DATA}	DDRX1 Input Data Speed	all sides	_	300	—	250	—	208	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency			150	—	125	—	104	MHz
Generic DDF	X1 Inputs with Clock and Data C	Centered at Pin Using PC	LK Pin f	or Clock	Input –	GDDRX	1_RX.SC	LK.Cen	tered ^{9, 12}
t _{SU}	Input Data Setup Before CLK		0.566		0.560		0.538	—	ns
t _{HO}	Input Data Hold After CLK	All MachXO2 devices,	0.778		0.879		1.090	—	ns
f _{DATA}	DDRX1 Input Data Speed	all sides		300		250		208	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency			150		125		104	MHz
Generic DDF	RX2 Inputs with Clock and Data	Aligned at Pin Using PC	LK Pin f	for Clock	k Input –	GDDR	(2_RX.E	CLK.Ali	gned ^{9, 12}
t _{DVA}	Input Data Valid After CLK		—	0.316		0.342		0.364	UI
t _{DVE}	Input Data Hold After CLK	MachXO2-640U,	0.710		0.675		0.679	—	UI
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	664	_	554	_	462	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency	bottom side only ¹¹		332		277		231	MHz
f _{SCLK}	SCLK Frequency			166		139	—	116	MHz
Generic DDF	X2 Inputs with Clock and Data C	Centered at Pin Using PC	LK Pin f	or Clock	Input –	GDDRX	2_RX.EC	LK.Cen	tered ^{9, 12}
t _{SU}	Input Data Setup Before CLK		0.233		0.219		0.198	—	ns
t _{HO}	Input Data Hold After CLK	MachXO2-640U	0.287	—	0.287	—	0.344	—	ns
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO2-1200/U and larger devices,	_	664	_	554	_	462	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency	bottom side only ¹¹	—	332	—	277	—	231	MHz
f _{SCLK}	SCLK Frequency	1	—	166		139		116	MHz



sysCONFIG Port Timing Specifications

Symbol	Pa	arameter	Min.	Max.	Units
All Configuration Mo	des		1		1
t _{PRGM}	PROGRAMN low p	oulse accept	55	—	ns
t _{PRGMJ}	PROGRAMN low p	oulse rejection	-	25	ns
t _{INITL}	INITN low time	LCMXO2-256	—	30	μs
		LCMXO2-640	—	35	μs
		LCMXO2-640U/ LCMXO2-1200	—	55	μs
		LCMXO2-1200U/ LCMXO2-2000	-	70	μs
		LCMXO2-2000U/ LCMXO2-4000	_	105	μs
		LCMXO2-7000	—	130	μs
t _{DPPINIT}	PROGRAMN low t	o INITN low	—	150	ns
t _{DPPDONE}	PROGRAMN low t	o DONE low	—	150	ns
t _{IODISS}	PROGRAMN low t	o I/O disable	—	120	ns
Slave SPI					•
f _{MAX}	CCLK clock freque	CCLK clock frequency		66	MHz
t _{CCLKH}	CCLK clock pulse	width high	7.5	—	ns
t _{CCLKL}	CCLK clock pulse	width low	7.5	—	ns
t _{STSU}	CCLK setup time		2	—	ns
t _{STH}	CCLK hold time		0	—	ns
t _{STCO}	CCLK falling edge	to valid output	—	10	ns
t _{STOZ}	CCLK falling edge	to valid disable	—	10	ns
t _{STOV}	CCLK falling edge	to valid enable	—	10	ns
t _{SCS}	Chip select high tir	ne	25	—	ns
t _{SCSS}	Chip select setup t	ime	3	—	ns
t _{SCSH}	Chip select hold tir	ne	3	—	ns
Master SPI					
f _{MAX}	MCLK clock freque	ency	—	133	MHz
t _{MCLKH}	MCLK clock pulse	width high	3.75	—	ns
t _{MCLKL}	MCLK clock pulse	width low	3.75	—	ns
t _{STSU}	MCLK setup time		5	—	ns
t _{STH}	MCLK hold time		1	—	ns
t _{CSSPI}	INITN high to chip	select low	100	200	ns
t _{MCLK}	INITN high to first I	MCLK edge	0.75	1	μs



MachXO2 Family Data Sheet Pinout Information

March 2017

Data Sheet DS1035

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
		[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).
		[Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.
		[A/B/C/D] indicates the PIO within the group to which the pad is connected.
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic.
		During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.
NC	—	No connect.
GND	_	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together. For QFN 48 package, the exposed die pad is the device ground.
VCC	_	V_{CC} – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIOx	_	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.
PLL and Clock Functi	ons (Us	ed as user-programmable I/O pins when not used for PLL or clock pins)
[LOC]_GPLL[T, C]_IN	_	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]		Primary Clock pads. One to three clock pads per side.
Test and Programming	g (Dual t	function pins used for test access port and during sysCONFIG™)
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
ТСК	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	0	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
		Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then:
JTAGENB	I	If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O.
		If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.
		For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.
Configuration (Dual fu	nction p	ins used during sysCONFIG)
PROGRAMN	I	Initiates configuration sequence when asserted low. During configuration, or when reserved as PROGRAMN in user mode, this pin always has an active pull-up.

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Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, or when reserved as INITn in user mode, this pin has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress. During configuration, or when reserved as DONE in user mode, this pin has an active pull-up.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.
SCL	I/O	Slave I ² C clock input and master I ² C clock output.
SDA	I/O	Slave I ² C data input and master I ² C data output.



Ordering Information

MachXO2 devices have top-side markings, for commercial and industrial grades, as shown below:



Notes:

- 1. Markings are abbreviated for small packages.
- 2. See PCN 05A-12 for information regarding a change to the top-side mark logo.



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32C	1280	2.5 V / 3.3 V	-4	Halogen-Free QFN	32	COM
LCMXO2-1200HC-5SG32C	1280	2.5 V / 3.3 V	-5	Halogen-Free QFN	32	COM
LCMXO2-1200HC-6SG32C	1280	2.5 V / 3.3 V	-6	Halogen-Free QFN	32	COM
LCMXO2-1200HC-4TG100C	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100C	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100C	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132C	1280	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132C	1280	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132C	1280	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144C	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144C	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144C	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256C	1280	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-1200UHC-5FTG256C	1280	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-1200UHC-6FTG256C	1280	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100C	2112	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-5TG100C	2112	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-6TG100C	2112	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-4MG132C	2112	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-5MG132C	2112	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-6MG132C	2112	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-4TG144C	2112	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-5TG144C	2112	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-6TG144C	2112	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-4BG256C	2112	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-5BG256C	2112	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-6BG256C	2112	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-4FTG256C	2112	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HC-5FTG256C	2112	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HC-6FTG256C	2112	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	COM



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144C	6864	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	СОМ
LCMXO2-7000HC-5TG144C	6864	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-6TG144C	6864	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-4BG256C	6864	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-5BG256C	6864	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-6BG256C	6864	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-4FTG256C	6864	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-5FTG256C	6864	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-6FTG256C	6864	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-4BG332C	6864	2.5 V / 3.3 V	-4	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-5BG332C	6864	2.5 V / 3.3 V	-5	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-6BG332C	6864	2.5 V / 3.3 V	-6	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-4FG400C	6864	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-5FG400C	6864	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-6FG400C	6864	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-4FG484C	6864	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-5FG484C	6864	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-6FG484C	6864	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100CR1 ¹	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100CR1 ¹	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100CR1 ¹	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132CR11	1280	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132CR11	1280	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132CR11	1280	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144CR1 ¹	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144CR1 ¹	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144CR11	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	COM

1. Specifications for the "LCMXO2-1200HC-speed package CR1" are the same as the "LCMXO2-1200HC-speed package C" devices respectively, except as specified in the R1 Device Specifications section of this data sheet.



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84I	4320	2.5 V / 3.3 V	-4	Halogen-Free QFN	84	IND
LCMXO2-4000HC-5QN84I	4320	2.5 V / 3.3 V	-5	Halogen-Free QFN	84	IND
LCMXO2-4000HC-6QN84I	4320	2.5 V / 3.3 V	-6	Halogen-Free QFN	84	IND
LCMXO2-4000HC-4TG144I	4320	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-5TG144I	4320	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-6TG144I	4320	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-4MG132I	4320	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-5MG132I	4320	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-6MG132I	4320	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-4BG256I	4320	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-5BG256I	4320	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-6BG256I	4320	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-4FTG256I	4320	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-5FTG256I	4320	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-6FTG256I	4320	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-4BG332I	4320	2.5 V / 3.3 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-5BG332I	4320	2.5 V / 3.3 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-6BG332I	4320	2.5 V / 3.3 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-4FG484I	4320	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-5FG484I	4320	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-6FG484I	4320	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144I	6864	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-5TG144I	6864	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-6TG144I	6864	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-4BG256I	6864	2.5 V / 3.3 V	-4	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-5BG256I	6864	2.5 V / 3.3 V	-5	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-6BG256I	6864	2.5 V / 3.3 V	-6	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-4FTG256I	6864	2.5 V / 3.3 V	-4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-5FTG256I	6864	2.5 V / 3.3 V	-5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-6FTG256I	6864	2.5 V / 3.3 V	-6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-4BG332I	6864	2.5 V / 3.3 V	-4	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-5BG332I	6864	2.5 V / 3.3 V	-5	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-6BG332I	6864	2.5 V / 3.3 V	-6	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-4FG400I	6864	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-5FG400I	6864	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-6FG400I	6864	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-4FG484I	6864	2.5 V / 3.3 V	-4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-5FG484I	6864	2.5 V / 3.3 V	-5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-6FG484I	6864	2.5 V / 3.3 V	-6	Halogen-Free fpBGA	484	IND



R1 Device Specifications

The LCMXO2-1200ZE/HC "R1" devices have the same specifications as their Standard (non-R1) counterparts except as listed below. For more details on the R1 to Standard migration refer to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard Non-R1) Devices.

- The User Flash Memory (UFM) cannot be programmed through the internal WISHBONE interface. It can still be programmed through the JTAG/SPI/I²C ports.
- The on-chip differential input termination resistor value is higher than intended. It is approximately 200Ω as opposed to the intended 100Ω. It is recommended to use external termination resistors for differential inputs. The on-chip termination resistors can be disabled through Lattice design software.
- Soft Error Detection logic may not produce the correct result when it is run for the first time after configuration. To use this feature, discard the result from the first operation. Subsequent operations will produce the correct result.
- Under certain conditions, IIH exceeds data sheet specifications. The following table provides more details:

Condition	Clamp	Pad Rising IIH Max.	Pad Falling IIH Min.	Steady State Pad High IIH	Steady State Pad Low IIL
VPAD > VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD = VCCIO	ON	10 µA	–10 μA	10 µA	10 µA
VPAD = VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD < VCCIO	OFF	10 µA	–10 μA	10 µA	10 µA

- The user SPI interface does not operate correctly in some situations. During master read access and slave write access, the last byte received does not generate the RRDY interrupt.
- In GDDRX2, GDDRX4 and GDDR71 modes, ECLKSYNC may have a glitch in the output under certain conditions, leading to possible loss of synchronization.
- When using the hard I²C IP core, the I²C status registers I2C_1_SR and I2C_2_SR may not update correctly.
- PLL Lock signal will glitch high when coming out of standby. This glitch lasts for about 10 μsec before returning low.
- Dual boot only available on HC devices, requires tying VCC and VCCIO2 to the same 3.3 V or 2.5 V supply.



MachXO2 Family Data Sheet Revision History

March 2017

Data Sheet DS1035

Date	Version	Section	Change Summary
March 2017	3.3	DC and Switching Characteristics	Updated the Absolute Maximum Ratings section. Added standards.
			Updated the sysIO Recommended Operating Conditions section. Added standards.
			Updated the sysIO Single-Ended DC Electrical Characteristics sec- tion. Added standards.
			Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA} . The parameter descriptions were also modified.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA} . The parameter descriptions were also modified.
			Updated the sysCONFIG Port Timing Specifications section. Corrected the t_{INITL} units from ns to μ s.
		Pinout Information	Updated the Signal Descriptions section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals.
			Updated the Pinout Information Summary section. Added footnote to MachXO2-1200 32 QFN.
		Ordering Information	Updated the MachXO2 Part Number Description section. Corrected the MG184, BG256, FTG256 package information. Added "(0.8 mm Pitch)" to BG332.
			Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. — Updated LCMXO2-1200ZE-1UWG25ITR50 footnote. — Corrected footnote numbering typo. — Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2- 2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s.

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Date	Version	Section	Change Summary
December 2014	2.9	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Removed XO2-4000U data. — Removed 400-ball ftBGA. — Removed 25-ball WLCSP value for XO2-2000U.
		DC and Switching Characteristics	Updated the Recommended Operating Conditions section. Adjusted Max. values for V_{CC} and V_{CCIO}
			Updated the sysIO Recommended Operating Conditions section. Adjusted Max. values for LVCMOS 3.3, LVTTL, PCI, LVDS33 and LVPECL.
		Pinout Information	Updated the Pinout Information Summary section. Removed MachXO2-4000U.
		Ordering Information	Updated the MachXO2 Part Number Description section. Removed BG400 package.
			Updated the High-Performance Commercial Grade Devices with Volt- age Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
			Updated the High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
November 2014	2.8	Introduction	Updated the Features section. — Revised I/Os under Flexible Logic Architecture. — Revised standby power under Ultra Low Power Devices. — Revise input frequency range under Flexible On-Chip Clocking.
			Updated Table 1-1, MachXO2 Family Selection Guide. — Added XO2-4000U data. — Removed HE and ZE device options for XO2-4000. — Added 400-ball ftBGA.
		Pinout Information	Updated the Pinout Information Summary section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added BG400 package.
			Updated the Ordering Information section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400 part numbers.
October 2014	2.7	Ordering Information	Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Fixed typo in LCMXO2-2000ZE- 1UWG49ITR part number package.
		Architecture	Updated the Supported Standards section. Added MIPI information to Table 2-12. Supported Input Standards and Table 2-13. Supported Output Standards.
		DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition.
			Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition.
			Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.
July 2014	2.6	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics ^{1, 2} section. Updated footnote 4.
			Updated Register-to-Register Performance section. Updated foot- note.
		Ordering Information	Updated UW49 package to UWG49 in MachXO2 Part Number Description.
			Updated LCMXO2-2000ZE-1UWG49CTR package in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging.