# Lattice Semiconductor Corporation - LCMXO2-7000ZE-3BG256C Datasheet


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

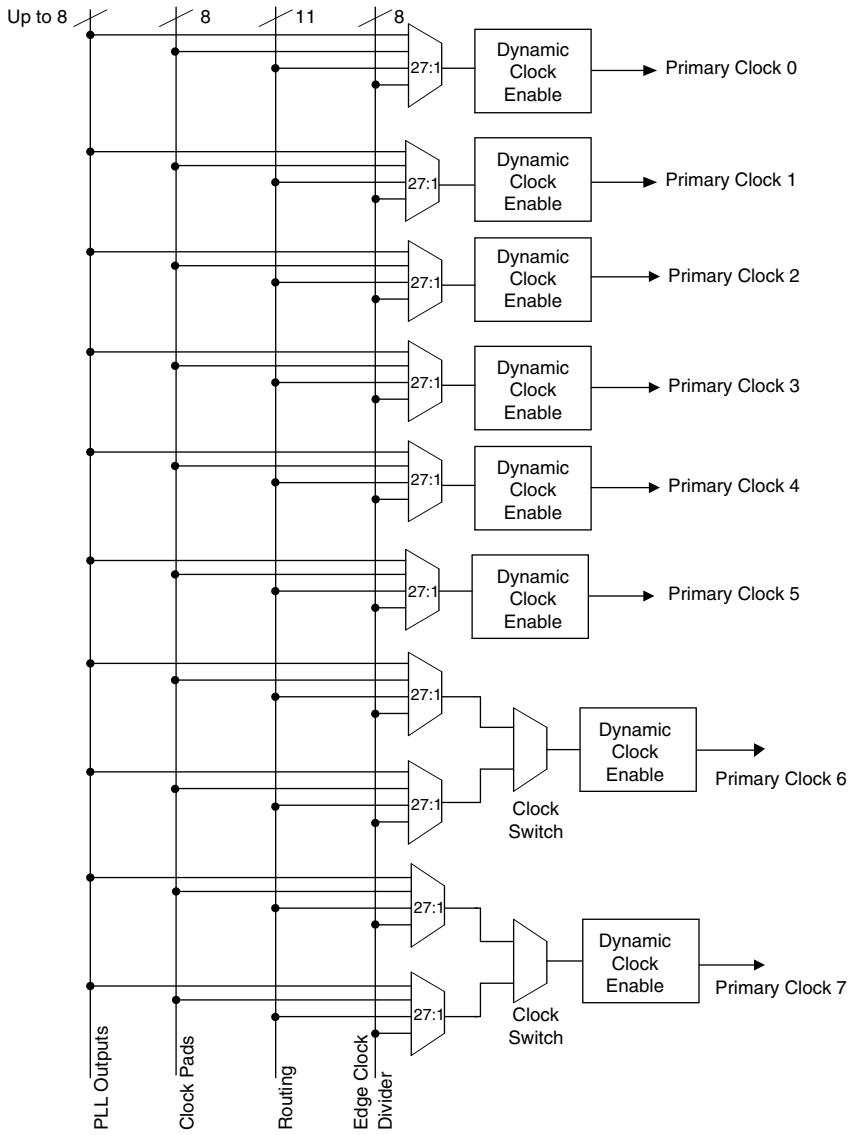
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 858 |
| Number of Logic Elements/Cells | 6864 |
| Total RAM Bits | 245760 |
| Number of I/O | 206 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 256-LFBGA |
| Supplier Device Package | 256-CABGA (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-7000ze-3bg256c |

*Figure 2-5. Primary Clocks for MachXO2 Devices*




Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO2 External Switching Characteristics table.

*Table 2-4. PLL Signal Descriptions (Continued)*

| Port Name | I/O | Description |
|---|---|---|
| CLKOP | O | Primary PLL output clock (with phase shift adjustment) |
| CLKOS | O | Secondary PLL output clock (with phase shift adjust) |
| CLKOS2 | O | Secondary PLL output clock2 (with phase shift adjust) |
| CLKOS3 | O | Secondary PLL output clock3 (with phase shift adjust) |
| LOCK | O | PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feedback signals. |
| DPHSRC | O | Dynamic Phase source – ports or WISHBONE is active |
| STDBY | I | Standby signal to power down the PLL |
| RST | I | PLL reset without resetting the M-divider. Active high reset. |
| RESETM | I | PLL reset - includes resetting the M-divider. Active high reset. |
| RESETC | I | Reset for CLKOS2 output divider only. Active high reset. |
| RESETD | I | Reset for CLKOS3 output divider only. Active high reset. |
| ENCLKOP | I | Enable PLL output CLKOP |
| ENCLKOS | I | Enable PLL output CLKOS when port is active |
| ENCLKOS2 | I | Enable PLL output CLKOS2 when port is active |
| ENCLKOS3 | I | Enable PLL output CLKOS3 when port is active |
| PLLCLK | I | PLL data bus clock input signal |
| PLLRST | I | PLL data bus reset. This resets only the data bus not any register values. |
| PLLSTB | I | PLL data bus strobe signal |
| PLLWE | I | PLL data bus write enable signal |
| PLLADDR [4:0] | I | PLL data bus address |
| PLLDATI [7:0] | I | PLL data bus data input |
| PLLDATO [7:0] | O | PLL data bus data output |
| PLLACK | O | PLL data bus acknowledge signal |

## sysMEM Embedded Block RAM Memory

The MachXO2-640/U and larger devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

### sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.

## DDR Memory Support

Certain PICs on the right edge of MachXO2-640U, MachXO2-1200/U and larger devices, have additional circuitry to allow the implementation of DDR memory interfaces. There are two groups of 14 or 12 PIOs each on the right edge with additional circuitry to implement DDR memory interfaces. This capability allows the implementation of up to 16-bit wide memory interfaces. One PIO from each group contains a control element, the DQS Read/Write Block, to facilitate the generation of clock and control signals (DQSR90, DQSW90, DDRCLKPOL and DATAVALID). These clock and control signals are distributed to the other PIO in the group through dedicated low skew routing.

## DQS Read Write Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Read Write block provides the required clock alignment for DDR memory interfaces. DQSR90 and DQSW90 signals are generated by the DQS Read Write block from the DQS input.

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the read cycle) is unknown. The MachXO2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This circuit changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each read cycle for the correct clock polarity. Prior to the read operation in DDR memories, DQS is in tri-state (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit in the DQS Read Write block detects the first DQS rising edge after the preamble state and generates the DDRCLKPOL signal. This signal is used to control the polarity of the clock to the synchronizing registers.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration signals (6-bit bus) from a DLL on the right edge of the device. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, PCI, SSTL, HSTL, LVDS, BLVDS, MLVDS and LVPECL.

Each bank is capable of supporting multiple I/O standards. In the MachXO2 devices, single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS and PCI), differential (LVDS) and referenced input buffers (SSTL and HSTL) are powered using I/O supply voltage ($V_{CCIO}$). Each sysIO bank has its own $V_{CCIO}$. In addition, each bank has a voltage reference, $V_{REF}$, which allows the use of referenced input buffers independent of the bank $V_{CCIO}$.

MachXO2-256 and MachXO2-640 devices contain single-ended ratioed input buffers and single-ended output buffers with complementary outputs on all the I/O banks. Note that the single-ended input buffers on these devices do not contain PCI clamps. In addition to the single-ended I/O buffers these two devices also have differential and referenced input buffers on all I/Os. The I/Os are arranged in pairs, the two pads in the pair are described as "T" and "C", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 devices contain three types of sysIO buffer pairs.

1. **Left and Right sysIO Buffer Pairs**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential and referenced input buffers.

2. **Bottom sysIO Buffer Pairs**
   The sysIO buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential and referenced input buffers. Only the I/Os on the bottom banks have programmable PCI clamps and differential input termination. The PCI clamp is enabled after $V_{CC}$ and $V_{CCIO}$ are at valid operating levels and the device has been configured.

3. **Top sysIO Buffer Pairs**
   The sysIO buffer pairs in the top bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential and referenced I/O buffers. Half of the sysIO buffer pairs on the top edge have true differential outputs. The sysIO buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver. The referenced input buffer can also be configured as a differential input buffer.

## Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when $V_{CC}$ and $V_{CCIO0}$ have reached $V_{PORUP}$ level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-down to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to $V_{CCIO}$ as the default functionality). The I/O pins will maintain the blank configuration until $V_{CC}$ and $V_{CCIO}$ (for I/O banks containing configuration I/Os) have reached $V_{PORUP}$ levels at which time the I/Os will take on the user-configured settings only after a proper download/configuration.

## Supported Standards

The MachXO2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL, and PCI. The buffer supports the LVTTL, PCI, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO2-640U, MachXO2-1200/U and higher devices support on-chip LVDS output buffers on approximately 50% of the I/Os on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO2 devices. PCI support is provided in the bottom bank of theMachXO2-640U, MachXO2-1200/U and higher density devices. Table 2-11 summarizes the I/O characteristics of the MachXO2 PLDs.

Tables 2-11 and 2-12 show the I/O standards (together with their supply and reference voltages) supported by the MachXO2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1202, MachXO2 sysIO Usage Guide.

## Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  — Watchdog timer
  — Clear timer on compare match
  — Fast PWM
  — Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

***Figure 2-23. Timer/Counter Block Diagram***

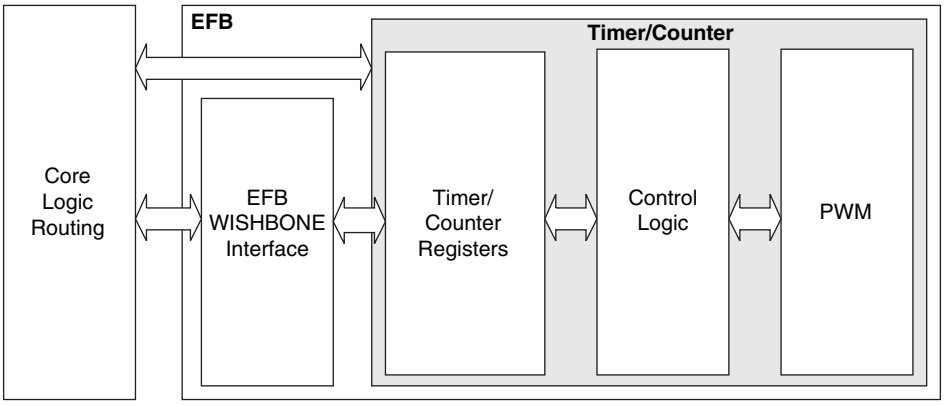



***Table 2-17. Timer/Counter Signal Description***

| Port | I/O | Description |
|---|---|---|
| tc_clki | I | Timer/Counter input clock signal |
| tc_rstn | I | Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled |
| tc_ic | I | Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping. |
| tc_int | O | Without WISHBONE – Can be used as overflow flag<br>With WISHBONE – Controlled by three IRQ registers |
| tc_oc | O | Timer counter output signal |

For more details on these embedded functions, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

## User Flash Memory (UFM)

MachXO2-640/U and higher density devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, $I^2C$ and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices.

## Standby Mode and Power Saving Options

MachXO2 devices are available in three options for maximum flexibility: ZE, HC and HE devices. The ZE devices have ultra low static and dynamic power consumption. These devices use a 1.2 V core voltage that further reduces power consumption. The HC and HE devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V $V_{CC}$ and 3.3 V $V_{CC}$ while the HE devices operate at 1.2 V $V_{CC}$.

MachXO2 devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO2 devices support an ultra low power Stand-by mode. While most of these features are available in all three device types, these features are mainly intended for use with MachXO2 ZE devices to manage power consumption.

In the stand-by mode the MachXO2 devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate $I^2C$ or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO2 devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

When implementing background programming of the on-chip Flash, care must be taken for the operation of the PLL. For devices that have two PLLs (XO2-2000U, -4000 and -7000), the system must put the RPLL (Right-side PLL) in reset state during the background Flash programming. More detailed description can be found in TN1204, MachXO2 Programming and Configuration Usage Guide.

**Security and One-Time Programmable Mode (OTP)**
For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO2 devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile Flash memory spaces. The device can be in one of two modes:

1. Unlocked – Readback of the SRAM configuration and non-volatile Flash memory spaces is allowed.

2. Permanently Locked – The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

**Dual Boot**
MachXO2 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the on-chip Flash. The golden image MUST reside in an external SPI Flash. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

**Soft Error Detection**
The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1206, MachXO2 Soft Error Detection Usage Guide.

## TraceID

Each MachXO2 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, $I^2C$, or JTAG interfaces.

## Density Shifting

The MachXO2 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO2 migration files.

## BLVDS

The MachXO2 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

***Figure 3-2. BLVDS Multi-point Output Example***

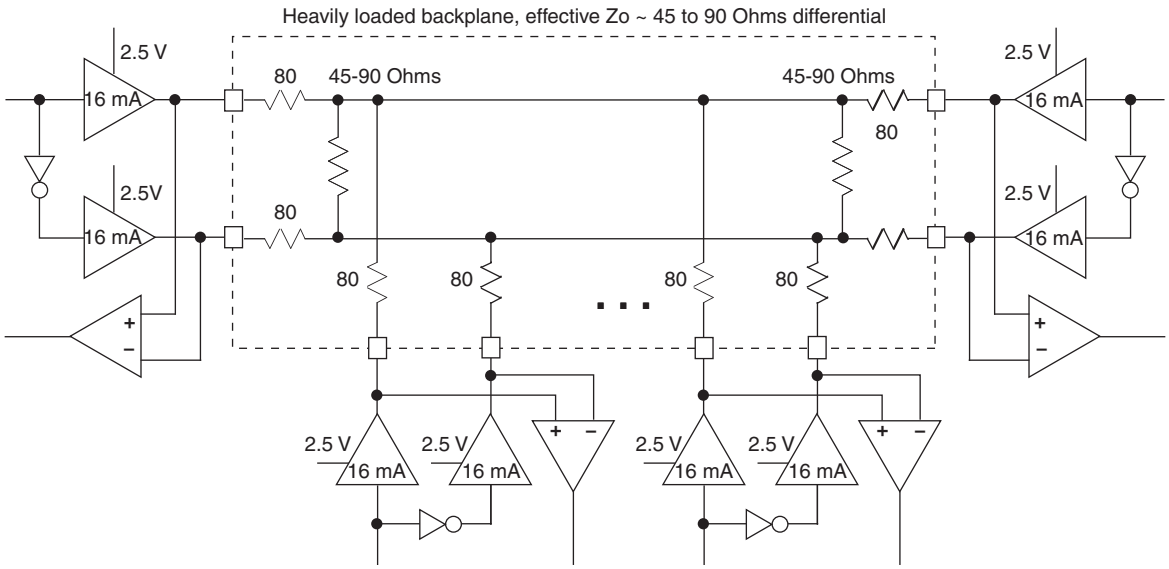



***Table 3-2. BLVDS DC Conditions[1]***

**Over Recommended Operating Conditions**

| Symbol | Description | Nominal | | Units |
|---|---|---|---|---|
| | | Zo = 45 | Zo = 90 | |
| $Z_{OUT}$ | Output impedance | 20 | 20 | Ohms |
| $R_S$ | Driver series resistance | 80 | 80 | Ohms |
| $R_{TLEFT}$ | Left end termination | 45 | 90 | Ohms |
| $R_{TRIGHT}$ | Right end termination | 45 | 90 | Ohms |
| $V_{OH}$ | Output high voltage | 1.376 | 1.480 | V |
| $V_{OL}$ | Output low voltage | 1.124 | 1.020 | V |
| $V_{OD}$ | Output differential voltage | 0.253 | 0.459 | V |
| $V_{CM}$ | Output common mode voltage | 1.250 | 1.250 | V |
| $I_{DC}$ | DC output current | 11.236 | 10.204 | mA |

1. For input buffer, see LVDS table.

| Parameter | Description | Device | –6 | | –5 | | –4 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{SU\_DEL}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-256HC-HE | 1.42 | — | 1.59 | — | 1.96 | — | ns |
| | | MachXO2-640HC-HE | 1.41 | — | 1.58 | — | 1.96 | — | ns |
| | | MachXO2-1200HC-HE | 1.63 | — | 1.79 | — | 2.17 | — | ns |
| | | MachXO2-2000HC-HE | 1.61 | — | 1.76 | — | 2.13 | — | ns |
| | | MachXO2-4000HC-HE | 1.66 | — | 1.81 | — | 2.19 | — | ns |
| | | MachXO2-7000HC-HE | 1.53 | — | 1.67 | — | 2.03 | — | ns |
| $t_{H\_DEL}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-256HC-HE | –0.24 | — | –0.24 | — | –0.24 | — | ns |
| | | MachXO2-640HC-HE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-1200HC-HE | –0.24 | — | –0.24 | — | –0.24 | — | ns |
| | | MachXO2-2000HC-HE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-4000HC-HE | –0.25 | — | –0.25 | — | –0.25 | — | ns |
| | | MachXO2-7000HC-HE | –0.21 | — | –0.21 | — | –0.21 | — | ns |
| $f_{MAX\_IO}$ | Clock Frequency of I/O and PFU Register | All MachXO2 devices | — | 388 | — | 323 | — | 269 | MHz |
| **General I/O Pin Parameters (Using Edge Clock without PLL)** | | | | | | | | | |
| $t_{COE}$ | Clock to Output – PIO Output Register | MachXO2-1200HC-HE | — | 7.53 | — | 7.76 | — | 8.10 | ns |
| | | MachXO2-2000HC-HE | — | 7.53 | — | 7.76 | — | 8.10 | ns |
| | | MachXO2-4000HC-HE | — | 7.45 | — | 7.68 | — | 8.00 | ns |
| | | MachXO2-7000HC-HE | — | 7.53 | — | 7.76 | — | 8.10 | ns |
| $t_{SUE}$ | Clock to Data Setup – PIO Input Register | MachXO2-1200HC-HE | –0.19 | — | –0.19 | — | –0.19 | — | ns |
| | | MachXO2-2000HC-HE | –0.19 | — | –0.19 | — | –0.19 | — | ns |
| | | MachXO2-4000HC-HE | –0.16 | — | –0.16 | — | –0.16 | — | ns |
| | | MachXO2-7000HC-HE | –0.19 | — | –0.19 | — | –0.19 | — | ns |
| $t_{HE}$ | Clock to Data Hold – PIO Input Register | MachXO2-1200HC-HE | 1.97 | — | 2.24 | — | 2.52 | — | ns |
| | | MachXO2-2000HC-HE | 1.97 | — | 2.24 | — | 2.52 | — | ns |
| | | MachXO2-4000HC-HE | 1.89 | — | 2.16 | — | 2.43 | — | ns |
| | | MachXO2-7000HC-HE | 1.97 | — | 2.24 | — | 2.52 | — | ns |
| $t_{SU\_DELE}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-1200HC-HE | 1.56 | — | 1.69 | — | 2.05 | — | ns |
| | | MachXO2-2000HC-HE | 1.56 | — | 1.69 | — | 2.05 | — | ns |
| | | MachXO2-4000HC-HE | 1.74 | — | 1.88 | — | 2.25 | — | ns |
| | | MachXO2-7000HC-HE | 1.66 | — | 1.81 | — | 2.17 | — | ns |
| $t_{H\_DELE}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-1200HC-HE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-2000HC-HE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-4000HC-HE | –0.34 | — | –0.34 | — | –0.34 | — | ns |
| | | MachXO2-7000HC-HE | –0.29 | — | –0.29 | — | –0.29 | — | ns |
| **General I/O Pin Parameters (Using Primary Clock with PLL)** | | | | | | | | | |
| $t_{COPLL}$ | Clock to Output – PIO Output Register | MachXO2-1200HC-HE | — | 5.97 | — | 6.00 | — | 6.13 | ns |
| | | MachXO2-2000HC-HE | — | 5.98 | — | 6.01 | — | 6.14 | ns |
| | | MachXO2-4000HC-HE | — | 5.99 | — | 6.02 | — | 6.16 | ns |
| | | MachXO2-7000HC-HE | — | 6.02 | — | 6.06 | — | 6.20 | ns |
| $t_{SUPLL}$ | Clock to Data Setup – PIO Input Register | MachXO2-1200HC-HE | 0.36 | — | 0.36 | — | 0.65 | — | ns |
| | | MachXO2-2000HC-HE | 0.36 | — | 0.36 | — | 0.63 | — | ns |
| | | MachXO2-4000HC-HE | 0.35 | — | 0.35 | — | 0.62 | — | ns |
| | | MachXO2-7000HC-HE | 0.34 | — | 0.34 | — | 0.59 | — | ns |

| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{SU\_DEL}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-256ZE | 2.62 | — | 2.91 | — | 3.14 | — | ns |
| | | MachXO2-640ZE | 2.56 | — | 2.85 | — | 3.08 | — | ns |
| | | MachXO2-1200ZE | 2.30 | — | 2.57 | — | 2.79 | — | ns |
| | | MachXO2-2000ZE | 2.25 | — | 2.50 | — | 2.70 | — | ns |
| | | MachXO2-4000ZE | 2.39 | — | 2.60 | — | 2.76 | — | ns |
| | | MachXO2-7000ZE | 2.17 | — | 2.33 | — | 2.43 | — | ns |
| $t_{H\_DEL}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-256ZE | –0.44 | — | –0.44 | — | –0.44 | — | ns |
| | | MachXO2-640ZE | –0.43 | — | –0.43 | — | –0.43 | — | ns |
| | | MachXO2-1200ZE | –0.28 | — | –0.28 | — | –0.28 | — | ns |
| | | MachXO2-2000ZE | –0.31 | — | –0.31 | — | –0.31 | — | ns |
| | | MachXO2-4000ZE | –0.34 | — | –0.34 | — | –0.34 | — | ns |
| | | MachXO2-7000ZE | –0.21 | — | –0.21 | — | –0.21 | — | ns |
| $f_{MAX\_IO}$ | Clock Frequency of I/O and PFU Register | All MachXO2 devices | — | 150 | — | 125 | — | 104 | MHz |
| **General I/O Pin Parameters (Using Edge Clock without PLL)** | | | | | | | | | |
| $t_{COE}$ | Clock to Output – PIO Output Register | MachXO2-1200ZE | — | 11.10 | — | 11.51 | — | 11.91 | ns |
| | | MachXO2-2000ZE | — | 11.10 | — | 11.51 | — | 11.91 | ns |
| | | MachXO2-4000ZE | — | 10.89 | — | 11.28 | — | 11.67 | ns |
| | | MachXO2-7000ZE | — | 11.10 | — | 11.51 | — | 11.91 | ns |
| $t_{SUE}$ | Clock to Data Setup – PIO Input Register | MachXO2-1200ZE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-2000ZE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-4000ZE | –0.15 | — | –0.15 | — | –0.15 | — | ns |
| | | MachXO2-7000ZE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| $t_{HE}$ | Clock to Data Hold – PIO Input Register | MachXO2-1200ZE | 3.81 | — | 4.11 | — | 4.52 | — | ns |
| | | MachXO2-2000ZE | 3.81 | — | 4.11 | — | 4.52 | — | ns |
| | | MachXO2-4000ZE | 3.60 | — | 3.89 | — | 4.28 | — | ns |
| | | MachXO2-7000ZE | 3.81 | — | 4.11 | — | 4.52 | — | ns |
| $t_{SU\_DELE}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-1200ZE | 2.78 | — | 3.11 | — | 3.40 | — | ns |
| | | MachXO2-2000ZE | 2.78 | — | 3.11 | — | 3.40 | — | ns |
| | | MachXO2-4000ZE | 3.11 | — | 3.48 | — | 3.79 | — | ns |
| | | MachXO2-7000ZE | 2.94 | — | 3.30 | — | 3.60 | — | ns |
| $t_{H\_DELE}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-1200ZE | –0.29 | — | -0.29 | — | –0.29 | — | ns |
| | | MachXO2-2000ZE | –0.29 | — | -0.29 | — | –0.29 | — | ns |
| | | MachXO2-4000ZE | –0.46 | — | -0.46 | — | –0.46 | — | ns |
| | | MachXO2-7000ZE | –0.37 | — | -0.37 | — | –0.37 | — | ns |
| **General I/O Pin Parameters (Using Primary Clock with PLL)** | | | | | | | | | |
| $t_{COPLL}$ | Clock to Output – PIO Output Register | MachXO2-1200ZE | — | 7.95 | — | 8.07 | — | 8.19 | ns |
| | | MachXO2-2000ZE | — | 7.97 | — | 8.10 | — | 8.22 | ns |
| | | MachXO2-4000ZE | — | 7.98 | — | 8.10 | — | 8.23 | ns |
| | | MachXO2-7000ZE | — | 8.02 | — | 8.14 | — | 8.26 | ns |
| $t_{SUPLL}$ | Clock to Data Setup – PIO Input Register | MachXO2-1200ZE | 0.85 | — | 0.85 | — | 0.89 | — | ns |
| | | MachXO2-2000ZE | 0.84 | — | 0.84 | — | 0.86 | — | ns |
| | | MachXO2-4000ZE | 0.84 | — | 0.84 | — | 0.85 | — | ns |
| | | MachXO2-7000ZE | 0.83 | — | 0.83 | — | 0.81 | — | ns |

| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{HPLL}$ | Clock to Data Hold – PIO Input Register | MachXO2-1200ZE | 0.66 | — | 0.68 | — | 0.80 | — | ns |
| | | MachXO2-2000ZE | 0.68 | — | 0.70 | — | 0.83 | — | ns |
| | | MachXO2-4000ZE | 0.68 | — | 0.71 | — | 0.84 | — | ns |
| | | MachXO2-7000ZE | 0.73 | — | 0.74 | — | 0.87 | — | ns |
| $t_{SU\_DELPLL}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-1200ZE | 5.14 | — | 5.69 | — | 6.20 | — | ns |
| | | MachXO2-2000ZE | 5.11 | — | 5.67 | — | 6.17 | — | ns |
| | | MachXO2-4000ZE | 5.27 | — | 5.84 | — | 6.35 | — | ns |
| | | MachXO2-7000ZE | 5.15 | — | 5.71 | — | 6.23 | — | ns |
| $t_{H\_DELPLL}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-1200ZE | –1.36 | — | –1.36 | — | –1.36 | — | ns |
| | | MachXO2-2000ZE | –1.35 | — | –1.35 | — | –1.35 | — | ns |
| | | MachXO2-4000ZE | –1.43 | — | –1.43 | — | –1.43 | — | ns |
| | | MachXO2-7000ZE | –1.41 | — | –1.41 | — | –1.41 | — | ns |
| **Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 12]** | | | | | | | | | |
| $t_{DVA}$ | Input Data Valid After CLK | All MachXO2 devices, all sides | — | 0.382 | — | 0.401 | — | 0.417 | UI |
| $t_{DVE}$ | Input Data Hold After CLK | | 0.670 | — | 0.684 | — | 0.693 | — | UI |
| $f_{DATA}$ | DDRX1 Input Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{DDRX1}$ | DDRX1 SCLK Frequency | | — | 70 | — | 58 | — | 49 | MHz |
| **Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 12]** | | | | | | | | | |
| $t_{SU}$ | Input Data Setup Before CLK | All MachXO2 devices, all sides | 1.319 | — | 1.412 | — | 1.462 | — | ns |
| $t_{HO}$ | Input Data Hold After CLK | | 0.717 | — | 1.010 | — | 1.340 | — | ns |
| $f_{DATA}$ | DDRX1 Input Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{DDRX1}$ | DDRX1 SCLK Frequency | | — | 70 | — | 58 | — | 49 | MHz |
| **Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 12]** | | | | | | | | | |
| $t_{DVA}$ | Input Data Valid After CLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11] | — | 0.361 | — | 0.346 | — | 0.334 | UI |
| $t_{DVE}$ | Input Data Hold After CLK | | 0.602 | — | 0.625 | — | 0.648 | — | UI |
| $f_{DATA}$ | DDRX2 Serial Input Data Speed | | — | 280 | — | 234 | — | 194 | Mbps |
| $f_{DDRX2}$ | DDRX2 ECLK Frequency | | — | 140 | — | 117 | — | 97 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 59 | — | 49 | MHz |
| **Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 12]** | | | | | | | | | |
| $t_{SU}$ | Input Data Setup Before CLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11] | 0.472 | — | 0.672 | — | 0.865 | — | ns |
| $t_{HO}$ | Input Data Hold After CLK | | 0.363 | — | 0.501 | — | 0.743 | — | ns |
| $f_{DATA}$ | DDRX2 Serial Input Data Speed | | — | 280 | — | 234 | — | 194 | Mbps |
| $f_{DDRX2}$ | DDRX2 ECLK Frequency | | — | 140 | — | 117 | — | 97 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 59 | — | 49 | MHz |
| **Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input - GDDRX4_RX.ECLK.Aligned[9, 12]** | | | | | | | | | |
| $t_{DVA}$ | Input Data Valid After ECLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only[11] | — | 0.307 | — | 0.316 | — | 0.326 | UI |
| $t_{DVE}$ | Input Data Hold After ECLK | | 0.662 | — | 0.650 | — | 0.649 | — | UI |
| $f_{DATA}$ | DDRX4 Serial Input Data Speed | | — | 420 | — | 352 | — | 292 | Mbps |
| $f_{DDRX4}$ | DDRX4 ECLK Frequency | | — | 210 | — | 176 | — | 146 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 53 | — | 44 | — | 37 | MHz |

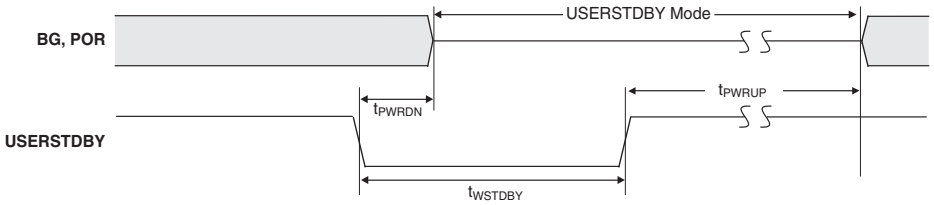
## MachXO2 Oscillator Output Frequency

| Symbol | Parameter | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|
| $f_{MAX}$ | Oscillator Output Frequency (Commercial Grade Devices, 0 to 85°C) | 125.685 | 133 | 140.315 | MHz |
| | Oscillator Output Frequency (Industrial Grade Devices, –40 °C to 100 °C) | 124.355 | 133 | 141.645 | MHz |
| $t_{DT}$ | Output Clock Duty Cycle | 43 | 50 | 57 | % |
| $t_{OPJIT}$[1] | Output Clock Period Jitter | 0.01 | 0.012 | 0.02 | UIPP |
| $t_{STABLEOSC}$ | STDBY Low to Oscillator Stable | 0.01 | 0.05 | 0.1 | µs |

1. Output Clock Period Jitter specified at 133 MHz. The values for lower frequencies will be smaller UIPP. The typical value for 133 MHz is 95 ps and for 2.08 MHz the typical value is 1.54 ns.

## MachXO2 Standby Mode Timing – HC/HE Devices

| Symbol | Parameter | Device | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PWRDN}$ | USERSTDBY High to Stop | All | — | — | 9 | ns |
| $t_{PWRUP}$ | USERSTDBY Low to Power Up | LCMXO2-256 | | — | | µs |
| | | LCMXO2-640 | | — | | µs |
| | | LCMXO2-640U | | — | | µs |
| | | LCMXO2-1200 | 20 | — | 50 | µs |
| | | LCMXO2-1200U | | — | | µs |
| | | LCMXO2-2000 | | — | | µs |
| | | LCMXO2-2000U | | — | | µs |
| | | LCMXO2-4000 | | — | | µs |
| | | LCMXO2-7000 | | — | | µs |
| $t_{WSTDBY}$ | USERSTDBY Pulse Width | All | 18 | — | — | ns |




## MachXO2 Standby Mode Timing – ZE Devices

| Symbol | Parameter | Device | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PWRDN}$ | USERSTDBY High to Stop | All | — | — | 13 | ns |
| $t_{PWRUP}$ | USERSTDBY Low to Power Up | LCMXO2-256 | | — | | µs |
| | | LCMXO2-640 | | — | | µs |
| | | LCMXO2-1200 | 20 | — | 50 | µs |
| | | LCMXO2-2000 | | — | | µs |
| | | LCMXO2-4000 | | — | | µs |
| | | LCMXO2-7000 | | — | | µs |
| $t_{WSTDBY}$ | USERSTDBY Pulse Width | All | 19 | — | — | ns |
| $t_{BNDGAPSTBL}$ | USERSTDBY High to Bandgap Stable | All | — | — | 15 | ns |

## Pinout Information Summary

| | MachXO2-256 | | | | | MachXO2-640 | | | MachXO2-640U |
|---|---|---|---|---|---|---|---|---|---|
| | 32 QFN[1] | 48 QFN[3] | 64 ucBGA | 100 TQFP | 132 csBGA | 48 QFN[3] | 100 TQFP | 132 csBGA | 144 TQFP |
| **General Purpose I/O per Bank** | | | | | | | | | |
| Bank 0 | 8 | 10 | 9 | 13 | 13 | 10 | 18 | 19 | 27 |
| Bank 1 | 2 | 10 | 12 | 14 | 14 | 10 | 20 | 20 | 26 |
| Bank 2 | 9 | 10 | 11 | 14 | 14 | 10 | 20 | 20 | 28 |
| Bank 3 | 2 | 10 | 12 | 14 | 14 | 10 | 20 | 20 | 26 |
| Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total General Purpose Single Ended I/O | 21 | 40 | 44 | 55 | 55 | 40 | 78 | 79 | 107 |
| | | | | | | | | | |
| **Differential I/O per Bank** | | | | | | | | | |
| Bank 0 | 4 | 5 | 5 | 7 | 7 | 5 | 9 | 10 | 14 |
| Bank 1 | 1 | 5 | 6 | 7 | 7 | 5 | 10 | 10 | 13 |
| Bank 2 | 4 | 5 | 5 | 7 | 7 | 5 | 10 | 10 | 14 |
| Bank 3 | 1 | 5 | 6 | 7 | 7 | 5 | 10 | 10 | 13 |
| Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total General Purpose Differential I/O | 10 | 20 | 22 | 28 | 28 | 20 | 39 | 40 | 54 |
| | | | | | | | | | |
| **Dual Function I/O** | 22 | 25 | 27 | 29 | 29 | 25 | 29 | 29 | 33 |
| **High-speed Differential I/O** | | | | | | | | | |
| Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 7 |
| **Gearboxes** | | | | | | | | | |
| Number of 7:1 or 8:1 Output Gearbox Available (Bank 0) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 7 |
| Number of 7:1 or 8:1 Input Gearbox Available (Bank 2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 7 |
| **DQS Groups** | | | | | | | | | |
| Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 |
| | | | | | | | | | |
| **VCCIO Pins** | | | | | | | | | |
| Bank 0 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 3 |
| Bank 1 | 1 | 1 | 2 | 2 | 2 | 1 | 2 | 2 | 3 |
| Bank 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 3 |
| Bank 3 | 1 | 1 | 2 | 2 | 2 | 1 | 2 | 2 | 3 |
| Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | | |
| VCC | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 4 |
| GND[2] | 2 | 1 | 8 | 8 | 8 | 1 | 8 | 10 | 12 |
| NC | 0 | 0 | 1 | 26 | 58 | 0 | 3 | 32 | 8 |
| Reserved for Configuration | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Total Count of Bonded Pins | 32 | 49 | 64 | 100 | 132 | 49 | 100 | 132 | 144 |

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.
2. For 48 QFN package, exposed die pad is the device ground.
3. 48-pin QFN information is 'Advanced'.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000HE-6BG332C | 4320 | 1.2 V | –6 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HE-4FG484C | 4320 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HE-5FG484C | 4320 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HE-6FG484C | 4320 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000HE-4TG144C | 6864 | 1.2 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000HE-5TG144C | 6864 | 1.2 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000HE-6TG144C | 6864 | 1.2 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000HE-4BG256C | 6864 | 1.2 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000HE-5BG256C | 6864 | 1.2 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000HE-6BG256C | 6864 | 1.2 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000HE-4FTG256C | 6864 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000HE-5FTG256C | 6864 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000HE-6FTG256C | 6864 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000HE-4BG332C | 6864 | 1.2 V | –4 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000HE-5BG332C | 6864 | 1.2 V | –5 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000HE-6BG332C | 6864 | 1.2 V | –6 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000HE-4FG484C | 6864 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000HE-5FG484C | 6864 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000HE-6FG484C | 6864 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | COM |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000ZE-1QN84I | 4320 | 1.2 V | –1 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000ZE-2QN84I | 4320 | 1.2 V | –2 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000ZE-3QN84I | 4320 | 1.2 V | –3 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000ZE-1MG132I | 4320 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000ZE-2MG132I | 4320 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000ZE-3MG132I | 4320 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000ZE-1TG144I | 4320 | 1.2 V | –1 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000ZE-2TG144I | 4320 | 1.2 V | –2 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000ZE-3TG144I | 4320 | 1.2 V | –3 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000ZE-1BG256I | 4320 | 1.2 V | –1 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000ZE-2BG256I | 4320 | 1.2 V | –2 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000ZE-3BG256I | 4320 | 1.2 V | –3 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000ZE-1FTG256I | 4320 | 1.2 V | –1 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000ZE-2FTG256I | 4320 | 1.2 V | –2 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000ZE-3FTG256I | 4320 | 1.2 V | –3 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000ZE-1BG332I | 4320 | 1.2 V | –1 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000ZE-2BG332I | 4320 | 1.2 V | –2 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000ZE-3BG332I | 4320 | 1.2 V | –3 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000ZE-1FG484I | 4320 | 1.2 V | –1 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000ZE-2FG484I | 4320 | 1.2 V | –2 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000ZE-3FG484I | 4320 | 1.2 V | –3 | Halogen-Free fpBGA | 484 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000ZE-1TG144I | 6864 | 1.2 V | –1 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000ZE-2TG144I | 6864 | 1.2 V | –2 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000ZE-3TG144I | 6864 | 1.2 V | –3 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000ZE-1BG256I | 6864 | 1.2 V | –1 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000ZE-2BG256I | 6864 | 1.2 V | –2 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000ZE-3BG256I | 6864 | 1.2 V | –3 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000ZE-1FTG256I | 6864 | 1.2 V | –1 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000ZE-2FTG256I | 6864 | 1.2 V | –2 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000ZE-3FTG256I | 6864 | 1.2 V | –3 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000ZE-1BG332I | 6864 | 1.2 V | –1 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000ZE-2BG332I | 6864 | 1.2 V | –2 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000ZE-3BG332I | 6864 | 1.2 V | –3 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000ZE-1FG484I | 6864 | 1.2 V | –1 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000ZE-2FG484I | 6864 | 1.2 V | –2 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000ZE-3FG484I | 6864 | 1.2 V | –3 | Halogen-Free fpBGA | 484 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-1200HC-4TG100IR1[1] | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200HC-5TG100IR1[1] | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200HC-6TG100IR1[1] | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200HC-4MG132IR1[1] | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200HC-5MG132IR1[1] | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200HC-6MG132IR1[1] | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200HC-4TG144IR1[1] | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200HC-5TG144IR1[1] | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200HC-6TG144IR1[1] | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |

1. Specifications for the “LCMXO2-1200HC-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

## High Performance Industrial Grade Devices Without Voltage Regulator, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000HE-4TG100I | 2112 | 1.2 V | –4 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-2000HE-5TG100I | 2112 | 1.2 V | –5 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-2000HE-6TG100I | 2112 | 1.2 V | –6 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-2000HE-4MG132I | 2112 | 1.2 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-2000HE-5MG132I | 2112 | 1.2 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-2000HE-6MG132I | 2112 | 1.2 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-2000HE-4TG144I | 2112 | 1.2 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000HE-5TG144I | 2112 | 1.2 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000HE-6TG144I | 2112 | 1.2 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000HE-4BG256I | 2112 | 1.2 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-2000HE-5BG256I | 2112 | 1.2 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-2000HE-6BG256I | 2112 | 1.2 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-2000HE-4FTG256I | 2112 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-2000HE-5FTG256I | 2112 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-2000HE-6FTG256I | 2112 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000UHE-4FG484I | 2112 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-2000UHE-5FG484I | 2112 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-2000UHE-6FG484I | 2112 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | IND |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| December 2014 | 2.9 | Introduction | Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide.<br>— Removed XO2-4000U data.<br>— Removed 400-ball ftBGA.<br>— Removed 25-ball WLCSP value for XO2-2000U. |
| | | DC and Switching Characteristics | Updated the Recommended Operating Conditions section. Adjusted Max. values for $V_{CC}$ and $V_{CCIO}$. |
| | | | Updated the sysIO Recommended Operating Conditions section. Adjusted Max. values for LVCMOS 3.3, LVTTL, PCI, LVDS33 and LVPECL. |
| | | Pinout Information | Updated the Pinout Information Summary section. Removed MachXO2-4000U. |
| | | Ordering Information | Updated the MachXO2 Part Number Description section. Removed BG400 package. |
| | | | Updated the High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers. |
| | | | Updated the High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers. |
| November 2014 | 2.8 | Introduction | Updated the Features section.<br>— Revised I/Os under Flexible Logic Architecture.<br>— Revised standby power under Ultra Low Power Devices.<br>— Revise input frequency range under Flexible On-Chip Clocking. |
| | | | Updated Table 1-1, MachXO2 Family Selection Guide.<br>— Added XO2-4000U data.<br>— Removed HE and ZE device options for XO2-4000.<br>— Added 400-ball ftBGA. |
| | | Pinout Information | Updated the Pinout Information Summary section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400. |
| | | Ordering Information | Updated the MachXO2 Part Number Description section. Added BG400 package. |
| | | | Updated the Ordering Information section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400 part numbers. |
| October 2014 | 2.7 | Ordering Information | Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Fixed typo in LCMXO2-2000ZE-1UWG49ITR part number package. |
| | | Architecture | Updated the Supported Standards section. Added MIPI information to Table 2-12. Supported Input Standards and Table 2-13. Supported Output Standards. |
| | | DC and Switching Characteristics | Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition. |
| | | | Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition. |
| | | | Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values. |
| July 2014 | 2.6 | DC and Switching Characteristics | Updated sysIO Single-Ended DC Electrical Characteristics[1, 2] section. Updated footnote 4. |
| | | | Updated Register-to-Register Performance section. Updated footnote. |
| | | Ordering Information | Updated UW49 package to UWG49 in MachXO2 Part Number Description. |
| | | | Updated LCMXO2-2000ZE-1UWG49CTR package in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging. |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| May 2014 | 2.5 | Architecture | Updated TransFR (Transparent Field Reconfiguration) section.<br>Updated TransFR description for PLL use during background Flash programming. |
| February 2014 | 02.4 | Introduction | Included the 49 WLCSP package in the MachXO2 Family Selection Guide table. |
| | | Architecture | Added information to Standby Mode and Power Saving Options section. |
| | | Pinout Information | Added the XO2-2000 49 WLCSP in the Pinout Information Summary table. |
| | | Ordering Information | Added UW49 package in MachXO2 Part Number Description. |
| | | | Added and LCMXO2-2000ZE-1UWG49CTR in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging section. |
| | | | Added and LCMXO2-2000ZE-1UWG49ITR in Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. |
| December 2013 | 02.3 | Architecture | Updated information on CLKOS output divider in sysCLOCK Phase Locked Loops (PLLs) section. |
| | | DC and Switching Characteristics | Updated Static Supply Current – ZE Devices table. |
| | | | Updated footnote 4 in sysIO Single-Ended DC Electrical Characteristics table; Updated $V_{IL}$ Max. (V) data for LVCMOS 25 and LVCMOS 28. |
| | | | Updated $V_{OS}$ test condition in sysIO Differential Electrical Characteristics - LVDS table. |
| September 2013 | 02.2 | Architecture | Removed $I^2C$ Clock-Stretching feature per PCN #10A-13. |
| | | | Removed information on PDPR memory in RAM Mode section. |
| | | | Updated Supported Input Standards table. |
| | | DC and Switching Characteristics | Updated Power-On-Reset Voltage Levels table. |
| June 2013 | 02.1 | Architecture | Architecture Overview – Added information on the state of the register on power up and after configuration. |
| | | | sysCLOCK Phase Locked Loops (PLLs) section – Added missing cross reference to sysCLOCK PLL Timing table. |
| | | DC and Switching Characteristics | Added slew rate information to footnote 2 of the MachXO2 External Switching Characteristics – HC/HE Devices and the MachXO2 External Switching Characteristics – ZE Devices tables. |
| | | | Power-On-Reset Voltage Levels table – Added symbols. |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| January 2013 | 02.0 | Introduction | Updated the total number IOs to include JTAGENB. |
| | | Architecture | Supported Output Standards table – Added 3.3 $V_{CCIO}$ (Typ.) to LVDS row. |
| | | | Changed SRAM CRC Error Detection to Soft Error Detection. |
| | | DC and Switching Characteristics | Power Supply Ramp Rates table – Updated Units column for $t_{RAMP}$ symbol. |
| | | | Added new Maximum sysIO Buffer Performance table. |
| | | | sysCLOCK PLL Timing table – Updated Min. column values for $f_{IN}$, $f_{OUT}$, $f_{OUT2}$ and $f_{PFD}$ parameters. Added $t_{SPO}$ parameter. Updated footnote 6. |
| | | | MachXO2 Oscillator Output Frequency table – Updated symbol name for $t_{STABLEOSC.}$ |
| | | | DC Electrical Characteristics table – Updated conditions for $I_{IL,}$ $I_{IH}$ symbols. |
| | | | Corrected parameters tDQVBS and tDQVAS |
| | | | Corrected MachXO2 ZE parameters tDVADQ and tDVEDQ |
| | | Pinout Information | Included the MachXO2-4000HE 184 csBGA package. |
| | | Ordering Information | Updated part number. |
| April 2012 | 01.9 | Architecture | Removed references to TN1200. |
| | | Ordering Information | Updated the Device Status portion of the MachXO2 Part Number Description to include the 50 parts per reel for the WLCSP package. |
| | | | Added new part number and footnote 2 for LCMXO2-1200ZE-1UWG25ITR50. |
| | | | Updated footnote 1 for LCMXO2-1200ZE-1UWG25ITR. |
| | | Supplemental Information | Removed references to TN1200. |
| March 2012 | 01.8 | Introduction | Added 32 QFN packaging information to Features bullets and MachXO2 Family Selection Guide table. |
| | | DC and Switching Characteristics | Changed ‘STANDBY’ to ‘USERSTDBY’ in Standby Mode timing diagram. |
| | | Pinout Information | Removed footnote from Pin Information Summary tables. |
| | | | Added 32 QFN package to Pin Information Summary table. |
| | | Ordering Information | Updated Part Number Description and Ordering Information tables for 32 QFN package. |
| | | | Updated topside mark diagram in the Ordering Information section. |