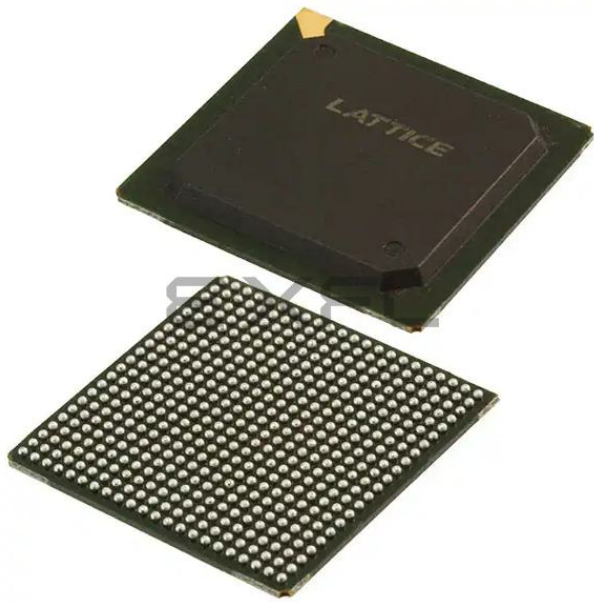




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

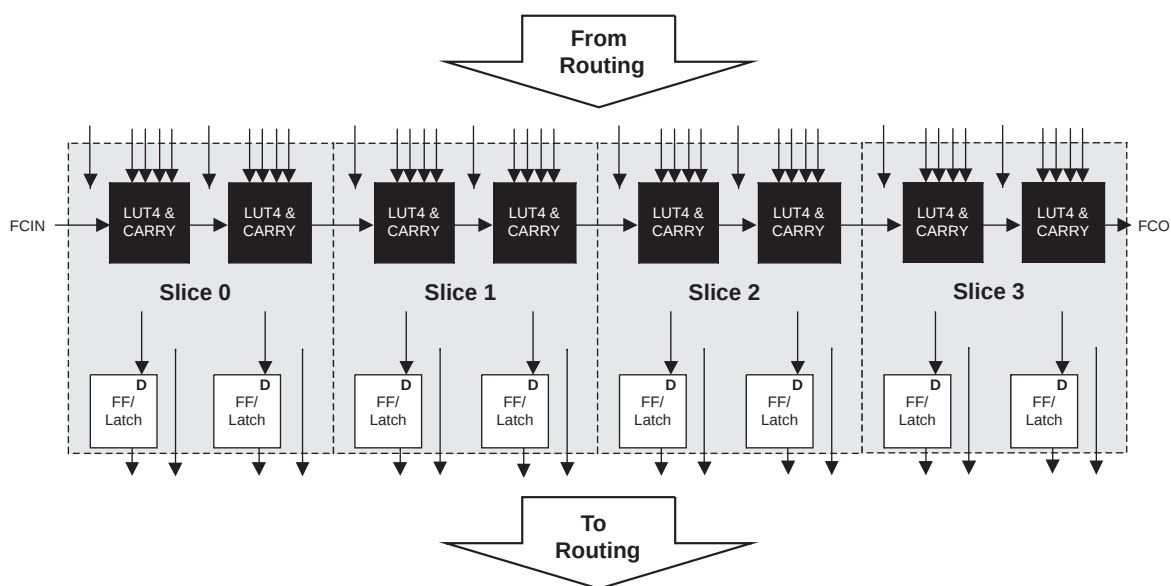
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	858
Number of Logic Elements/Cells	6864
Total RAM Bits	245760
Number of I/O	334
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmx02-7000ze-3fg484i

Figure 2-3. PFU Block Diagram



Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU Block	
	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.
3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

Table 2-7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

More information on the input gearbox is available in TN1203, [Implementing High-Speed Interfaces with MachXO2 Devices](#).

Output Gearbox

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDR4 (8:1) gearbox or as two ODDR2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

Table 2-10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDR4(8:1): D[7:0]		
GDDR2(4:1)(IOL-A): D[3:0]		
GDDR2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-17 shows the output gearbox block diagram.

Figure 2-21. I²C Core Block Diagram

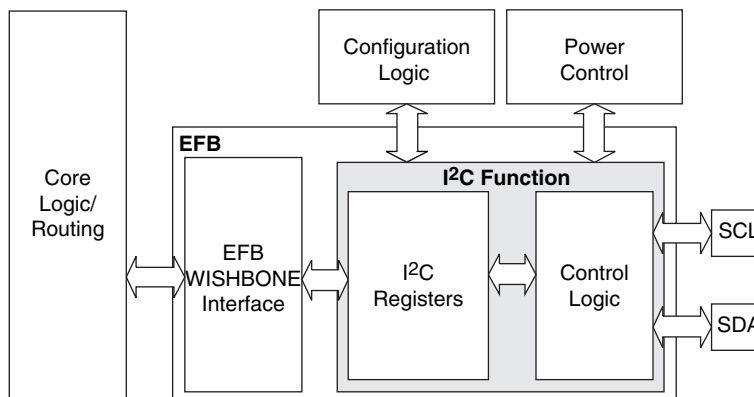


Table 2-15 describes the signals interfacing with the I²C cores.

Table 2-15. I²C Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I ² C core. The signal is an output if the I ² C core is in master mode. The signal is an input if the I ² C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I ² C ports in each MachXO2 device.
i2c_sda	Bi-directional	Bi-directional data line of the I ² C core. The signal is an output when data is transmitted from the I ² C core. The signal is an input when data is received into the I ² C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I ² C ports in each MachXO2 device.
i2c_irqo	Output	Interrupt request output signal of the I ² C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I ² C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I ² C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I ² C Tab.

Hardened SPI IP Core

Every MachXO2 device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO2 devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface

Power-On-Reset Voltage Levels^{1, 2, 3, 4, 5}

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and V_{CCIO0})	0.9	—	1.06	V
$V_{PORUPEXT}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	—	2.1	V
$V_{PORDNBG}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CCINT})	0.75	—	0.93	V
$V_{PORDNBGEXT}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	—	1.33	V
$V_{PORDNSRAM}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CCINT})	—	0.6	—	V
$V_{PORDNSRAMEXT}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	—	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.
3. Note that V_{PORUP} (min.) and $V_{PORDNBG}$ (max.) are in different process corners. For any given process corner $V_{PORDNBG}$ (max.) is always 12.0 mV below V_{PORUP} (min.).
4. $V_{PORUPEXT}$ is for HC devices only. In these devices a separate POR circuit monitors the external V_{CC} power supply.
5. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

Programming/Erase Specifications

Symbol	Parameter	Min.	Max. ¹	Units
N_{PROG}	Flash Programming cycles per $t_{RETENTION}$	—	10,000	Cycles
	Flash functional programming cycles	—	100,000	
$t_{RETENTION}$	Data retention at 100 °C junction temperature	10	—	Years
	Data retention at 85 °C junction temperature	20	—	

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

Hot Socketing Specifications^{1, 2, 3}

Symbol	Parameter	Condition	Max.	Units
I_{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/-1000	μA

1. Insensitive to sequence of V_{CC} and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO} .
2. $0 < V_{CC} < V_{CC} (MAX)$, $0 < V_{CCIO} < V_{CCIO} (MAX)$.
3. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} .

ESD Performance

Please refer to the [MachXO2 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

Static Supply Current – ZE Devices^{1, 2, 3, 6}

Symbol	Parameter	Device	Typ. ⁴	Units
I_{CC}	Core Power Supply	LCMXO2-256ZE	18	μA
		LCMXO2-640ZE	28	μA
		LCMXO2-1200ZE	56	μA
		LCMXO2-2000ZE	80	μA
		LCMXO2-4000ZE	124	μA
		LCMXO2-7000ZE	189	μA
I_{CCIO}	Bank Power Supply ⁵ $V_{CCIO} = 2.5 V$	All devices	1	μA

- For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).
- Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off. To estimate the impact of turning each of these items on, please refer to the following table or for more detail with your specific design use the Power Calculator tool.
- Frequency = 0 MHz.
- $T_J = 25^\circ C$, power supplies at nominal voltage.
- Does not include pull-up/pull-down.
- To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Static Power Consumption Contribution of Different Components – ZE Devices

The table below can be used for approximating static power consumption. For a more accurate power analysis for your design please use the Power Calculator tool.

Symbol	Parameter	Typ.	Units
I_{DCBG}	Bandgap DC power contribution	101	μA
I_{DCPOR}	POR DC power contribution	38	μA
$I_{DCIOBANKCONTROLLER}$	DC power contribution per I/O bank controller	143	μA

sysIO Recommended Operating Conditions

Standard	V _{CCIO} (V)			V _{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS 3.3	3.135	3.3	3.6	—	—	—
LVC MOS 2.5	2.375	2.5	2.625	—	—	—
LVC MOS 1.8	1.71	1.8	1.89	—	—	—
LVC MOS 1.5	1.425	1.5	1.575	—	—	—
LVC MOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.6	—	—	—
PCI ³	3.135	3.3	3.6	—	—	—
SSTL25	2.375	2.5	2.625	1.15	1.25	1.35
SSTL18	1.71	1.8	1.89	0.833	0.9	0.969
HSTL18	1.71	1.8	1.89	0.816	0.9	1.08
LVC MOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVC MOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVC MOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVC MOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVC MOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVC MOS12R33 ⁴	3.135	3.3	3.6	0.45	0.6	0.75
LVC MOS12R25 ⁴	2.375	2.5	2.625	0.45	0.6	0.75
LVC MOS10R33 ⁴	3.135	3.3	3.6	0.35	0.5	0.65
LVC MOS10R25 ⁴	2.375	2.5	2.625	0.35	0.5	0.65
LVDS25 ^{1, 2}	2.375	2.5	2.625	—	—	—
LVDS33 ^{1, 2}	3.135	3.3	3.6	—	—	—
LVPECL ¹	3.135	3.3	3.6	—	—	—
BLVDS ¹	2.375	2.5	2.625	—	—	—
RSDS ¹	2.375	2.5	2.625	—	—	—
SSTL18D	1.71	1.8	1.89	—	—	—
SSTL25D	2.375	2.5	2.625	—	—	—
HSTL18D	1.71	1.8	1.89	—	—	—

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.

2. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.

3. Input on the bottom bank of the MachXO2-640U, MachXO2-1200/U and larger devices only.

4. Supported only for inputs and BIDs for all ZE devices, and –6 speed grade for HE and HC devices.

BLVDS

The MachXO2 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

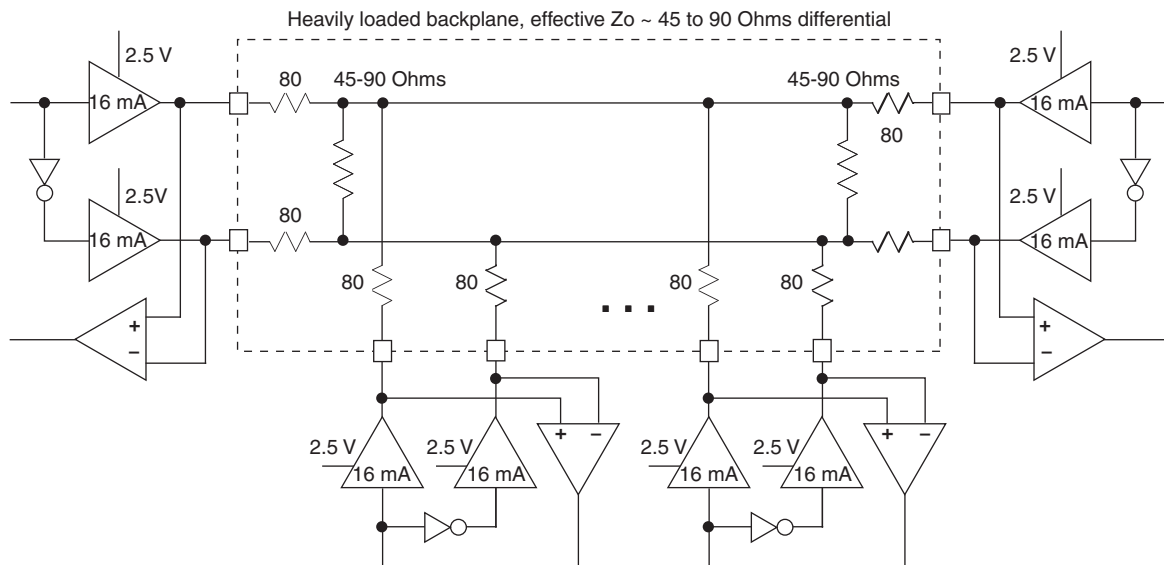


Table 3-2. BLVDS DC Conditions¹

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z _{OUT}	Output impedance	20	20	Ohms
R _S	Driver series resistance	80	80	Ohms
R _{TLEFT}	Left end termination	45	90	Ohms
R _{TRIGHT}	Right end termination	45	90	Ohms
V _{OH}	Output high voltage	1.376	1.480	V
V _{OL}	Output low voltage	1.124	1.020	V
V _{OD}	Output differential voltage	0.253	0.459	V
V _{CM}	Output common mode voltage	1.250	1.250	V
I _{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.

MachXO2 External Switching Characteristics – HC/HE Devices^{1, 2, 3, 4, 5, 6, 7}

Over Recommended Operating Conditions

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f _{MAX_PRI} ⁸	Frequency for Primary Clock Tree	All MachXO2 devices	—	388	—	323	—	269	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	0.5	—	0.6	—	0.7	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO2-256HC-HE	—	912	—	939	—	975	ps
		MachXO2-640HC-HE	—	844	—	871	—	908	ps
		MachXO2-1200HC-HE	—	868	—	902	—	951	ps
		MachXO2-2000HC-HE	—	867	—	897	—	941	ps
		MachXO2-4000HC-HE	—	865	—	892	—	931	ps
		MachXO2-7000HC-HE	—	902	—	942	—	989	ps
Edge Clock									
f _{MAX_EDGE} ⁸	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	400	—	333	—	278	MHz
Pin-LUT-Pin Propagation Delay									
t _{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	—	6.72	—	6.96	—	7.24	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t _{CO}	Clock to Output – PIO Output Register	MachXO2-256HC-HE	—	7.13	—	7.30	—	7.57	ns
		MachXO2-640HC-HE	—	7.15	—	7.30	—	7.57	ns
		MachXO2-1200HC-HE	—	7.44	—	7.64	—	7.94	ns
		MachXO2-2000HC-HE	—	7.46	—	7.66	—	7.96	ns
		MachXO2-4000HC-HE	—	7.51	—	7.71	—	8.01	ns
		MachXO2-7000HC-HE	—	7.54	—	7.75	—	8.06	ns
t _{SU}	Clock to Data Setup – PIO Input Register	MachXO2-256HC-HE	–0.06	—	–0.06	—	–0.06	—	ns
		MachXO2-640HC-HE	–0.06	—	–0.06	—	–0.06	—	ns
		MachXO2-1200HC-HE	–0.17	—	–0.17	—	–0.17	—	ns
		MachXO2-2000HC-HE	–0.20	—	–0.20	—	–0.20	—	ns
		MachXO2-4000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-7000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
t _H	Clock to Data Hold – PIO Input Register	MachXO2-256HC-HE	1.75	—	1.95	—	2.16	—	ns
		MachXO2-640HC-HE	1.75	—	1.95	—	2.16	—	ns
		MachXO2-1200HC-HE	1.88	—	2.12	—	2.36	—	ns
		MachXO2-2000HC-HE	1.89	—	2.13	—	2.37	—	ns
		MachXO2-4000HC-HE	1.94	—	2.18	—	2.43	—	ns
		MachXO2-7000HC-HE	1.98	—	2.23	—	2.49	—	ns

Parameter	Description	Device	-6		-5		-4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR ^{9, 12}									
t _{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. ¹³	—	0.369	—	0.395	—	0.421	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.529	—	0.530	—	0.527	—	UI
t _{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f _{DATA}	MEM LPDDR Serial Data Speed		—	280	—	250	—	208	Mbps
f _{SCLK}	SCLK Frequency		—	140	—	125	—	104	MHz
f _{LPDDR}	LPDDR Data Transfer Rate		0	280	0	250	0	208	Mbps
DDR ^{9, 12}									
t _{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. ¹³	—	0.350	—	0.387	—	0.414	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.545	—	0.538	—	0.532	—	UI
t _{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f _{DATA}	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f _{SCLK}	SCLK Frequency		—	150	—	125	—	104	MHz
f _{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps
DDR2 ^{9, 12}									
t _{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. ¹³	—	0.360	—	0.378	—	0.406	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.555	—	0.549	—	0.542	—	UI
t _{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f _{DATA}	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f _{SCLK}	SCLK Frequency		—	150	—	125	—	104	MHz
f _{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps

- Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
- General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
- Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
- DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
- 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
- For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$.
- The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps (-6), 113 ps (-5), 120 ps (-4).
- This number for general purpose usage. Duty cycle tolerance is +/- 10%.
- Duty cycle is +/-5% for system usage.
- The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
- High-speed DDR and LVDS not supported in SG32 (32 QFN) packages.
- Advance information for MachXO2 devices in 48 QFN packages.
- DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

MachXO2 External Switching Characteristics – ZE Devices^{1, 2, 3, 4, 5, 6, 7}

Over Recommended Operating Conditions

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f _{MAX_PRI} ⁸	Frequency for Primary Clock Tree	All MachXO2 devices	—	150	—	125	—	104	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	1.00	—	1.20	—	1.40	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO2-256ZE	—	1250	—	1272	—	1296	ps
		MachXO2-640ZE	—	1161	—	1183	—	1206	ps
		MachXO2-1200ZE	—	1213	—	1267	—	1322	ps
		MachXO2-2000ZE	—	1204	—	1250	—	1296	ps
		MachXO2-4000ZE	—	1195	—	1233	—	1269	ps
		MachXO2-7000ZE	—	1243	—	1268	—	1296	ps
Edge Clock									
f _{MAX_EDGE} ⁸	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	210	—	175	—	146	MHz
Pin-LUT-Pin Propagation Delay									
t _{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	—	9.35	—	9.78	—	10.21	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t _{CO}	Clock to Output – PIO Output Register	MachXO2-256ZE	—	10.46	—	10.86	—	11.25	ns
		MachXO2-640ZE	—	10.52	—	10.92	—	11.32	ns
		MachXO2-1200ZE	—	11.24	—	11.68	—	12.12	ns
		MachXO2-2000ZE	—	11.27	—	11.71	—	12.16	ns
		MachXO2-4000ZE	—	11.28	—	11.78	—	12.28	ns
		MachXO2-7000ZE	—	11.22	—	11.76	—	12.30	ns
t _{SU}	Clock to Data Setup – PIO Input Register	MachXO2-256ZE	–0.21	—	–0.21	—	–0.21	—	ns
		MachXO2-640ZE	–0.22	—	–0.22	—	–0.22	—	ns
		MachXO2-1200ZE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-2000ZE	–0.27	—	–0.27	—	–0.27	—	ns
		MachXO2-4000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-7000ZE	–0.33	—	–0.33	—	–0.33	—	ns
t _H	Clock to Data Hold – PIO Input Register	MachXO2-256ZE	3.96	—	4.25	—	4.65	—	ns
		MachXO2-640ZE	4.01	—	4.31	—	4.71	—	ns
		MachXO2-1200ZE	3.95	—	4.29	—	4.73	—	ns
		MachXO2-2000ZE	3.94	—	4.29	—	4.74	—	ns
		MachXO2-4000ZE	3.96	—	4.36	—	4.87	—	ns
		MachXO2-7000ZE	3.93	—	4.37	—	4.91	—	ns

Figure 3-5. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms

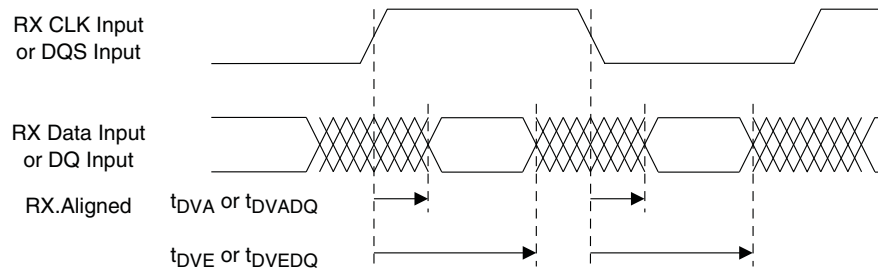


Figure 3-6. Receiver RX.CLK.Centered Waveforms

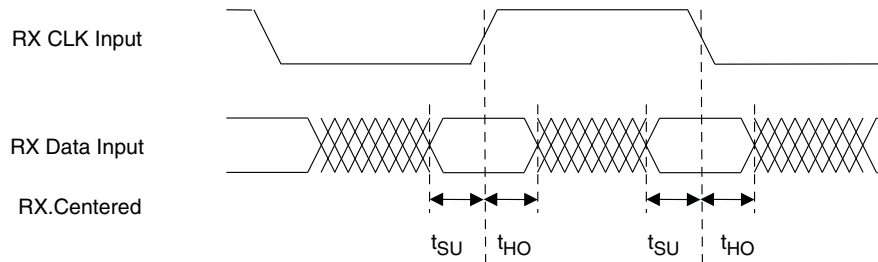


Figure 3-7. Transmitter TX.CLK.Aligned Waveforms

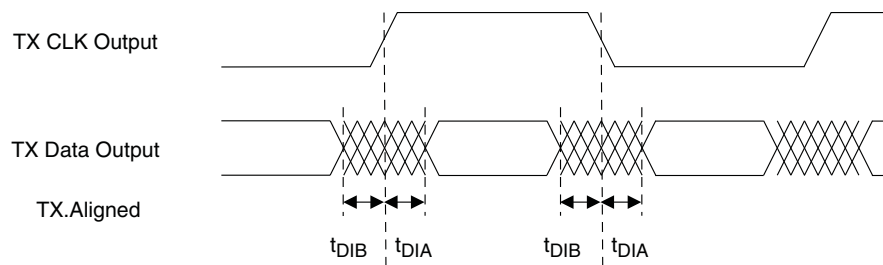


Figure 3-8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms

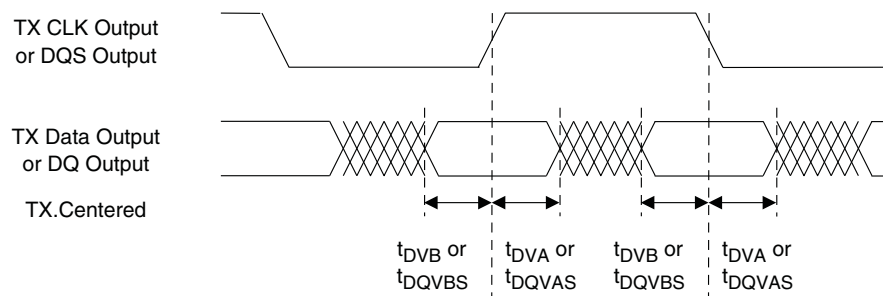
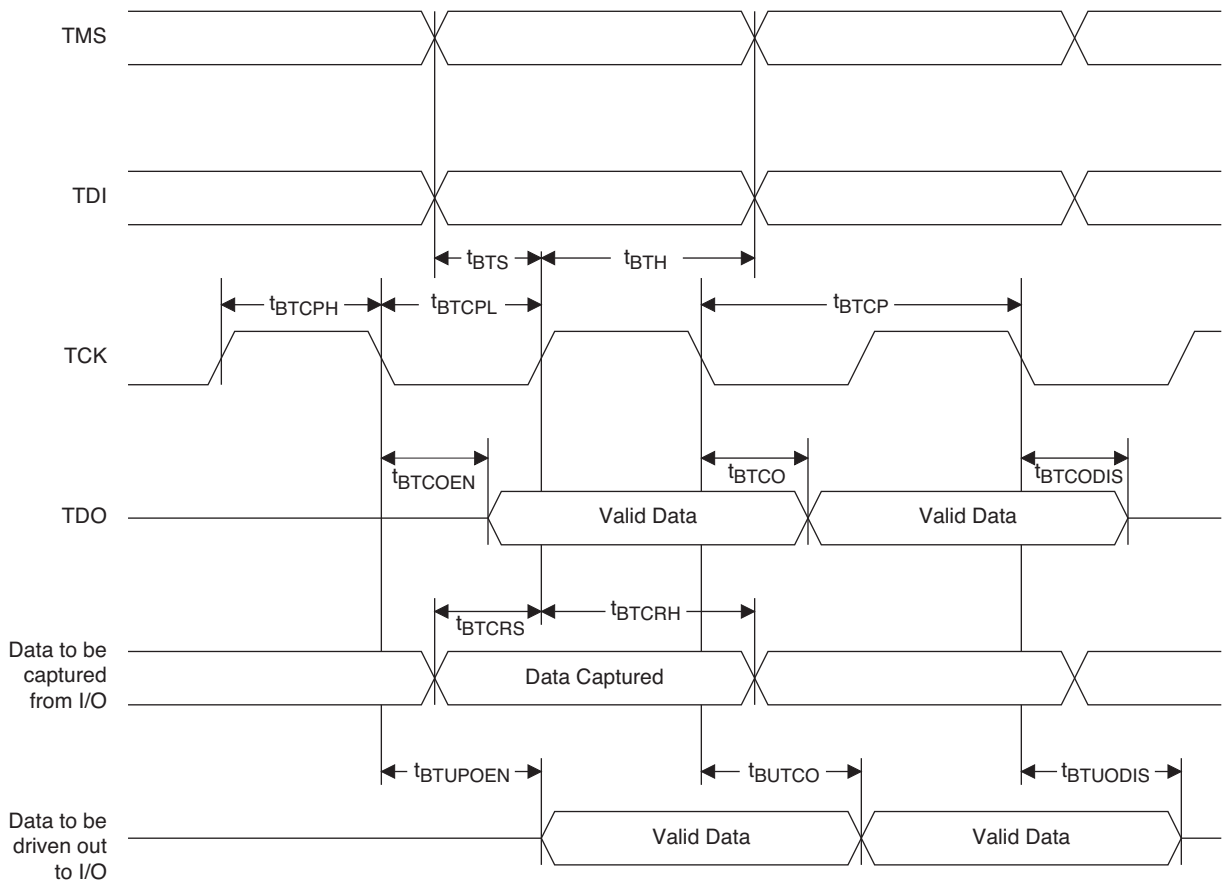


Figure 3-12. JTAG Port Timing Waveforms



	MachXO2-1200					MachXO2-1200U
	100 TQFP	132 csBGA	144 TQFP	25 WLCSP	32 QFN ¹	256 ftBGA
General Purpose I/O per Bank						
Bank 0	18	25	27	11	9	50
Bank 1	21	26	26	0	2	52
Bank 2	20	28	28	7	9	52
Bank 3	20	25	26	0	2	16
Bank 4	0	0	0	0	0	16
Bank 5	0	0	0	0	0	20
Total General Purpose Single Ended I/O	79	104	107	18	22	206
Differential I/O per Bank						
Bank 0	9	13	14	5	4	25
Bank 1	10	13	13	0	1	26
Bank 2	10	14	14	2	4	26
Bank 3	10	12	13	0	1	8
Bank 4	0	0	0	0	0	8
Bank 5	0	0	0	0	0	10
Total General Purpose Differential I/O	39	52	54	7	10	103
Dual Function I/O						
	31	33	33	18	22	33
High-speed Differential I/O						
Bank 0	4	7	7	0	0	14
Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	4	7	7	0	0	14
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	5	7	7	0	2	14
DQS Groups						
Bank 1	1	2	2	0	0	2
VCCIO Pins						
Bank 0	2	3	3	1	2	4
Bank 1	2	3	3	0	1	4
Bank 2	2	3	3	1	2	4
Bank 3	3	3	3	0	1	1
Bank 4	0	0	0	0	0	2
Bank 5	0	0	0	0	0	1
VCC	2	4	4	2	2	8
GND	8	10	12	2	2	24
NC	1	1	8	0	0	1
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	100	132	144	25	32	256

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.

For Further Information

For further information regarding logic signal connections for various packages please refer to the MachXO2 Device Pinout Files.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Users must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- [Thermal Management](#) document
- TN1198, [Power Estimation and Management for MachXO2 Devices](#)
- The Power Calculator tool is included with the Lattice design tools, or as a standalone download from www.latticesemi.com/software

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144C	6864	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-2TG144C	6864	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-3TG144C	6864	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-1BG256C	6864	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-2BG256C	6864	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-3BG256C	6864	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-1FTG256C	6864	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-2FTG256C	6864	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-3FTG256C	6864	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-1BG332C	6864	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-2BG332C	6864	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-3BG332C	6864	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-1FG484C	6864	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-2FG484C	6864	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-3FG484C	6864	1.2 V	–3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100CR1 ¹	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100CR1 ¹	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100CR1 ¹	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132CR1 ¹	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132CR1 ¹	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132CR1 ¹	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144CR1 ¹	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144CR1 ¹	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144CR1 ¹	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200ZE-speed package CR1” are the same as the “LCMXO2-1200ZE-speed package C” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100C	2112	1.2 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-5TG100C	2112	1.2 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-6TG100C	2112	1.2 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-4TG144C	2112	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-5TG144C	2112	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-6TG144C	2112	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-4MG132C	2112	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-5MG132C	2112	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-6MG132C	2112	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-4BG256C	2112	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-5BG256C	2112	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-6BG256C	2112	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-4FTG256C	2112	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-5FTG256C	2112	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-6FTG256C	2112	1.2 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484C	2112	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-5FG484C	2112	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-6FG484C	2112	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4TG144C	4320	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-5TG144C	4320	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-6TG144C	4320	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-4MG132C	4320	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-5MG132C	4320	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-6MG132C	4320	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-4BG256C	4320	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4MG184C	4320	1.2 V	–4	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5MG184C	4320	1.2 V	–5	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-6MG184C	4320	1.2 V	–6	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5BG256C	4320	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-6BG256C	4320	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4FTG256C	4320	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-5FTG256C	4320	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-6FTG256C	4320	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-4BG332C	4320	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-5BG332C	4320	1.2 V	–5	Halogen-Free caBGA	332	COM

Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32I	256	1.2 V	–1	Halogen-Free QFN	32	IND
LCMXO2-256ZE-2SG32I	256	1.2 V	–2	Halogen-Free QFN	32	IND
LCMXO2-256ZE-3SG32I	256	1.2 V	–3	Halogen-Free QFN	32	IND
LCMXO2-256ZE-1UMG64I	256	1.2 V	–1	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-2UMG64I	256	1.2 V	–2	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-3UMG64I	256	1.2 V	–3	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-1TG100I	256	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-2TG100I	256	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-3TG100I	256	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-1MG132I	256	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-2MG132I	256	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-3MG132I	256	1.2 V	–3	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100I	640	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-2TG100I	640	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-3TG100I	640	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-1MG132I	640	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-2MG132I	640	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-3MG132I	640	1.2 V	–3	Halogen-Free csBGA	132	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1UWG25ITR ¹	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR50 ³	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR1K ²	1280	1.2 V	–1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1SG32I	1280	1.2 V	–1	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-2SG32I	1280	1.2 V	–2	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-3SG32I	1280	1.2 V	–3	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-1TG100I	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100I	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100I	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132I	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132I	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132I	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144I	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144I	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144I	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1UWG49ITR ¹	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR50 ³	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR1K ²	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1TG100I	2112	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-2TG100I	2112	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-3TG100I	2112	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-1MG132I	2112	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-2MG132I	2112	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-3MG132I	2112	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-1TG144I	2112	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-2TG144I	2112	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-3TG144I	2112	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-1BG256I	2112	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-2BG256I	2112	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-3BG256I	2112	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-1FTG256I	2112	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-2FTG256I	2112	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-3FTG256I	2112	1.2 V	–3	Halogen-Free ftBGA	256	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84I	4320	2.5 V / 3.3 V	–4	Halogen-Free QFN	84	IND
LCMXO2-4000HC-5QN84I	4320	2.5 V / 3.3 V	–5	Halogen-Free QFN	84	IND
LCMXO2-4000HC-6QN84I	4320	2.5 V / 3.3 V	–6	Halogen-Free QFN	84	IND
LCMXO2-4000HC-4TG144I	4320	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-5TG144I	4320	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-6TG144I	4320	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-4MG132I	4320	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-5MG132I	4320	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-6MG132I	4320	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-4BG256I	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-5BG256I	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-6BG256I	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-4FTG256I	4320	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-5FTG256I	4320	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-6FTG256I	4320	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-4BG332I	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-5BG332I	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-6BG332I	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-4FG484I	4320	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-5FG484I	4320	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-6FG484I	4320	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144I	6864	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-5TG144I	6864	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-6TG144I	6864	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-4BG256I	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-5BG256I	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-6BG256I	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-4FTG256I	6864	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-5FTG256I	6864	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-6FTG256I	6864	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-4BG332I	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-5BG332I	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-6BG332I	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-4FG400I	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-5FG400I	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-6FG400I	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-4FG484I	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-5FG484I	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-6FG484I	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND