

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XF

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	12
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f08kl200-e-st

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams: PIC24FXXKL301/401



		Pin Number				
Function	20-Pin PDIP/ SSOP/ SOIC	20-Pin QFN	14-Pin PDIP/ TSSOP	I/O	Buffer	Description
SCK1	15	12	8	I/O	ST	MSSP1 SPI Serial Input/Output Clock
SCL1	12	9	8	I/O	I ² C	MSSP1 I ² C Clock Input/Output
SCLKI	10	7	12	I	ST	Digital Secondary Clock Input
SDA1	13	10	9	I/O	I ² C	MSSP1 I ² C Data Input/Output
SDI1	17	14	11	I	ST	MSSP1 SPI Serial Data Input
SDO1	16	13	9	0	—	MSSP1 SPI Serial Data Output
SOSCI	9	6	11	I	ANA	Secondary Oscillator Input
SOSCO	10	7	12	0	ANA	Secondary Oscillator Output
SS1	12	9	12	0	_	SPI1 Slave Select
T1CK	13	10	9	I	ST	Timer1 Clock
ТЗСК	18	15	12	I	ST	Timer3 Clock
T3G	6	3	11	I	ST	Timer3 External Gate Input
U1CTS	12	9	8	I	ST	UART1 Clear-to-Send Input
U1RTS	13	10	9	0	_	UART1 Request-to-Send Output
U1RX	6	3	12	I	ST	UART1 Receive
U1TX	11	8	11	0	_	UART1 Transmit
ULPWU	3	1	3	I	ANA	Ultra Low-Power Wake-up Input
Vdd	20	17	14	Р	_	Positive Supply for Peripheral Digital Logic and I/O Pins
VREF+	2	19	2	Ι	ANA	A/D Reference Voltage Input (+)
VREF-	3	20	3	Ι	ANA	A/D Reference Voltage Input (-)
Vss	19	16	13	Р	—	Ground Reference for Logic and I/O Pins

TABLE 1-5: PIC24F16KL20X/10X FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Legend: TTL = TTL input buffer ANA = Analog level input/output ST = Schmitt Trigger input buffer $I^2C = I^2C^{TM}/SMBus$ input buffer

2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS, is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A 0.1 μ F (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- Handling high-frequency noise: If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μ F to 0.001 μ F. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 μ F in parallel with 0.001 μ F).
- Maximizing performance: On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including microcontrollers, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μF to 47 μF .

2.3 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions: Device Reset, and Device Programming and Debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the MCLR pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{\text{MCLR}}$ pin should be placed within 0.25 inch (6 mm) of the pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS





Register(s) Name	Description
W0 through W15	Working Register Array
PC	23-Bit Program Counter
SR	ALU STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
PSVPAG	Program Space Visibility Page Address Register
RCOUNT	REPEAT Loop Counter Register
CORCON	CPU Control Register

3.2 CPU Control Registers

REGISTER 3-1: SR: ALU STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	_		_	_	—	DC
bit 15	·						bit 8
R/W-0 ⁽¹	l) R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2 ⁽²⁾	IPL1 ⁽²⁾	IPL0 ⁽²⁾	RA	Ν	OV	Z	С
bit 7							bit 0
. .							
Legend:			••				
R = Read	able bit	W = Writable b	it	U = Unimplem	nented bit, read		
-n = value	e at POR	" = Bit is set		$0^{\circ} = Bit is clea$	ared	x = Bit is unkn	lown
hit 15_0	Unimplemen	ted: Read as '0'	1				
bit 8	DC: ALU Half	f Carry/Borrow b	it				
	1 = A carry-o	out from the 4 th lo	ow-order bit (f	or byte-sized da	ata) or 8 th low-o	order bit (for wo	ord-sized data)
	of the res	sult occurred		5	,	Υ.	,
	0 = No carry-	out from the 4 th	or 8 th low-ord	ler bit of the res	sult has occurre	ed	
bit 7-5	IPL<2:0>: CF	V Interrupt Prio	rity Level (IPL	.) Status bits ^{(1,2}			
	111 = CPU Ir	terrupt Priority L	_evel is 7 (15) _evel is 6 (14)	; user interrupt	s disabled		
	101 = CPU Ir	nterrupt Priority L	_evel is 5 (14)				
	100 = CPU Ir	nterrupt Priority L	_evel is 4 (12)				
	011 = CPU Ir	nterrupt Priority L	Level is 3 (11)				
	010 = CPU Ir 001 = CPU Ir	nterrupt Priority I	_evel is 2 (10) evel is 1 (9)				
	000 = CPU Ir	nterrupt Priority L	_evel is 0 (8)				
bit 4	RA: REPEAT	Loop Active bit					
	1 = REPEAT	oop in progress					
L :+ 0	0 = REPEAT ION	oop not in progre	ess				
DIL 3	1 = Result wa	live bil s negative					
	0 = Result wa	is non-negative	(zero or positi	ve)			
bit 2	OV: ALU Ove	erflow bit					
	1 = Overflow	occurred for sigi	ned (2's comp	lement) arithm	etic in this arith	metic operatior	า
	0 = No overflo	ow has occurred					
bit 1	Z: ALU Zero I	oit					
	1 = An operat 0 = The most	lion, which effec recent operatio	ts the ∠ bit, ha n, which effec	as set it at some ts the Z bit, has	e time in the pa s cleared it (i.e.	ist , a non-zero re:	sult)
bit 0	C: ALU Carry	/Borrow bit					
	1 = A carry-ou	ut from the Most	Significant bi	t (MSb) of the r	result occurred		
	0 = No carry-	out from the Mos	st Significant I	oit (MSb) of the	e result occurred	d	
Note 1:	The IPL Status bi	ts are read-only	when NSTDI	S (INTCON1<1	5>) = 1.		
2:	The IPL Status bi	ts are concatena	ated with the I	PL3 bit (CORC	ON<3>) to form	n the CPU Inter	rrupt Priority

2: The IPL Status bits are concatenated with the IPL3 bit (CORCON<3>) to form the CPU Interrupt Priority Level (IPL). The value in parentheses indicates the IPL when IPL3 = 1.

REGISTER 8-25: IPC9: INTERRUPT PRIORITY CONTROL REGISTER 9

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
_	—	—	—	—	—	—	—	
bit 15							bit 8	
U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0	
_	T3GIP2	T3GIP1	T3GIP0	—	—	—	—	
bit 7							bit 0	
Legend:								
R = Readable	e bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unknown		
bit 15-7	Unimplemen	ted: Read as '0	כי					
bit 6-4	T3GIP<2:0>:	Timer3 Externa	al Gate Interru	ot Priority bits				
	111 = Interru	pt is Priority 7 (I	highest priority	interrupt)				
	•							

•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3-0 Unimplemented: Read as '0'

REGISTER 8-28: IPC18: INTERRUPT PRIORITY CONTROL REGISTER 18

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—		_	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
_	—	—	—	—	HLVDIP2	HLVDIP1	HLVDIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 Unimplemented: Read as '0'

bit 2-0 HLVDIP<2:0>: High/Low-Voltage Detect Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-29: IPC20: INTERRUPT PRIORITY CONTROL REGISTER 20

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
—	—	—	—	—	—	—	—	
bit 15							bit 8	
U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0	
—	_	_	—		ULPWUIP2	ULPWUIP1	ULPWUIP0	
bit 7							bit 0	
Legend:								
R = Readable	e bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit		'1' = Bit is set		'0' = Bit is clea	'0' = Bit is cleared		x = Bit is unknown	

bit 15-3 Unimplemented: Read as '0'

bit 6-4 ULPWUIP<2:0>: Ultra Low-Power Wake-up Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

.

•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1
ROI	DOZE2	DOZE1	DOZE0	DOZEN ⁽¹⁾	RCDIV2	RCDIV1	RCDIV0
bit 15						·	bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_			_				
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own
bit 15	ROI: Recover	on Interrupt bit	i i				
	1 = Interrupts	clear the DOZ	EN bit, and re	set the CPU an	d peripheral clo	ock ratio to 1:1	
	0 = Interrupts	s have no effect	on the DOZE	N bit			
bit 14-12	DOZE<2:0>:	CPU-to-Periphe	eral Clock Rat	io Select bits			
	111 = 1:128						
	110 = 1:64						
	101 = 1.32 100 = 1.16						
	011 = 1:8						
	010 = 1 :4						
	001 = 1:2						
	000 = 1:1						
bit 11	DOZEN: DOZ	E Enable bit					
	1 = DOZE < 22 0 = CPU and	:U> DITS SPECITY	the CPU-to-pe	eripheral clock r	atio		
bit 10.8		EPC Postscal	ciock ratio are	361 10 1.1			
DIL 10-8	When COSC		N < 14.12 = 11	1 or 0.01:			
	111 = 31.25 k	 <u>Hz</u> (divide-bv-2 	256)	<u> </u>			
	110 = 125 kH	lz (divide-by-64)				
	101 = 250 kH	lz (divide-by-32)				
	100 = 500 kH	lz (divide-by-16)				
	011 = 1 MHz 010 = 2 MHz	(divide-by-6) (divide-by-4)					
	001 = 4 MHz	(divide-by-2) (d	lefault)				
	000 = 8 MHz	(divide-by-1)	-				
	When COSC<	<2:0> (OSCCO	N<14:12>) = 1	.10:			
	111 = 1.95 kH	Hz (divide-by-25	56)				
	110 = 7.81 Km 101 = 15.62 km	12 (divide-by-64 Hz (divide-by-3	+) 32)				
	100 = 31.25 k	Hz (divide-by-1	l6)				
	011 = 62.5 kH	Hz (divide-by-8)					
	010 = 125 kH	lz (divide-by-4)	(- - f ()				
	001 = 250 kH	IZ (alvide-by-2)	(default)				
hit 7-0		ted: Read as 'r)'				
		Logi i logi da l	,				

REGISTER 9-2: CLKDIV: CLOCK DIVIDER REGISTER

Note 1: This bit is automatically cleared when the ROI bit is set and an interrupt occurs.

9.4 Clock Switching Operation

With few limitations, applications are free to switch between any of the four clock sources (POSC, SOSC, FRC and LPRC) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC24F devices have a safeguard lock built into the switching process.

Note: The Primary Oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMDx Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

9.4.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in the FOSC Configuration register must be programmed to '0'. (Refer to **Section 23.0** "**Special Features**" for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and FSCM function are disabled; this is the default setting.

The NOSCx control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSCx bits (OSCCON<14:12>) will reflect the clock source selected by the FNOSCx Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

9.4.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

- 1. If desired, read the COSCx bits (OSCCON<14:12>) to determine the current oscillator source.
- 2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
- 3. Write the appropriate value to the NOSCx bits (OSCCON<10:8>) for the new oscillator source.
- 4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
- 5. Set the OSWEN bit to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically, as follows:

- 1. The clock switching hardware compares the COSCx bits with the new value of the NOSCx bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
- If a valid clock switch has been initiated, the LOCK (OSCCON<5>) and CF (OSCCON<3>) bits are cleared.
- The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware will wait until the OST expires. If the new source is using the PLL, then the hardware waits until a PLL lock is detected (LOCK = 1).
- 4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
- 5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSCx bits value is transferred to the COSCx bits.
- The old clock source is turned off at this time, with the exception of LPRC (if WDT or FSCM, with LPRC as a clock source, are enabled) or SOSC (if SOSCEN remains enabled).

Note 1: The processor will continue to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.

2: Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes. The following code sequence for a clock switch is recommended:

- 1. Disable interrupts during the OSCCON register unlock and write sequence.
- Execute the unlock sequence for the OSCCON high byte by writing 78h and 9Ah to OSCCON<15:8>, in two back-to-back instructions.
- 3. Write the new oscillator source to the NOSCx bits in the instruction immediately following the unlock sequence.
- Execute the unlock sequence for the OSCCON low byte by writing 46h and 57h to OSCCON<7:0>, in two back-to-back instructions.
- 5. Set the OSWEN bit in the instruction immediately following the unlock sequence.
- 6. Continue to execute code that is not clock-sensitive (optional).
- 7. Invoke an appropriate amount of software delay (cycle counting) to allow the selected oscillator and/or PLL to start and stabilize.
- 8. Check to see if OSWEN is '0'. If it is, the switch was successful. If OSWEN is still set, then check the LOCK bit to determine the cause of failure.

The core sequence for unlocking the OSCCON register and initiating a clock switch is shown in Example 9-1.

EXAMPLE 9-1: BASIC CODE SEQUENCE FOR CLOCK SWITCHING

;Place the new oscillator selection in WO
;OSCCONH (high byte) Unlock Sequence
MOV #OSCCONH, w1
MOV #0x78, w2
MOV #0x9A, w3
MOV.b w2, [w1]
MOV.b w3, [w1]
;Set new oscillator selection
MOV.b WREG, OSCCONH
;OSCCONL (low byte) unlock sequence
MOV #OSCCONL, w1
MOV #0x46, w2
MOV #0x57, w3
MOV.b w2, [w1]
MOV.b w3, [w1]
;Start oscillator switch operation
BSET OSCCON, #0

9.5 Reference Clock Output

In addition to the CLKO output (Fosc/2) available in certain oscillator modes, the device clock in the PIC24F16KL402 family devices can also be configured to provide a reference clock output signal to a port pin. This feature is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application.

This reference clock output is controlled by the REFOCON register (Register 9-4). Setting the ROEN bit (REFOCON<15>) makes the clock signal available on the REFO pin. The RODIV bits (REFOCON<11:8>) enable the selection of 16 different clock divider options.

The ROSSLP and ROSEL bits (REFOCON<13:12>) control the availability of the reference output during Sleep mode. The ROSEL bit determines if the oscillator on OSC1 and OSC2, or the current system clock source, is used for the reference clock output. The ROSSLP bit determines if the reference source is available on REFO when the device is in Sleep mode.

To use the reference clock output in Sleep mode, both the ROSSLP and ROSEL bits must be set. The device clock must also be configured for one of the primary modes (EC, HS or XT). Therefore, if the ROSEL bit is also not set, the oscillator on OSC1 and OSC2 will be powered down when the device enters Sleep mode. Clearing the ROSEL bit allows the reference output frequency to change as the system clock changes during any clock switches.

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0		
ULPEN	—	ULPSIDL	_	—	—	—	ULPSINK		
bit 15							bit 8		
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
_	—	—		—	—	_	—		
bit 7							bit 0		
Legend:									
R = Readab	le bit	W = Writable I	oit	U = Unimplemented bit, read as '0'					
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown			
bit 15	ULPEN: ULF	PWU Module En	able bit						
	1 = Module i	s enabled							
	0 = Module I	s disabled							
bit 14	Unimpleme	nted: Read as '0)'						
bit 13	ULPSIDL: U	ILPWU Stop in Ic	le Select bit						
	1 = Discontir	nues module ope	eration when t	the device enter	rs Idle mode				
	0 = Continue	es module opera	tion in Idle mo	ode					
bit 12-9	Unimpleme	nted: Read as '0)'						
bit 8	ULPSINK: L	JLPWU Current	Sink Enable b	oit					
	1 = Current	sink is enabled							
	0 = Current	sink is disabled							
bit 7-0	Unimpleme	nted: Read as '0)'						

REGISTER 10-1: ULPWCON: ULPWU CONTROL REGISTER

10.4 Doze Mode

Generally, changing clock speed and invoking one of the power-saving modes are the preferred strategies for reducing power consumption. There may be circumstances, however, where this is not practical. For example, it may be necessary for an application to maintain uninterrupted, synchronous communication, even while it is doing nothing else. Reducing system clock speed may introduce communication errors, while using a power-saving mode may stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default.

It is also possible to use Doze mode to selectively reduce power consumption in event driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption. Meanwhile, the CPU Idles, waiting for something to invoke an interrupt routine. Enabling the automatic return to full-speed CPU operation on interrupts is enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

10.5 Selective Peripheral Module Control

Idle and Doze modes allow users to substantially reduce power consumption by slowing or stopping the CPU clock. Even so, peripheral modules still remain clocked and thus, consume power. There may be cases where the application needs what these modes do not provide: the allocation of power resources to CPU processing, with minimal power consumption from the peripherals.

PIC24F devices address this requirement by allowing peripheral modules to be selectively disabled, reducing or eliminating their power consumption. This can be done with two control bits:

- The Peripheral Enable bit, generically named, "XXXEN", located in the module's main control SFR.
- The Peripheral Module Disable (PMD) bit, generically named, "XXXMD", located in one of the PMD Control registers.

Both bits have similar functions in enabling or disabling its associated module. Setting the PMD bit for a module disables all clock sources to that module, reducing its power consumption to an absolute minimum. In this state, the control and status registers associated with the peripheral will also be disabled, so writes to those registers will have no effect, and read values will be invalid. Many peripheral modules have a corresponding PMD bit.

In contrast, disabling a module by clearing its XXXEN bit, disables its functionality, but leaves its registers available to be read and written to. Power consumption is reduced, but not by as much as when the PMD bits are used.

To achieve more selective power savings, peripheral modules can also be selectively disabled when the device enters Idle mode. This is done through the control bit of the generic name format, "XXXIDL". By default, all modules that can operate during Idle mode will do so. Using the disable on Idle feature disables the module while in Idle mode, allowing further reduction of power consumption during Idle mode. This enhances power savings for extremely critical power applications.

12.0 TIMER1

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Timers, refer to the "dsPIC33/PIC24 Family Reference Manual", "Timers" (DS39704).

The Timer1 module is a 16-bit timer which can operate as a free-running, interval timer/counter, or serve as the time counter for a software-based Real-Time Clock (RTC). Timer1 is only reset on initial VDD power-on events. This allows the timer to continue operating as an RTC clock source through other types of device Reset.

Timer1 can operate in three modes:

- 16-Bit Timer
- 16-Bit Synchronous Counter
- 16-Bit Asynchronous Counter

Timer1 also supports these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation During CPU Idle and Sleep modes
- Interrupt on 16-Bit Period Register Match or Falling Edge of External Gate Signal

Figure 12-1 illustrates a block diagram of the 16-bit Timer1 module.

To configure Timer1 for operation:

- 1. Set the TON bit (= 1).
- 2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
- 3. Set the Clock and Gating modes using the TCS and TGATE bits.
- 4. Set or clear the TSYNC bit to configure synchronous or asynchronous operation.
- 5. Load the timer period value into the PR1 register.
- 6. If interrupts are required, set the Timer1 Interrupt Enable bit, T1IE. Use the Timer1 Interrupt Priority bits, T1IP<2:0>, to set the interrupt priority.



NOTES:





Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
ADD	ADD	f	f = f + WREG	1	1	C, DC, N, OV, Z
	ADD	f,WREG	WREG = f + WREG	1	1	C, DC, N, OV, Z
	ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C, DC, N, OV, Z
	ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C, DC, N, OV, Z
	ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C, DC, N, OV, Z
ADDC	ADDC	f	f = f + WREG + (C)	1	1	C, DC, N, OV, Z
	ADDC	f,WREG	WREG = f + WREG + (C)	1	1	C, DC, N, OV, Z
	ADDC	#lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C, DC, N, OV, Z
	ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C, DC, N, OV, Z
	ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C, DC, N, OV, Z
AND	AND	f	f = f .AND. WREG	1	1	N, Z
	AND	f,WREG	WREG = f .AND. WREG	1	1	N, Z
	AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N, Z
	AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N, Z
	AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N, Z
ASR	ASR	£	f = Arithmetic Right Shift f	1	1	C, N, OV, Z
	ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C, N, OV, Z
	ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C, N, OV, Z
	ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N, Z
	ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N, Z
BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
	BCLR	Ws,#bit4	Bit Clear Ws	1	1	None
BRA	BRA	C,Expr	Branch if Carry	1	1 (2)	None
	BRA	GE, Expr	Branch if Greater than or Equal	1	1 (2)	None
	BRA	GEU, Expr	Branch if Unsigned Greater than or Equal	1	1 (2)	None
	BRA	GT, Expr	Branch if Greater than	1	1 (2)	None
	BRA	GTU, Expr	Branch if Unsigned Greater than	1	1 (2)	None
	BRA	LE, Expr	Branch if Less than or Equal	1	1 (2)	None
	BRA	LEU, Expr	Branch if Unsigned Less than or Equal	1	1 (2)	None
	BRA	LT, Expr	Branch if Less than	1	1 (2)	None
	BRA	LTU, Expr	Branch if Unsigned Less than	1	1 (2)	None
	BRA	N,Expr	Branch if Negative	1	1 (2)	None
	BRA	NC,Expr	Branch if Not Carry	1	1 (2)	None
	BRA	NN, Expr	Branch if Not Negative	1	1 (2)	None
	BRA	NOV,Expr	Branch if Not Overflow	1	1 (2)	None
	BRA	NZ,Expr	Branch if Not Zero	1	1 (2)	None
	BRA	OV,Expr	Branch if Overflow	1	1 (2)	None
	BRA	Expr	Branch Unconditionally	1	2	None
	BRA	Z,Expr	Branch if Zero	1	1 (2)	None
	BRA	Wn	Computed Branch	1	2	None
BSET	BSET	f,#bit4	Bit Set f	1	1	None
	BSET	Ws,#bit4	Bit Set Ws	1	1	None
BSW	BSW.C	Ws,Wb	Write C bit to Ws <wb></wb>	1	1	None
	BSW.Z	Ws,Wb	Write Z bit to Ws <wb></wb>	1	1	None
BTG	BTG	f,#bit4	Bit Toggle f	1	1	None
	BTG	Ws,#bit4	Bit Toggle Ws	1	1	None
BTSC	BTSC	f,#bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
	BTSC	Ws,#bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None

TABLE 25-2:	INSTRUCTION SET	OVERVIEW

TABLE 26-1: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Тур	Max	Unit
Operating Junction Temperature Range	TJ	-40	_	+140	°C
Operating Ambient Temperature Range	TA	-40		+125	°C
$\begin{array}{l} \mbox{Power Dissipation:} \\ \mbox{Internal Chip Power Dissipation:} \\ \mbox{PINT} = V \mbox{DD } x \ (\mbox{IDD} - \Sigma \ \mbox{IOH}) \\ \mbox{I/O Pin Power Dissipation:} \\ \mbox{PI/O} = \Sigma \ (\{\mbox{VDD} - \mbox{VOH}\} \ x \ \mbox{IOH}) + \Sigma \ (\mbox{VOL } x \ \mbox{IOL}) \end{array}$	PD		Pint + Pi/c)	W
Maximum Allowed Power Dissipation	PDMAX	((TJ – TA)/θJA		

TABLE 26-2: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Тур	Max	Unit	Notes
Package Thermal Resistance, 20-Pin PDIP	θJA	62.4		°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θJA	60	—	°C/W	1
Package Thermal Resistance, 20-Pin SSOP	θJA	108	—	°C/W	1
Package Thermal Resistance, 28-Pin SSOP	θJA	71	—	°C/W	1
Package Thermal Resistance, 20-Pin SOIC	θJA	75	—	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θJA	80.2	—	°C/W	1
Package Thermal Resistance, 20-Pin QFN	θJA	43	—	°C/W	1
Package Thermal Resistance, 28-Pin QFN	θJA	32	—	°C/W	1
Package Thermal Resistance, 14-Pin PDIP	θJA	62.4	—	°C/W	1
Package Thermal Resistance, 14-Pin TSSOP	θJA	108	_	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ JA) numbers are achieved by package simulations.

TABLE 26-3: DC CHARACTERISTICS: TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS								
Para m No.	Symbol	Characteristic	Min Typ ⁽¹⁾ Max Units Conditions					
DC10	Vdd	Supply Voltage	1.8		3.6	V		
DC12	Vdr	RAM Data Retention Voltage ⁽²⁾	1.5	-	_	V		
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	Vss	_	0.7	V		
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	0-3.3V in 0.1s 0-2.5V in 60 ms	
	Vbg	Band Gap Voltage Reference	1.14	1.2	1.26	V		

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This is the limit to which VDD can be lowered without losing RAM data.





TABLE 26-18: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions	
OS10	Fosc	External CLKI Frequency (External clocks allowed only in EC mode)	DC 4	_	32 8	MHz MHz	EC ECPLL	
		Oscillator Frequency	0.2 4 4 31		4 25 8 33	MHz MHz MHz kHz	XT HS HSPLL SOSC	
OS20	Tosc	Tosc = 1/Fosc	—	—		—	See Parameter OS10 for Fosc value	
OS25	Тсү	Instruction Cycle Time ⁽²⁾	62.5	—	DC	ns		
OS30	TosL, TosH	External Clock in (OSCI) High or Low Time	0.45 x Tosc	_		ns	EC	
OS31	TosR, TosF	External Clock in (OSCI) Rise or Fall Time	—	_	20	ns	EC	
OS40	TckR	CLKO Rise Time ⁽³⁾	—	6	10	ns		
OS41	TckF	CLKO Fall Time ⁽³⁾	_	6	10	ns		

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Min." values with an external clock applied to the OSCI/CLKI pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSCO pin. CLKO is low for the Q1-Q2 period (1/2 TCY) and high for the Q3-Q4 period (1/2 TCY).

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Microchip Technology Drawing C04-087C Sheet 1 of 2

Worldwide Sales and Service

AMERICAS

Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: http://www.microchip.com/ support Web Address: www.microchip.com

Atlanta Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455

Austin, TX Tel: 512-257-3370

Boston Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088

Chicago Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075

Cleveland Independence, OH Tel: 216-447-0464 Fax: 216-447-0643

Dallas Addison, TX Tel: 972-818-7423 Fax: 972-818-2924

Detroit Novi, MI Tel: 248-848-4000

Houston, TX Tel: 281-894-5983

Indianapolis Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453

Los Angeles Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608

New York, NY Tel: 631-435-6000

San Jose, CA Tel: 408-735-9110

Canada - Toronto Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office Suites 3707-14, 37th Floor Tower 6, The Gateway Harbour City, Kowloon Hong Kong Tel: 852-2401-1200 Fax: 852-2401-3431 Australia - Sydney

Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing Tel: 86-10-8569-7000 Fax: 86-10-8528-2104

China - Chengdu Tel: 86-28-8665-5511 Fax: 86-28-8665-7889

China - Chongqing Tel: 86-23-8980-9588 Fax: 86-23-8980-9500

China - Hangzhou Tel: 86-571-2819-3187 Fax: 86-571-2819-3189

China - Hong Kong SAR

Tel: 852-2943-5100 Fax: 852-2401-3431

China - Nanjing Tel: 86-25-8473-2460

Fax: 86-25-8473-2470 China - Qingdao Tel: 86-532-8502-7355 Fax: 86-532-8502-7205

China - Shanghai Tel: 86-21-5407-5533 Fax: 86-21-5407-5066

China - Shenyang Tel: 86-24-2334-2829 Fax: 86-24-2334-2393

China - Shenzhen Tel: 86-755-8864-2200 Fax: 86-755-8203-1760

China - Wuhan Tel: 86-27-5980-5300 Fax: 86-27-5980-5118

China - Xian Tel: 86-29-8833-7252 Fax: 86-29-8833-7256

China - Xiamen Tel: 86-592-2388138 Fax: 86-592-2388130

China - Zhuhai Tel: 86-756-3210040 Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore Tel: 91-80-3090-4444 Fax: 91-80-3090-4123

India - New Delhi Tel: 91-11-4160-8631 Fax: 91-11-4160-8632

India - Pune Tel: 91-20-3019-1500

Japan - Osaka Tel: 81-6-6152-7160 Fax: 81-6-6152-9310

Japan - Tokyo Tel: 81-3-6880- 3770 Fax: 81-3-6880-3771

Korea - Daegu Tel: 82-53-744-4301 Fax: 82-53-744-4302

Korea - Seoul Tel: 82-2-554-7200 Fax: 82-2-558-5932 or 82-2-558-5934

Malaysia - Kuala Lumpur Tel: 60-3-6201-9857 Fax: 60-3-6201-9859

Malaysia - Penang Tel: 60-4-227-8870 Fax: 60-4-227-4068

Philippines - Manila Tel: 63-2-634-9065 Fax: 63-2-634-9069

Singapore Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan - Hsin Chu Tel: 886-3-5778-366 Fax: 886-3-5770-955

Taiwan - Kaohsiung Tel: 886-7-213-7830

Taiwan - Taipei Tel: 886-2-2508-8600 Fax: 886-2-2508-0102

Thailand - Bangkok Tel: 66-2-694-1351 Fax: 66-2-694-1350

EUROPE

Austria - Wels Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 Denmark - Copenhagen Tel: 45-4450-2828 Fax: 45-4485-2829

France - Paris Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany - Dusseldorf Tel: 49-2129-3766400

Germany - Munich Tel: 49-89-627-144-0 Fax: 49-89-627-144-44

Germany - Pforzheim Tel: 49-7231-424750

Italy - Milan Tel: 39-0331-742611 Fax: 39-0331-466781

Italy - Venice Tel: 39-049-7625286

Netherlands - Drunen Tel: 31-416-690399 Fax: 31-416-690340

Poland - Warsaw Tel: 48-22-3325737

Spain - Madrid Tel: 34-91-708-08-90 Fax: 34-91-708-08-91

Sweden - Stockholm Tel: 46-8-5090-4654

UK - Wokingham Tel: 44-118-921-5800 Fax: 44-118-921-5820

10/28/13