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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XF

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VQFN Exposed Pad
Supplier Device Package	20-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f08kl201t-i-mq

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Analog Features:

- 10-Bit, up to 12-Channel Analog-to-Digital (A/D) Converter:
 - 500 ksps conversion rate
 - Conversion available during Sleep and Idle
- Dual Rail-to-Rail Analog Comparators with Programmable Input/Output Configuration
- On-Chip Voltage Reference

Special Microcontroller Features:

- Operating Voltage Range of 1.8V to 3.6V
- 10,000 Erase/Write Cycle Endurance Flash Program Memory, Typical
- 100,000 Erase/Write Cycle Endurance Data EEPROM, Typical
- Flash and Data EEPROM Data Retention: 40 Years Minimum
- Self-Programmable under Software Control
- Programmable Reference Clock Output

- Fail-Safe Clock Monitor (FSCM) Operation:
 - Detects clock failure and switches to on-chip, Low-Power RC (LPRC) oscillator
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Flexible Watchdog Timer (WDT):
 - Uses its own Low-Power RC oscillator
 - Windowed operating modes
 - Programmable period of 2 ms to 131s
- In-Circuit Serial Programming[™] (ICSP[™]) and In-Circuit Emulation (ICE) via 2 Pins
- Programmable High/Low-Voltage Detect (HLVD)
- Programmable Brown-out Reset (BOR):
 - Configurable for software controlled operation and shutdown in Sleep mode
 - Selectable trip points (1.8V, 2.7V and 3.0V)
 - Low-power 2.0V POR re-arm

		Pin N	umber				
Function	20-Pin PDIP/ SSOP/ SOIC	20-Pin QFN	28-Pin SPDIP/ SSOP/ SOIC	28-Pin QFN	I/O	Buffer	Description
CN0	10	7	12	9	Ι	ST	Interrupt-on-Change Inputs
CN1	9	6	11	8	Ι	ST	
CN2	2	19	2	27	Ι	ST	
CN3	3	20	3	28	I	ST	
CN4	4	1	4	1	I	ST	
CN5	5	2	5	2	I	ST	
CN6	6	3	6	3	I	ST	
CN7	_	—	7	4	I	ST	
CN8	14	11	20	17	I	ST	
CN9	—	_	19	16	Ι	ST	
CN11	18	15	26	23	I	ST	
CN12	17	14	25	22	I	ST	
CN13	16	13	24	21	Ι	ST	
CN14	15	12	23	20	Ι	ST	
CN15	_	_	22	19	Ι	ST	
CN16	_	_	21	18	I	ST	
CN21	13	10	18	15	Ι	ST	
CN22	12	9	17	14	Ι	ST	
CN23	11	8	16	13	Ι	ST	
CN24	_	—	15	12	I	ST	
CN27	_	—	14	11	I	ST	
CN29	8	5	10	7	I	ST	
CN30	7	4	9	6	I	ST	
CVREF	17	14	25	22	I	ANA	Comparator Voltage Reference Output
CVREF+	2	19	2	27	I	ANA	Comparator Reference Positive Input Voltage
CVREF-	3	20	3	28	I	ANA	Comparator Reference Negative Input Voltage
FLT0	17	14	25	22	I	ST	ECCP1 Enhanced PWM Fault Input
HLVDIN	15	12	23	20	I	ST	High/Low-Voltage Detect Input
INT0	11	8	16	13	I	ST	Interrupt 0 Input
INT1	17	14	25	22	I	ST	Interrupt 1 Input
INT2	14	11	20	17	I	ST	Interrupt 2 Input
MCLR	1	18	1	26	I	ST	Master Clear (device Reset) Input. This line is brought low to cause a Reset.
OSCI	7	4	9	6	Ι	ANA	Main Oscillator Input
OSCO	8	5	10	7	0	ANA	Main Oscillator Output
P1A	14	11	20	17	0	_	ECCP1 Output A (Enhanced PWM Mode)
P1B	5	2	21	18	0	—	ECCP1 Output B (Enhanced PWM Mode)
P1C	4	1	22	19	0	—	ECCP1 Output C (Enhanced PWM Mode)
P1D	16	13	18	15	0	_	ECCP1 Output D (Enhanced PWM Mode)

TABLE 1-4:	PIC24F16KL40X/30X FAMILY PINOUT DESCRIPTIONS ((CONTINUED)

Legend:

TTL = TTL input buffer

ANA = Analog level input/output

ST = Schmitt Trigger input buffer $I^2C = I^2C^{TM}/SMBus$ input buffer

		Pin Number	,			
Function	20-Pin PDIP/ SSOP/ SOIC	20-Pin QFN	14-Pin PDIP/ TSSOP	I/O	Buffer	Description
CVREF	17	14	11	I	ANA	Comparator Voltage Reference Output
CVREF+	2	19	2	I	ANA	Comparator Reference Positive Input Voltage
CVREF-	3	20	3	I	ANA	Comparator Reference Negative Input Voltage
HLVDIN	15	12	6	I	ST	High/Low-Voltage Detect Input
INT0	11	8	12	I	ST	Interrupt 0 Input
INT1	17	14	11	I	ST	Interrupt 1 Input
INT2	14	11	10	I	ST	Interrupt 2 Input
MCLR	1	18	1	Ι	ST	Master Clear (device Reset) Input. This line is brought low to cause a Reset.
OSCI	7	4	4	I	ANA	Main Oscillator Input
OSCO	8	5	5	0	ANA	Main Oscillator Output
PGEC1	5	2		I/O	ST	ICSP™ Clock 1
PCED1	4	1	_	I/O	ST	ICSP Data 1
PGEC2	2	19	2	I/O	ST	ICSP Clock 2
PGED2	3	20	3	I/O	ST	ICSP Data 2
PGEC3	10	7	7	I/O	ST	ICSP Clock 3
PGED3	9	6	6	I/O	ST	ICSP Data 3
RA0	2	19	2	I/O	ST	PORTA Pins
RA1	3	20	3	I/O	ST	
RA2	7	4	4	I/O	ST	
RA3	8	5	5	I/O	ST	
RA4	10	7	7	I/O	ST	
RA5	1	18	1	Ι	ST	
RA6	14	11	10	I/O	ST	
RB0	4	1	_	I/O	ST	PORTB Pins
RB1	5	2	_	I/O	ST	
RB2	6	3	—	I/O	ST	
RB4	9	6	6	I/O	ST	
RB7	11	8	_	I/O	ST	
RB8	12	9	8	I/O	ST	
RB9	13	10	9	I/O	ST	
RB12	15	12	—	I/O	ST	
RB13	16	13	—	I/O	ST	
RB14	17	14	11	I/O	ST	
RB15	18	15	12	I/O	ST	
REFO	18	15	12	0	—	Reference Clock Output

PIC24F16KL20X/10X FAMILY PINOUT DESCRIPTIONS (CONTINUED) **TABLE 1-5:**

Legend: TTL = TTL input buffer ANA = Analog level input/output ST = Schmitt Trigger input buffer $I^2C = I^2C^{TM}/SMBus$ input buffer

3.0 CPU

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the CPU, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"CPU"** (DS39703).

The PIC24F CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set and a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M instructions of user program memory space. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction and the table instructions. Overhead-free program loop constructs are supported using the REPEAT instructions, which are interruptible at any point.

PIC24F devices have sixteen, 16-bit Working registers in the programmer's model. Each of the Working registers can act as a data, address or address offset register. The 16th Working register (W15) operates as a Software Stack Pointer (SSP) for interrupts and calls.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K word boundary of either program memory or data EEPROM memory, defined by the 8-bit Program Space Visibility Page Address (PSVPAG) register. The program to data space mapping feature lets any instruction access program space as if it were data space.

The Instruction Set Architecture (ISA) has been significantly enhanced beyond that of the PIC18, but maintains an acceptable level of backward compatibility. All PIC18 instructions and addressing modes are supported, either directly, or through simple macros. Many of the ISA enhancements have been driven by compiler efficiency needs.

The core supports Inherent (no operand), Relative, Literal, Memory Direct and three groups of addressing modes. All modes support Register Direct and various Register Indirect modes. Each group offers up to seven addressing modes. Instructions are associated with predefined addressing modes depending upon their functional requirements. For most instructions, the core is capable of executing a data (or program data) memory read, a Working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing trinary operations (i.e., A + B = C) to be executed in a single cycle.

A high-speed, 17-bit by 17-bit multiplier has been included to significantly enhance the core arithmetic capability and throughput. The multiplier supports Signed, Unsigned and Mixed mode, 16-bit by 16-bit or 8-bit by 8-bit integer multiplication. All multiply instructions execute in a single cycle.

The 16-bit ALU has been enhanced with integer divide assist hardware that supports an iterative non-restoring divide algorithm. It operates in conjunction with the REPEAT instruction looping mechanism and a selection of iterative divide instructions to support 32-bit (or 16-bit), divided by a 16-bit integer signed and unsigned division. All divide operations require 19 cycles to complete, but are interruptible at any cycle boundary.

The PIC24F has a vectored exception scheme, with up to eight sources of non-maskable traps and up to 118 interrupt sources. Each interrupt source can be assigned to one of seven priority levels.

A block diagram of the CPU is illustrated in Figure 3-1.

3.1 Programmer's Model

Figure 3-2 displays the programmer's model for the PIC24F. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions.

Table 3-1 provides a description of each register. All registers associated with the programmer's model are memory mapped.

7.4.2 DETECTING BOR

When BOR is enabled, the BOR bit (RCON<1>) is always reset to '1' on any BOR or POR event. This makes it difficult to determine if a BOR event has occurred just by reading the state of BOR alone. A more reliable method is to simultaneously check the state of both POR and BOR. This assumes that the POR and BOR bits are reset to '0' in the software, immediately after any POR event. If the BOR bit is '1' while POR is '0', it can be reliably assumed that a BOR event has occurred.

Note: Even when the device exits from Deep Sleep mode, both the POR and BOR are set.

7.4.3 DISABLING BOR IN SLEEP MODE

When BOREN<1:0> = 10, BOR remains under hardware control and operates as previously described. However, whenever the device enters Sleep mode, BOR is automatically disabled. When the device returns to any other operating mode, BOR is automatically re-enabled.

This mode allows for applications to recover from brown-out situations, while actively executing code when the device requires BOR protection the most. At the same time, it saves additional power in Sleep mode by eliminating the small incremental BOR current.

R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	U-0
U2TXIF ⁽	¹⁾ U2RXIF ⁽¹⁾	INT2IF	—	T4IF ⁽¹⁾	—	CCP3IF ⁽¹⁾	
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INT1IF	CNIF	CMIF	BCL1IF	SSP1IF
bit 7							bit 0
Lenend							
Legena:	able bit	M - Mritabla	~i+		controd hit roa	d oo 'O'	
		vv = vvritable i	JIL	0' = 0	nenteu bit, rea	u as u v = Bit is unkny	own
	alFOR				areu		JW11
bit 15		T2 Transmitter	Interrunt Elag	Status hit(1)			
bit 15	1 = Interrupt r	request has occ	urred	Status bit			
	0 = Interrupt r	equest has not	occurred				
bit 14	U2RXIF: UAF	RT2 Receiver In	terrupt Flag S	tatus bit ⁽¹⁾			
	1 = Interrupt r	equest has occ	urred				
	0 = Interrupt r	equest has not	occurred				
bit 13	INT2IF: Exter	nal Interrupt 2 I	-lag Status bit				
	1 = Interrupt r	equest has occ	urred				
h:+ 40		request has not	occurrea				
DIL 12 bit 11		ted: Read as () Status hit(1)				
	1 = Interrupt r	equest has occ					
	0 = Interrupt r	request has not	occurred				
bit 10	Unimplemen	ted: Read as '0)'				
bit 9	CCP3IF: Cap	ture/Compare/F	PWM3 Interrup	ot Flag Status b	it ⁽¹⁾		
	1 = Interrupt r	equest has occ	urred				
	0 = Interrupt r	equest has not	occurred				
bit 8-5	Unimplemen	ted: Read as '0)'				
bit 4	INT1IF: Exter	nal Interrupt 1 I	-lag Status bit				
	1 = Interrupt r	request has occ	urred				
hit 3	CNIE: Input C	equest has not		lag Status bit			
DIL 3	1 = Interrupt r		urred	ay Status bit			
	0 = Interrupt r	request has not	occurred				
bit 2	CMIF: Compa	arator Interrupt	Flag Status bit	t			
	1 = Interrupt r	equest has occ	urred				
	0 = Interrupt r	request has not	occurred				
bit 1	BCL1IF: MSS	SP1 I ² C™ Bus (Collision Interr	upt Flag Status	bit		
	1 = Interrupt r	equest has occ	urred				
	0 = Interrupt r	request has not	occurred				
dit U	SSP1IF: MSS	SP1 SPI/IC Eve	ent Interrupt F	lag Status bit			
	\perp = interrupt r	equest has occ					
			Coouricu				
Note 1:	These bits are un	implemented or	n PIC24FXXK	L10X and PIC2	4FXXKL20X d	levices.	

REGISTER 8-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1

REGISTER 8-28: IPC18: INTERRUPT PRIORITY CONTROL REGISTER 18

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—		_	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
_	—	—	—	—	HLVDIP2	HLVDIP1	HLVDIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 Unimplemented: Read as '0'

bit 2-0 HLVDIP<2:0>: High/Low-Voltage Detect Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-29: IPC20: INTERRUPT PRIORITY CONTROL REGISTER 20

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
—	—	—	—	—	—	—	—	
bit 15							bit 8	
U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0	
—	_	_	—		ULPWUIP2	ULPWUIP1	ULPWUIP0	
bit 7							bit 0	
Legend:								
R = Readable	e bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set				'0' = Bit is cleared x = Bit is unknown				

bit 15-3 Unimplemented: Read as '0'

bit 6-4 ULPWUIP<2:0>: Ultra Low-Power Wake-up Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

.

•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

NOTES:

REGISTER 11-1: ANSA: PORTA ANALOG SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	_	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	—	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:

bit 3-0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 Unimplemented: Read as '0'

ANSA<3:0>: Analog Select Control bits

1 = Digital input buffer is not active (use for analog input)

0 = Digital input buffer is active

REGISTER 11-2: ANSB: PORTB ANALOG SELECTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	U-0	U-0	U-0	U-0
ANSB15	ANSB14	ANSB13 ⁽¹⁾	ANSB12 ⁽¹⁾	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	—	—	ANSB4	ANSB3 ⁽²⁾	ANSB2 ⁽¹⁾	ANSB1 ⁽¹⁾	ANSB0 ⁽¹⁾
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12	ANSB<15:12>: Analog Select Control bits ⁽¹⁾ 1 = Digital input buffer is not active (use for analog input) 0 = Digital input buffer is active
bit 11-5	Unimplemented: Read as '0'
bit 4-0	ANSB<4:0>: Analog Select Control bits ⁽²⁾ 1 = Digital input buffer is not active (use for analog input) 0 = Digital input buffer is active

Note 1: ANSB<13:12,2:0> are unimplemented on 14-pin devices.

2: ANSB<3> is unimplemented on 14-pin and 20-pin devices.

ΠU	11_0	11_0	11_0	11_0	11_0	11_0	LL_Ω
0-0	0-0	0-0	0-0	0-0	0-0	0-0	0-0
							hit
							Dit
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0
oit 7		•	•		•	•	bit
.egend:							
२ = Readab	le bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'	
n = Value a	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 7 bit 6-4	ECCPASE: E 1 = A shutdow 0 = ECCP out ECCPAS<2:0 111 = VIL on 110 = VIL on 101 = VIL on 100 = VIL on	CCP1 Auto-Sh vn event has or tputs are opera >: ECCP1 Auto FLT0 pin, or eit FLT0 pin or C2 FLT0 pin or C1 FLT0 pin	utdown Event ccurred; ECCP ting o-Shutdown So her C1OUT or OUT comparat OUT comparat	Status bit outputs are in ource Select bit C2OUT is high or output is hig or output is hig	a shutdown sta s h h	ate	
	011 = Either (010 = C2OUT 001 = C1OUT 000 = Auto-sh	C1OUT or C2C Γ comparator o Γ comparator o nutdown is disa	utput is high utput is high utput is high bled				
oit 3-2	PSSAC<1:0>: P1A and P1C Pins Shutdown State Control bits 1x = P1A and P1C pins tri-state 01 = Drive pins, P1A and P1C, to '1' 00 = Drive pins, P1A and P1C, to '0'						
oit 1-0	PSSBD<1:0> 1x = P1B and 01 = Drive pir 00 = Drive pir	: P1B and P1D I P1D pins tri-st ns, P1B and P1 ns, P1B and P1	Pins Shutdow ate D, to '1' D, to '0'	n State Control	bits		

Note 1: The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level is present, the auto-shutdown will persist.

2: Writing to the ECCPASE bit is disabled while an auto-shutdown condition persists.

3: Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart), the PWM signal will always restart at the beginning of the next PWM period.

REGISTER 18-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0, HSC	R-1, HSC	
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	
bit 15 bit 8								

R/W-0	R/W-0	R/W-0	R-1, HSC	R-0, HSC	R-0, HSC	R/C-0, HS	R-0, HSC	
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	
bit 7 bit 0								

Legend:	HC = Hardware Clearable bit			
HS = Hardware Settable bit C = Clearable bit		HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit U = Unimplemented bit, rea		as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15,13 UTXISEL<1:0>: UARTx Transmission Interrupt Mode Selection bits

- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14	UTXINV:	IrDA [®] Encoder	Transmit	Polarity	Inversion	bit
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Dit i i	
	<u>If IREN = 0:</u>
	1 = UxTX Idle '0'
	0 = UxTX Idle '1'
	<u>If IREN = 1:</u>
	1 = UxTX Idle '1'
	0 = UxTX Idle '0'
bit 12	Unimplemented: Read as '0'
bit 11	UTXBRK: UARTx Transmit Break bit
	1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits; followed by Stop bit; cleared by hardware upon completion
	0 = Sync Break transmission is disabled or completed
bit 10	UTXEN: UARTx Transmit Enable bit
	 1 = Transmit is enabled; UxTX pin is controlled by UARTx
	0 = Transmit is disabled; any pending transmission is aborted and the buffer is reset. UxTX pin is controlled by the PORT register.
bit 9	UTXBF: UARTx Transmit Buffer Full Status bit (read-only)
	1 = Transmit buffer is full
	0 = Transmit buffer is not full, at least one more character can be written
bit 8	TRMT: Transmit Shift Register Empty bit (read-only)
	1 = Transmit Shift Register is empty and the transmit buffer is empty (the last transmission has completed)
	0 = Transmit Shift Register is not empty; a transmission is in progress or queued
bit 7-6	URXISEL<1:0>: UARTx Receive Interrupt Mode Selection bits
	 11 = Interrupt is set on the RSR transfer, making the receive buffer full (i.e., has 2 data characters) 10 = Reserved 01 = Reserved

00 = Interrupt is set when any character is received and transferred from the RSR to the receive buffer; receive buffer has one or more characters

REGISTER 21-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

bit 8 W-0 /R0 bit 0						
bit 8 W-0 VR0 bit 0						
W-0 √R0 bit 0						
W-0 √R0 bit 0						
VR0 bit 0						
bit 0						
t POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknownUnimplemented: Read as '0'CVREN: Comparator Voltage Reference Enable bit1 = CVREF circuit is powered on0 = CVREF circuit is powered downCVROE: Comparator VREF Output Enable bit1 = CVREF voltage level is output on the CVREF pin0 = CVREF voltage level is disconnected from the CVREF pin0 = CVRSS: Comparator VREF Source Selection bit1 = Comparator reference source, CVRSRC = VREF+ - VREF-0 = Comparator reference source, CVRSRC = AVDD - AVSSCVR<4:0>: Comparator VREF Value Selection 0 ≤ CVR<4:0> ≤ 31 bitsWhen CVRSS = 1: CVREF = (VREF-) + (CVR<4:0>/32) • (VREF+ - VREF-)When CVRSS = 0:						

23.4 Watchdog Timer (WDT)

For the PIC24F16KL402 family of devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

The nominal WDT clock source from LPRC is 31 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the FWPSA Configuration bit. With a 31 kHz input, the prescaler yields a nominal WDT time-out period (TWDT) of 1 ms in 5-bit mode or 4 ms in 7-bit mode.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the Configuration bits, WDTPS<3:0> (FWDT<3:0>), which allow the selection of a total of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler time-out periods, ranges from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- · On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

If the WDT is enabled in hardware (FWDTEN<1:0> = 11), it will continue to run during Sleep or Idle modes. When the WDT time-out occurs, the device will wake and code execution will continue from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bits (RCON<3:2>) will need to be cleared in software after the device wakes up.



The WDT Time-out Flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

Note:	The	CLRWDT	and	PWRSAV	instructions		
	clear the prescaler and postscaler counts						
	wher	n execute	d.				

23.4.1 WINDOWED OPERATION

The Watchdog Timer has an optional Fixed Window mode of operation. In this Windowed mode, CLRWDT instructions can only reset the WDT during the last 1/4 of the programmed WDT period. A CLRWDT instruction, executed before that window, causes a WDT Reset similar to a WDT time-out.

Windowed WDT mode is enabled by programming the Configuration bit, WINDIS (FWDT<6>), to '0'.

23.4.2 CONTROL REGISTER

The WDT is enabled or disabled by the FWDTEN<1:0> Configuration bits. When both the FWDTEN<1:0> Configuration bits are set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN<1:0> Configuration bits have been programmed to '10'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user to enable the WDT for critical code segments, and disable the WDT during non-critical segments, for maximum power savings. When the FWTEN<1:0> bits are set to '01', the WDT is enabled only in Run and Idle modes, and is disabled in Sleep. Software control of the WDT SWDTEN bit (RCON<5>) is disabled with this setting.



TABLE 25-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
PWRSAV	PWRSAV	#lit1	Go into Sleep or Idle mode	1	1	WDTO, Sleep
RCALL	RCALL	Expr	Relative Call	1	2	None
	RCALL	Wn	Computed Call	1	2	None
REPEAT	REPEAT	#lit14	Repeat Next Instruction lit14 + 1 times	1	1	None
	REPEAT	Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
RESET	RESET		Software Device Reset	1	1	None
RETFIE	RETFIE		Return from Interrupt	1	3 (2)	None
RETLW	RETLW	#litl0,Wn	Return with Literal in Wn	1	3 (2)	None
RETURN	RETURN		Return from Subroutine	1	3 (2)	None
RLC	RLC	f	f = Rotate Left through Carry f	1	1	C, N, Z
	RLC	f,WREG	WREG = Rotate Left through Carry f	1	1	C, N, Z
	RLC	Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C, N, Z
RLNC	RLNC	f	f = Rotate Left (No Carry) f	1	1	N, Z
	RLNC	f,WREG	WREG = Rotate Left (No Carry) f	1	1	N, Z
	RLNC	Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N, Z
RRC	RRC	f	f = Rotate Right through Carry f	1	1	C, N, Z
	RRC	f,WREG	WREG = Rotate Right through Carry f	1	1	C, N, Z
	RRC	Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C, N, Z
RRNC	RRNC	f	f = Rotate Right (No Carry) f	1	1	N, Z
	RRNC	f,WREG	WREG = Rotate Right (No Carry) f	1	1	N, Z
	RRNC	Ws,Wd	Wd = Rotate Right (No Carry) Ws	1	1	N, Z
SE	SE	Ws,Wnd	Wnd = Sign-Extended Ws	1	1	C, N, Z
SETM	SETM	f	f = FFFFh	1	1	None
	SETM	WREG	WREG = FFFFh	1	1	None
	SETM	Ws	Ws = FFFFh	1	1	None
SL	SL	f	f = Left Shift f	1	1	C, N, OV, Z
	SL	f,WREG	WREG = Left Shift f	1	1	C, N, OV, Z
	SL	Ws,Wd	Wd = Left Shift Ws	1	1	C, N, OV, Z
	SL	Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N, Z
	SL	Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N, Z
SUB	SUB	f	f = f – WREG	1	1	C, DC, N, OV, Z
	SUB	f,WREG	WREG = f – WREG	1	1	C, DC, N, OV, Z
	SUB	#lit10,Wn	Wn = Wn - lit10	1	1	C, DC, N, OV, Z
	SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1	C, DC, N, OV, Z
	SUB	Wb,#lit5,Wd	Wd = Wb - lit5	1	1	C, DC, N, OV, Z
SUBB	SUBB	f	$f = f - WREG - (\overline{C})$	1	1	C, DC, N, OV, Z
	SUBB	f,WREG	WREG = f – WREG – (\overline{C})	1	1	C, DC, N, OV, Z
	SUBB	#lit10,Wn	Wn = Wn - lit10 - (\overline{C})	1	1	C, DC, N, OV, Z
	SUBB	Wb.Ws.Wd	$Wd = Wb - Ws - (\overline{C})$	1	1	C. DC. N. OV. Z
	STIBB	Wb #lit5 Wd	$Wd = Wb - lit5 - (\overline{C})$	1	1	C DC N OV Z
CIIBP	SUBD	f	f = WREG = f	1	1	
DODIC	SUBP	f WREC	WREG = WREG - f	1	1	
	SUBP	Wh We Wd	Wd = Ws - Wb	1	1	
	SUBP	Wb #lit5 Wd	Wd = lit5 - Wb	1	1	C DC N OV Z
CUDDD	CUDDD	۳۵, ۳1105, Wd	$f = W/PEC = f = (\overline{C})$	1	1	C, DC, N, OV, Z
SUBBR	SUBBR	1		1	1	C, DC, N, OV, Z
	SUBBR	I,WREG		1	1	C, DC, N, OV, Z
	SUBBR	Wb,Ws,Wd	Wd = Ws - Wb - (C)	1	1	C, DC, N, OV, Z
	SUBBR	Wb,#lit5,Wd	Wd = lit5 - Wb - (C)	1	1	C, DC, N, OV, Z
SWAP	SWAP.b	Wn	Wn = Nibble Swap Wn	1	1	None
	SWAP	Wn	Wn = Byte Swap Wn	1	1	None



TABLE 26-27: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 0)

Param No.	Symbol	Characteristic	Min	Мах	Units	Conditions
73	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx Edge	20	_	ns	
74	TscH2dlL, TscL2dlL	Hold Time of SDIx Data Input to SCKx Edge	40	—	ns	
75	TDOR	SDOx Data Output Rise Time		25	ns	
76	TDOF	SDOx Data Output Fall Time	—	25	ns	
78	TscR	SCKx Output Rise Time (Master mode)	—	25	ns	
79	TscF	SCKx Output Fall Time (Master mode)		25	ns	
	FSCK	SCKx Frequency	_	10	MHz	



TABLE 26-28: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
73	TDIV2scH, TDIV2scL	Setup Time of SDIx Data Input to SCKx Edge	35		ns	
74	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	40	—	ns	
75	TDOR	SDOx Data Output Rise Time	—	25	ns	
76	TDOF	SDOx Data Output Fall Time	_	— 25 ns		
78	TscR	SCKx Output Rise Time (Master mode)	_	25 ns		
79	TscF	SCKx Output Fall Time (Master mode)	_	. 25 ns		
81	TDOV2scH, TDOV2scL	SDOx Data Output Setup to SCKx Edge	Тсү	—	ns	
	FSCK	SCKx Frequency	_	10	MHz	

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial							
Param No.	Symbol	Characteristic	Min.	Тур	Max.	Units	Conditions			
Device Supply										
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or 1.8	_	Lesser of: VDD + 0.3 or 3.6	V				
AD02	AVss	Module Vss Supply	Vss – 0.3		Vss + 0.3	V				
Reference Inputs										
AD05	VREFH	Reference Voltage High	AVss + 1.7	_	AVdd	V				
AD06	VREFL	Reference Voltage Low	AVss	_	AVDD - 1.7	V				
AD07	VREF	Absolute Reference Voltage	AVss – 0.3	—	AVDD + 0.3	V				
		·	Analo	g Input			·			
AD10	VINH-VINL	Full-Scale Input Span	VREFL		VREFH	V	(Note 1)			
AD11	Vin	Absolute Input Voltage	AVss - 0.3		AVDD + 0.3	V				
AD12	VINL	Absolute VINL Input Voltage	AVss – 0.3		AVDD/2	V				
AD17	Rin	Recommended Impedance of Analog Voltage Source	_	—	2.5K	Ω	10-bit			
	-		A/D A	ccuracy	-					
AD20b	NR	Resolution	—	10		bits				
AD21b	INL	Integral Nonlinearity	_	±1	±2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V			
AD22b	DNL	Differential Nonlinearity	_	±1	±1.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V			
AD23b	GERR	Gain Error	—	±1	±3	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V			
AD24b	EOFF	Offset Error	—	±1	±2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V			
AD25b		Monotonicity	_	_	_	_	(Note 2)			

TABLE 26-35: A/D MODULE SPECIFICATIONS

Note 1: Measurements are taken with external VREF+ and VREF- used as the A/D voltage reference.

2: The A/D conversion result never decreases with an increase in the input voltage.

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial							
Param No.	Symbol	Characteristic	Min.	Min. Typ Max. Units		Units	Conditions			
Clock Parameters										
AD50	Tad	A/D Clock Period	75	_	—	ns	Tcy = 75 ns, AD1CON3 is in default state			
AD51	TRC	A/D Internal RC Oscillator Period	_	250	—	ns				
	Conversion Rate									
AD55	TCONV	Conversion Time	_	12	_	TAD				
AD56	FCNV	Throughput Rate	—		500	ksps	$AVDD \ge 2.7V$			
AD57	TSAMP	Sample Time	—	1	—	TAD				
AD58	TACQ	Acquisition Time	750	—	—	ns	(Note 2)			
AD59	Tswc	Switching Time from Convert to Sample	—		(Note 3)	—				
AD60	TDIS	Discharge Time	0.5	—	—	TAD				
Clock Parameters										
AD61	TPSS	Sample Start Delay from Setting Sample bit (SAMP)	2		3	TAD				

TABLE 26-36: A/D CONVERSION TIMING REQUIREMENTS⁽¹⁾

Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

2: The time for the holding capacitor to acquire the "New" input voltage when the voltage changes full scale after the conversion (VDD to Vss or Vss to VDD).

3: On the following cycle of the device clock.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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