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## What is "Embedded - Microcontrollers"?

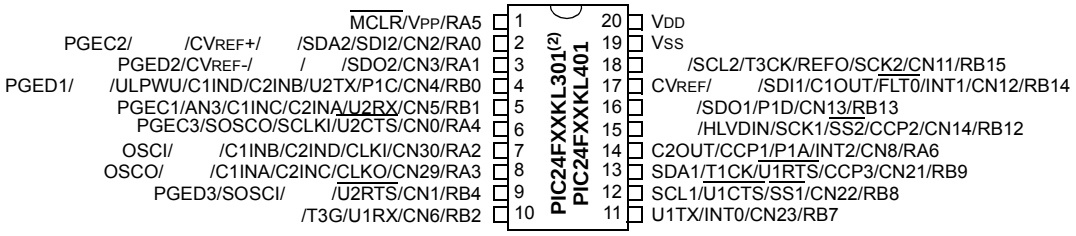
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

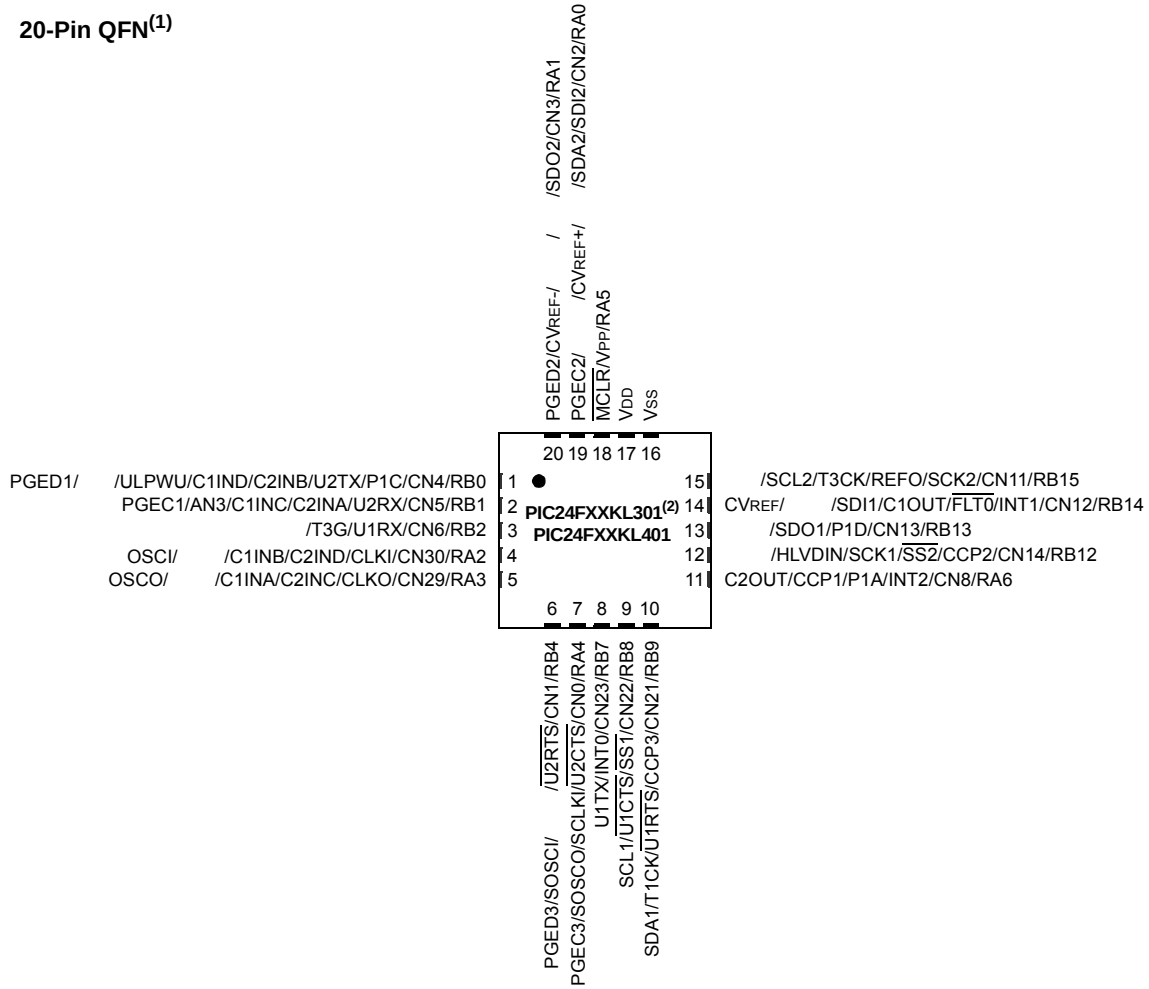
| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, HLVD, POR, PWM, WDT |
| Number of I/O | 18 |
| Program Memory Size | 8KB (2.75K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 20-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24f08kl301-e-ss |

## Pin Diagrams: PIC24FXXKL301/401

### 20-Pin PDIP/SSOP/SOIC(1)




### 20-Pin QFN(1)




**Note 1:** Analog features (indicated in ) are not available on PIC24FXXKL301 devices.

**2:** Alternate location for $I^2C$™ functionality of MSSP1, as determined by the I2C1SEL Configuration bit.

## 1.2 Other Special Features

- **Communications:** The PIC24F16KL402 family incorporates multiple serial communication peripherals to handle a range of application requirements. The MSSP module implements both SPI and $I^2C$™ protocols, and supports both Master and Slave modes of operation for each. Devices also include one of two UARTs with built-in IrDA® encoders/decoders.
- **Analog Features:** Select members of the PIC24F16KL402 family include a 10-bit A/D Converter module. The A/D module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, as well as faster sampling speeds.
  The comparator modules are configurable for a wide range of operations and can be used as either a single or double comparator module.

## 1.3 Details on Individual Family Members

Devices in the PIC24F16KL402 family are available in 14-pin, 20-pin and 28-pin packages. The general block diagram for all devices is shown in Figure 1-1.

The PIC24F16KL402 family may be thought of as four different device groups, each offering a slightly different set of features. These differ from each other in multiple ways:

- The size of the Flash program memory
- The presence and size of data EEPROM
- The presence of an A/D Converter and the number of external analog channels available
- The number of analog comparators
- The number of general purpose timers
- The number and type of CCP modules (i.e., CCP vs. ECCP)
- The number of serial communications modules (both MSSPs and UARTs)

The general differences between the different sub-families are shown in Table 1-1. The feature sets for specific devices are summarized in Table 1-2 and Table 1-3.

A list of the individual pin features available on the PIC24F16KL402 family devices, sorted by function, is provided in Table 1-4 (for PIC24FXXKL40X/30X devices) and Table 1-5 (for PIC24FXXKL20X/10X devices). Note that these tables show the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of this data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

**TABLE 1-1: FEATURE COMPARISON FOR PIC24F16KL402 FAMILY GROUPS**

| Device Group | Program Memory (bytes) | Data EEPROM (bytes) | Timers (8/16-bit) | CCP and ECCP | Serial (MSSP/ UART) | A/D (channels) | Comparators |
|---|---|---|---|---|---|---|---|
| PIC24FXXKL10X | 4K | — | 1/2 | 2/0 | 1/1 | — | 1 |
| PIC24FXXKL20X | 8K | — | 1/2 | 2/0 | 1/1 | 7 or 12 | 1 |
| PIC24FXXKL30X | 8K | 256 | 2/2 | 2/1 | 2/2 | — | 2 |
| PIC24FXXKL40X | 8K or 16K | 512 | 2/2 | 2/1 | 2/2 | 12 | 2 |

**TABLE 1-4: PIC24F16KL40X/30X FAMILY PINOUT DESCRIPTIONS**

| Function | Pin Number | | | | I/O | Buffer | Description |
|---|---|---|---|---|---|---|---|
| | 20-Pin PDIP/ SSOP/ SOIC | 20-Pin QFN | 28-Pin SPDIP/ SSOP/ SOIC | 28-Pin QFN | | | |
| AN0 | 2 | 19 | 2 | 27 | I | ANA | A/D Analog Inputs. Not available on PIC24F16KL30X family devices. |
| AN1 | 3 | 20 | 3 | 28 | I | ANA | |
| AN2 | 4 | 1 | 4 | 1 | I | ANA | |
| AN3 | 5 | 2 | 5 | 2 | I | ANA | |
| AN4 | 6 | 3 | 6 | 3 | I | ANA | |
| AN5 | — | — | 7 | 4 | I | ANA | |
| AN9 | 18 | 15 | 26 | 23 | I | ANA | |
| AN10 | 17 | 14 | 25 | 22 | I | ANA | |
| AN11 | 16 | 13 | 24 | 21 | I | ANA | |
| AN12 | 15 | 12 | 23 | 20 | I | ANA | |
| AN13 | 7 | 4 | 9 | 6 | I | ANA | |
| AN14 | 8 | 5 | 10 | 7 | I | ANA | |
| AN15 | 9 | 6 | 11 | 8 | I | ANA | |
| ASCL1 | — | — | 15 | 12 | I/O | $I^2C$™ | Alternate MSSP1 $I^2C$ Clock Input/Output |
| ASDA1 | — | — | 14 | 11 | I/O | $I^2C$ | Alternate MSSP1 $I^2C$ Data Input/Output |
| AVDD | 20 | 17 | 28 | 25 | I | ANA | Positive Supply for Analog modules |
| AVSS | 19 | 16 | 27 | 24 | I | ANA | Ground Reference for Analog modules |
| CCP1 | 14 | 11 | 20 | 17 | I/O | ST | CCP1/ECCP1 Capture Input/Compare and PWM Output |
| CCP2 | 15 | 12 | 23 | 20 | I/O | ST | CCP2 Capture Input/Compare and PWM Output |
| CCP3 | 13 | 10 | 19 | 16 | I/O | ST | CCP3 Capture Input/Compare and PWM Output |
| C1INA | 8 | 5 | 7 | 4 | I | ANA | Comparator 1 Input A (+) |
| C1INB | 7 | 4 | 6 | 3 | I | ANA | Comparator 1 Input B (-) |
| C1INC | 5 | 2 | 5 | 2 | I | ANA | Comparator 1 Input C (+) |
| C1IND | 4 | 1 | 4 | 1 | I | ANA | Comparator 1 Input D (-) |
| C1OUT | 17 | 14 | 25 | 22 | O | — | Comparator 1 Output |
| C2INA | 5 | 2 | 5 | 2 | I | ANA | Comparator 2 Input A (+) |
| C2INB | 4 | 1 | 4 | 1 | I | ANA | Comparator 2 Input B (-) |
| C2INC | 8 | 5 | 7 | 4 | I | ANA | Comparator 2 Input C (+) |
| C2IND | 7 | 4 | 6 | 3 | I | ANA | Comparator 2 Input D (-) |
| C2OUT | 14 | 11 | 20 | 17 | O | — | Comparator 2 Output |
| CLK I | 7 | 4 | 9 | 6 | I | ANA | Main Clock Input |
| CLKO | 8 | 5 | 10 | 7 | O | — | System Clock Output |

**Legend:** TTL = TTL input buffer
ANA = Analog level input/output
ST = Schmitt Trigger input buffer
$I^2C$ = $I^2C$™/SMBus input buffer

**TABLE 1-5: PIC24F16KL20X/10X FAMILY PINOUT DESCRIPTIONS**

| Function | Pin Number | | | I/O | Buffer | Description |
|---|---|---|---|---|---|---|
| | 20-Pin PDIP/ SSOP/ SOIC | 20-Pin QFN | 14-Pin PDIP/ TSSOP | | | |
| AN0 | 2 | 19 | 2 | I | ANA | A/D Analog Inputs. Not available on PIC24F16KL10X family devices. |
| AN1 | 3 | 20 | 3 | I | ANA | |
| AN2 | 4 | 1 | — | I | ANA | |
| AN3 | 5 | 2 | — | I | ANA | |
| AN4 | 6 | 3 | — | I | ANA | |
| AN9 | 18 | 15 | 12 | I | ANA | |
| AN10 | 17 | 14 | 11 | I | ANA | |
| AN11 | 16 | 13 | — | I | ANA | |
| AN12 | 15 | 12 | — | I | ANA | |
| AN13 | 7 | 4 | 4 | I | ANA | |
| AN14 | 8 | 5 | 5 | I | ANA | |
| AN15 | 9 | 6 | 6 | I | ANA | |
| AVDD | 20 | 17 | 14 | I | ANA | Positive Supply for Analog modules |
| AVSS | 19 | 16 | 13 | I | ANA | Ground Reference for Analog modules |
| CCP1 | 14 | 11 | 10 | I/O | ST | CCP1 Capture Input/Compare and PWM Output |
| CCP2 | 15 | 12 | 9 | I/O | ST | CCP2 Capture Input/Compare and PWM Output |
| C1INA | 8 | 5 | 5 | I | ANA | Comparator 1 Input A (+) |
| C1INB | 7 | 4 | 4 | I | ANA | Comparator 1 Input B (-) |
| C1INC | 5 | 2 | — | I | ANA | Comparator 1 Input C (+) |
| C1IND | 4 | 1 | — | I | ANA | Comparator 1 Input D (-) |
| C1OUT | 17 | 14 | 11 | O | — | Comparator 1 Output |
| CLK I | 7 | 4 | 9 | I | ANA | Main Clock Input |
| CLKO | 8 | 5 | 10 | O | — | System Clock Output |
| CN0 | 10 | 7 | 7 | I | ST | Interrupt-on-Change Inputs |
| CN1 | 9 | 6 | 6 | I | ST | |
| CN2 | 2 | 19 | 2 | I | ST | |
| CN3 | 3 | 20 | 3 | I | ST | |
| CN4 | 4 | 1 | — | I | ST | |
| CN5 | 5 | 2 | — | I | ST | |
| CN6 | 6 | 3 | — | I | ST | |
| CN8 | 14 | 11 | 10 | I | ST | |
| CN9 | — | — | — | I | ST | |
| CN11 | 18 | 15 | 12 | I | ST | |
| CN12 | 17 | 14 | 11 | I | ST | |
| CN13 | 16 | 13 | — | I | ST | |
| CN14 | 15 | 12 | — | I | ST | |
| CN21 | 13 | 10 | 9 | I | ST | |
| CN22 | 12 | 9 | 8 | I | ST | |
| CN23 | 11 | 8 | — | I | ST | |
| CN29 | 8 | 5 | 5 | I | ST | |
| CN30 | 7 | 4 | 4 | I | ST | |

**Legend:** TTL = TTL input buffer
ANA = Analog level input/output
ST = Schmitt Trigger input buffer
$I^2C$ = $I^2C$™/SMBus input buffer

**TABLE 1-5: PIC24F16KL20X/10X FAMILY PINOUT DESCRIPTIONS (CONTINUED)**

| Function | Pin Number | | | I/O | Buffer | Description |
|---|---|---|---|---|---|---|
| | 20-Pin PDIP/ SSOP/ SOIC | 20-Pin QFN | 14-Pin PDIP/ TSSOP | | | |
| CVREF | 17 | 14 | 11 | I | ANA | Comparator Voltage Reference Output |
| CVREF+ | 2 | 19 | 2 | I | ANA | Comparator Reference Positive Input Voltage |
| CVREF- | 3 | 20 | 3 | I | ANA | Comparator Reference Negative Input Voltage |
| HLVDIN | 15 | 12 | 6 | I | ST | High/Low-Voltage Detect Input |
| INT0 | 11 | 8 | 12 | I | ST | Interrupt 0 Input |
| INT1 | 17 | 14 | 11 | I | ST | Interrupt 1 Input |
| INT2 | 14 | 11 | 10 | I | ST | Interrupt 2 Input |
| $\overline{MCLR}$ | 1 | 18 | 1 | I | ST | Master Clear (device Reset) Input. This line is brought low to cause a Reset. |
| OSCI | 7 | 4 | 4 | I | ANA | Main Oscillator Input |
| OSCO | 8 | 5 | 5 | O | ANA | Main Oscillator Output |
| PGEC1 | 5 | 2 | — | I/O | ST | ICSP™ Clock 1 |
| PCED1 | 4 | 1 | — | I/O | ST | ICSP Data 1 |
| PGEC2 | 2 | 19 | 2 | I/O | ST | ICSP Clock 2 |
| PGED2 | 3 | 20 | 3 | I/O | ST | ICSP Data 2 |
| PGEC3 | 10 | 7 | 7 | I/O | ST | ICSP Clock 3 |
| PGED3 | 9 | 6 | 6 | I/O | ST | ICSP Data 3 |
| RA0 | 2 | 19 | 2 | I/O | ST | PORTA Pins |
| RA1 | 3 | 20 | 3 | I/O | ST | |
| RA2 | 7 | 4 | 4 | I/O | ST | |
| RA3 | 8 | 5 | 5 | I/O | ST | |
| RA4 | 10 | 7 | 7 | I/O | ST | |
| RA5 | 1 | 18 | 1 | I | ST | |
| RA6 | 14 | 11 | 10 | I/O | ST | |
| RB0 | 4 | 1 | — | I/O | ST | PORTB Pins |
| RB1 | 5 | 2 | — | I/O | ST | |
| RB2 | 6 | 3 | — | I/O | ST | |
| RB4 | 9 | 6 | 6 | I/O | ST | |
| RB7 | 11 | 8 | — | I/O | ST | |
| RB8 | 12 | 9 | 8 | I/O | ST | |
| RB9 | 13 | 10 | 9 | I/O | ST | |
| RB12 | 15 | 12 | — | I/O | ST | |
| RB13 | 16 | 13 | — | I/O | ST | |
| RB14 | 17 | 14 | 11 | I/O | ST | |
| RB15 | 18 | 15 | 12 | I/O | ST | |
| REFO | 18 | 15 | 12 | O | — | Reference Clock Output |

**Legend:** TTL = TTL input buffer
ANA = Analog level input/output
ST = Schmitt Trigger input buffer
$I^2C$ = $I^2C$™/SMBus input buffer

**EXAMPLE 5-2: ERASING A PROGRAM MEMORY ROW – 'C' LANGUAGE CODE**

```
// C example using MPLAB C30

  int __attribute__ ((space(auto_psv))) progAddr = &progAddr;  // Global variable located in Pgm Memory
  unsigned int offset;

//Set up pointer to the first memory location to be written

  TBLPAG = __builtin_tblpage(&progAddr);                      // Initialize PM Page Boundary SFR
  offset = &progAddr & 0xFFFF;                                // Initialize lower word of address

  __builtin_tblwtl(offset, 0x0000);                           // Set base address of erase block
                                                              // with dummy latch write

  NVMCON = 0x4058;                                            // Initialize NVMCON

  asm("DISI #5");                                             // Block all interrupts for next 5
                                                              // instructions
  __builtin_write_NVM();                                      // C30 function to perform unlock
                                                              // sequence and set WR
```

**EXAMPLE 5-3: LOADING THE WRITE BUFFERS – ASSEMBLY LANGUAGE CODE**

```
; Set up NVMCON for row programming operations
       MOV     #0x4004, W0                 ;
       MOV     W0, NVMCON                  ; Initialize NVMCON
; Set up a pointer to the first program memory location to be written
; program memory selected, and writes enabled
       MOV     #0x0000, W0                 ;
       MOV     W0, TBLPAG                  ; Initialize PM Page Boundary SFR
       MOV     #0x6000, W0                 ; An example program memory address
; Perform the TBLWT instructions to write the latches
; 0th_program_word
       MOV     #LOW_WORD_0, W2             ;
       MOV     #HIGH_BYTE_0, W3            ;
       TBLWTL  W2, [W0]                    ; Write PM low word into program latch
       TBLWTH  W3, [W0++]                  ; Write PM high byte into program latch
; 1st_program_word
       MOV     #LOW_WORD_1, W2             ;
       MOV     #HIGH_BYTE_1, W3            ;
       TBLWTL  W2, [W0]                    ; Write PM low word into program latch
       TBLWTH  W3, [W0++]                  ; Write PM high byte into program latch
;  2nd_program_word
       MOV     #LOW_WORD_2, W2             ;
       MOV     #HIGH_BYTE_2, W3            ;
       TBLWTL  W2, [W0]                    ; Write PM low word into program latch
       TBLWTH  W3, [W0++]                  ; Write PM high byte into program latch
       •
       •
       •
; 32nd_program_word
       MOV     #LOW_WORD_31, W2            ;
       MOV     #HIGH_BYTE_31, W3           ;
       TBLWTL  W2, [W0]                    ; Write PM low word into program latch
       TBLWTH  W3, [W0]                    ; Write PM high byte into program latch
```

### 6.4.1 ERASE DATA EEPROM

The data EEPROM can be fully erased, or can be partially erased, at three different sizes: one word, four words or eight words. The bits, NVMOP<1:0> (NVMCON<1:0>), decide the number of words to be erased. To erase partially from the data EEPROM, the following sequence must be followed:

1. Configure NVMCON to erase the required number of words: one, four or eight.
2. Load TBLPAG and WREG with the EEPROM address to be erased.
3. Clear the NVMIF status bit and enable the NVM interrupt (optional).
4. Write the key sequence to NVMKEY.
5. Set the WR bit to begin the erase cycle.
6. Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).

A typical erase sequence is provided in Example 6-2. This example shows how to do a one-word erase. Similarly, a four-word erase and an eight-word erase can be done. This example uses C library procedures to manage the Table Pointer (`builtin_tblpage` and `builtin_tbloffset`) and the Erase Page Pointer (`builtin_tblwtl`). The memory unlock sequence (`builtin_write_NVM`) also sets the WR bit to initiate the operation and returns control when complete.

**EXAMPLE 6-2: SINGLE-WORD ERASE**

```
int __attribute__ ((space(eedata))) eeData = 0x1234; // Global variable located in EEPROM
    unsigned int offset;

    // Set up NVMCON to erase one word of data EEPROM
    NVMCON = 0x4058;

    // Set up a pointer to the EEPROM location to be erased
    TBLPAG = __builtin_tblpage(&eeData);            // Initialize EE Data page pointer
    offset = __builtin_tbloffset(&eeData);          // Initizlize lower word of address
    __builtin_tblwtl(offset, 0);                    // Write EEPROM data to write latch

    asm volatile ("disi #5");                       // Disable Interrupts For 5 Instructions
    __builtin_write_NVM();                          // Issue Unlock Sequence & Start Write Cycle
    while(NVMCONbits.WR=1);                         // Optional: Poll WR bit to wait for
                                                    // write sequence to complete
```

**REGISTER 8-20: IPC3: INTERRUPT PRIORITY CONTROL REGISTER 3**

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | NVMIP2 | NVMIP1 | NVMIP0 | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | AD1IP2 | AD1IP1 | AD1IP0 | — | U1TXIP2 | U1TXIP1 | U1TXIP0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **NVMIP<2:0>:** NVM Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11-7 **Unimplemented:** Read as ‘0’

bit 6-4 **AD1IP<2:0>:** A/D Conversion Complete Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **U1TXIP<2:0>:** UART1 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

**REGISTER 9-3: OSCTUN: FRC OSCILLATOR TUNE REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | TUN5(1) | TUN4(1) | TUN3(1) | TUN2(1) | TUN1(1) | TUN0(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(1)

011111 = Maximum frequency deviation
011110
•
•
•
000001
000000 = Center frequency, oscillator is running at factory calibrated frequency
111111
•
•
•
100001
100000 = Minimum frequency deviation

**Note 1:** Increments or decrements of TUN<5:0> may not change the FRC frequency in equal steps over the FRC tuning range and may not be monotonic.

## 12.0 TIMER1

| | |
|---|---|
| **Note:** | This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Timers, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Timers"** (DS39704). |

The Timer1 module is a 16-bit timer which can operate as a free-running, interval timer/counter, or serve as the time counter for a software-based Real-Time Clock (RTC). Timer1 is only reset on initial VDD power-on events. This allows the timer to continue operating as an RTC clock source through other types of device Reset.

Timer1 can operate in three modes:

- 16-Bit Timer
- 16-Bit Synchronous Counter
- 16-Bit Asynchronous Counter

Timer1 also supports these features:

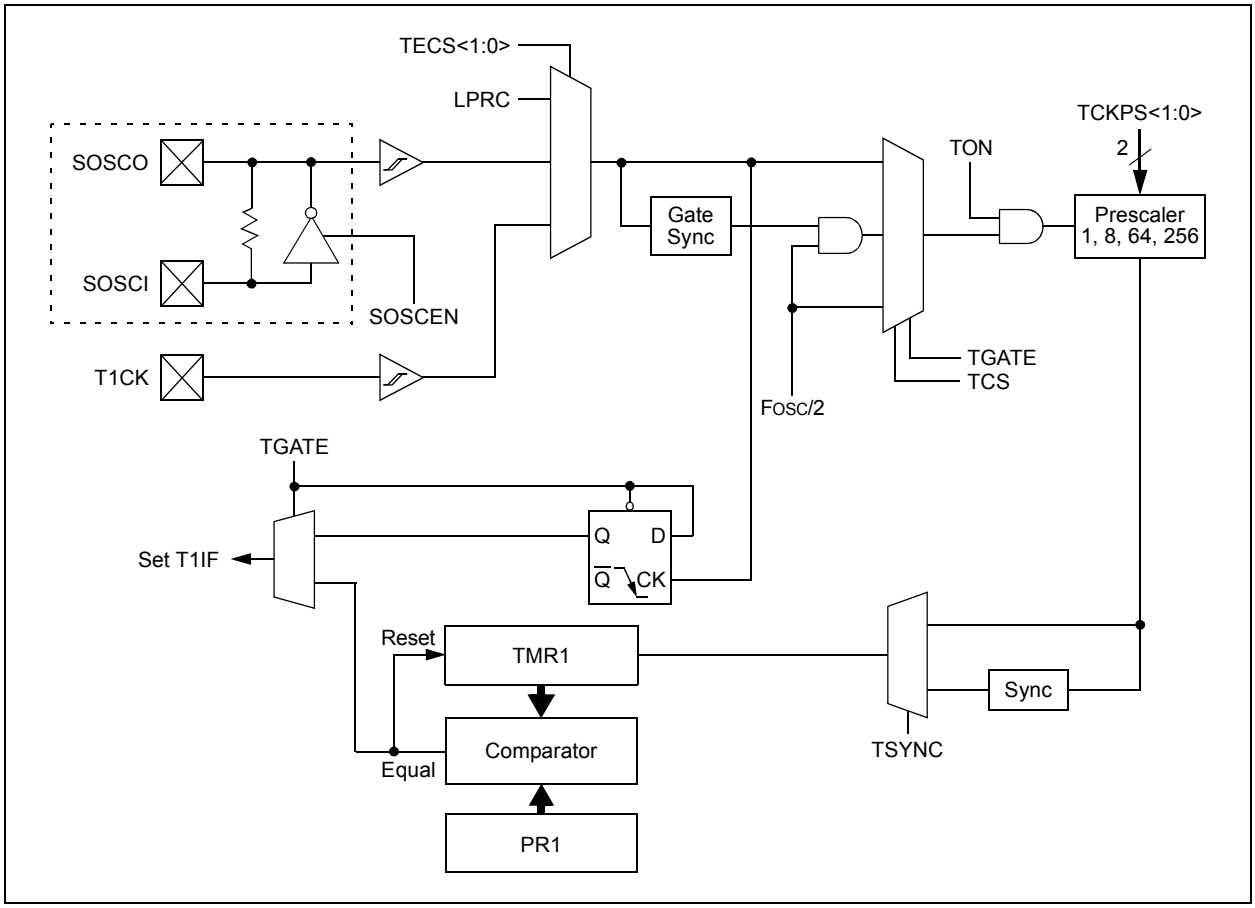
- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation During CPU Idle and Sleep modes
- Interrupt on 16-Bit Period Register Match or Falling Edge of External Gate Signal

Figure 12-1 illustrates a block diagram of the 16-bit Timer1 module.

To configure Timer1 for operation:

1. Set the TON bit (= 1).
2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits.
4. Set or clear the TSYNC bit to configure synchronous or asynchronous operation.
5. Load the timer period value into the PR1 register.
6. If interrupts are required, set the Timer1 Interrupt Enable bit, T1IE. Use the Timer1 Interrupt Priority bits, T1IP<2:0>, to set the interrupt priority.

**FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM**



## 16.0 CAPTURE/COMPARE/PWM (CCP) AND ENHANCED CCP MODULES

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Capture/Compare/PWM module, refer to the *"dsPIC33/PIC24 Family Reference Manual"*.

Depending on the particular device, PIC24F16KL402 family devices include up to three CCP and/or ECCP modules. Key features of all CCP modules include:

- 16-bit input capture for a range of edge events
- 16-bit output compare with multiple output options
- Single-output Pulse-Width Modulation (PWM) with up to 10 bits of resolution
- User-selectable time base from any available timer
- Special Event Trigger on capture and compare events to automatically trigger a range of peripherals

ECCP modules also include these features:

- Operation in Half-Bridge and Full-Bridge (Forward and Reverse) modes
- Pulse steering control across any or all Enhanced PWM pins with user-configurable steering synchronization
- User-configurable external Fault detect with auto-shutdown and auto-restart

PIC24FXXKL40X/30X devices instantiate three CCP modules, one Enhanced (ECCP1) and two standard (CCP2 and CCP3). All other devices instantiate two standard CCP modules (CCP1 and CCP2).

### 16.1 Timer Selection

On all PIC24F16KL402 family devices, the CCP and ECCP modules use Timer3 as the time base for capture and compare operations. PWM and Enhanced PWM operations may use either Timer2 or Timer4. PWM time base selection is done through the CCPTMRS0 register (Register 16-6).

### 16.2 CCP I/O Pins

To configure I/O pins with a CCP function, the proper mode must be selected by setting the CCPxM<3:0> bits.

Where the Enhanced CCP module is available, it may have up to four PWM outputs depending on the selected operating mode. These outputs are designated, P1A through P1D. The outputs that are active depend on the ECCP operating mode selected. To configure I/O pins for Enhanced PWM operation, the proper PWM mode must be selected by setting the PM<1:0> and CCPxM<3:0> bits.

**REGISTER 16-2: CCP1CON: ECCP1 CONTROL REGISTER (ECCP MODULES ONLY)(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PM1 | PM0 | DC1B1 | DC1B0 | CCP1M3(2) | CCP1M2(2) | CCP1M1(2) | CCP1M0(2) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7-6 **PM<1:0>:** Enhanced PWM Output Configuration bits

If CCP1M<3:2> = 00, 01, 10:

xx = P1A is assigned as a capture input or compare output; P1B, P1C and P1D are assigned as port pins

If CCP1M<3:2> = 11:

11 = Full-bridge output reverse: P1B is modulated; P1C is active; P1A and P1D are inactive

10 = Half-bridge output: P1A, P1B are modulated with dead-band control; P1C and P1D are assigned as port pins

01 = Full-bridge output forward: P1D is modulated; P1A is active; P1B, P1C are inactive

00 = Single output: P1A, P1B, P1C and P1D are controlled by steering

bit 5-4 **DC1B<1:0>**: PWM Duty Cycle bit 1 and bit 0 for CCP1 Module bits

Capture and Compare modes:

Unused.

PWM mode:

These bits are the two Least Significant bits (bit 1 and bit 0) of the 10-bit PWM duty cycle. The eight Most Significant bits (DC1B<9:2>) of the duty cycle are found in CCPR1L.

bit 3-0 **CCP1M<3:0>**: ECCP1 Module Mode Select bits(2)

1111 = PWM mode: P1A and P1C are active-low; P1B and P1D are active-low

1110 = PWM mode: P1A and P1C are active-low; P1B and P1D are active-high

1101 = PWM mode: P1A and P1C are active-high; P1B and P1D are active-low

1100 = PWM mode: P1A and P1C are active-high; P1B and P1D are active-high

1011 = Compare mode: Special Event Trigger; resets timer on CCP1 match (CCPxIF bit is set)

1010 = Compare mode: Generates software interrupt on compare match (CCP1IF bit is set, CCP1 pin reflects I/O state)

1001 = Compare mode: Initializes CCP1 pin high; on compare match, forces CCP1 pin low (CCP1IF bit is set)

1000 = Compare mode: Initializes CCP1 pin low; on compare match, forces CCP1 pin high (CCP1IF bit is set)

0111 = Capture mode: Every 16th rising edge

0110 = Capture mode: Every 4th rising edge

0101 = Capture mode: Every rising edge

0100 = Capture mode: Every falling edge

0011 = Reserved

0010 = Compare mode: Toggles output on match (CCP1IF bit is set)

0001 = Reserved

0000 = Capture/Compare/PWM is disabled (resets CCP1 module)

**Note 1:** This register is implemented only on PIC24FXXKL40X/30X devices. For all other devices, CCP1CON is configured as Register 16-1.

**2:** CCP1M<3:0> = 1011 will only reset the timer and not start the A/D conversion on a CCP1 match.

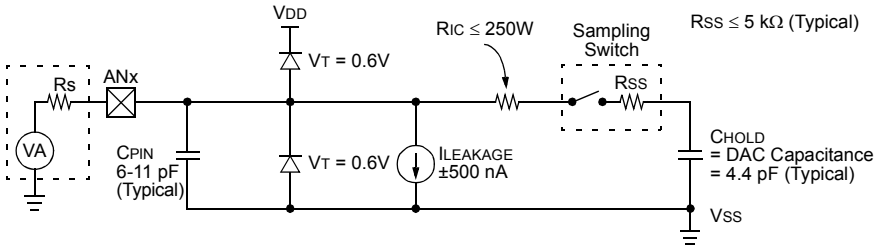
**EQUATION 19-1: A/D CONVERSION CLOCK PERIOD(1)**

$$ADCS = \frac{TAD}{TCY} - 1$$

$$TAD = TCY \bullet (ADCS + 1)$$

**Note 1:** Based on TCY = 2 * TOSC; Doze mode and PLL are disabled.

**FIGURE 19-2: 10-BIT A/D CONVERTER ANALOG INPUT MODEL**




| Legend: | | |
|---|---|---|
| | CPIN | = Input Capacitance |
| | VT | = Threshold Voltage |
| | ILEAKAGE | = Leakage Current at the pin due to Various Junctions |
| | RIC | = Interconnect Resistance |
| | RSS | = Sampling Switch Resistance |
| | CHOLD | = Sample/Hold Capacitance (from DAC) |

**Note:** CPIN value depends on device package and is not tested. Effect of CPIN is negligible if Rs ≤ 5 kΩ.

## 23.0 SPECIAL FEATURES

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Watchdog Timer, High-Level Device Integration and Programming Diagnostics, refer to the individual sections of the *"dsPIC33/PIC24 Family Reference Manual"* provided below:

- **"Watchdog Timer (WDT)"** (DS39697)
- **"High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)"** (DS39725)
- **"Programming and Diagnostics"** (DS39716)

PIC24F16KL402 family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation
- Factory Programmed Unique ID

### 23.1 Code Protect Security Options

The Boot Segment (BS) and General Segment (GS) are two segments on this device with separate programmable security levels. The Boot Segment, configured via the FBS Configuration register, can have three possible levels of security:

- **No Security (BSS = 111):** The Boot Segment is not utilized and all addresses in program memory are part of the General Segment (GS).
- **Standard Security (BSS = 110 or 101):** The Boot Segment is enabled and code-protected, preventing ICSP reads of the Flash memory. Standard security also prevents Flash reads and writes of the BS from the GS. The BS can still read and write to itself.
- **High Security (BSS = 010 or 001):** The Boot Segment is enabled with all of the security provided by Standard Security mode. In addition, in High-Security mode, there are program flow change restrictions in place. While executing from the GS, program flow changes that attempt to enter the BS (e.g., branch (BRA) or CALL instructions) can only enter the BS at one of the first 32 instruction locations (0x200 to 0x23F). Attempting to jump into the BS at an instruction higher than this will result in an Illegal Opcode Reset.

The General Segment, configured via the FGS Configuration register, can have two levels of security:

- **No Security (GSS0 = 1):** The GS is not code-protected and can be read in all modes.
- **Standard Security (GSS0 = 0):** The GS is code-protected, preventing ICSP reads of the Flash memory.

For more detailed information on these Security modes, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"CodeGuard™ Security"** (DS70199).

### 23.2 Configuration Bits

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location, F80000h. A complete list is provided in Table 23-1. A detailed explanation of the various bit functions is provided in Register 23-1 through Register 23-7.

The address, F80000h, is beyond the user program memory space. In fact, it belongs to the configuration memory space (800000h-FFFFFFh), which can only be accessed using Table Reads and Table Writes.

**TABLE 23-1: CONFIGURATION REGISTERS LOCATIONS**

| Configuration Register | Address |
|---|---|
| FBS | F80000 |
| FGS | F80004 |
| FOSCSEL | F80006 |
| FOSC | F80008 |
| FWDT | F8000A |
| FPOR | F8000C |
| FICD | F8000E |

**TABLE 26-1: THERMAL OPERATING CONDITIONS**

| Rating | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating Junction Temperature Range | $T_J$ | -40 | — | +140 | °C |
| Operating Ambient Temperature Range | $T_A$ | -40 | — | +125 | °C |
| Power Dissipation:<br>Internal Chip Power Dissipation:<br>$P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$<br>I/O Pin Power Dissipation:<br>$P_{I/O} = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$ | $P_D$ | $P_{INT} + P_{I/O}$ | | | W |
| Maximum Allowed Power Dissipation | $P_{DMAX}$ | $(T_J - T_A)/\theta_{JA}$ | | | W |

**TABLE 26-2: THERMAL PACKAGING CHARACTERISTICS**

| Characteristic | Symbol | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| Package Thermal Resistance, 20-Pin PDIP | $\theta_{JA}$ | 62.4 | — | °C/W | **1** |
| Package Thermal Resistance, 28-Pin SPDIP | $\theta_{JA}$ | 60 | — | °C/W | **1** |
| Package Thermal Resistance, 20-Pin SSOP | $\theta_{JA}$ | 108 | — | °C/W | **1** |
| Package Thermal Resistance, 28-Pin SSOP | $\theta_{JA}$ | 71 | — | °C/W | **1** |
| Package Thermal Resistance, 20-Pin SOIC | $\theta_{JA}$ | 75 | — | °C/W | **1** |
| Package Thermal Resistance, 28-Pin SOIC | $\theta_{JA}$ | 80.2 | — | °C/W | **1** |
| Package Thermal Resistance, 20-Pin QFN | $\theta_{JA}$ | 43 | — | °C/W | **1** |
| Package Thermal Resistance, 28-Pin QFN | $\theta_{JA}$ | 32 | — | °C/W | **1** |
| Package Thermal Resistance, 14-Pin PDIP | $\theta_{JA}$ | 62.4 | — | °C/W | **1** |
| Package Thermal Resistance, 14-Pin TSSOP | $\theta_{JA}$ | 108 | — | °C/W | **1** |

**Note 1:** Junction to ambient thermal resistance, Theta-$_{JA}$ ($\theta_{JA}$) numbers are achieved by package simulations.

**TABLE 26-3: DC CHARACTERISTICS: TEMPERATURE AND VOLTAGE SPECIFICATIONS**

| **DC CHARACTERISTICS** | | | **Standard Operating Conditions: 1.8V to 3.6V**<br>Operating temperature -40°C ≤ $T_A$ ≤ +85°C for Industrial<br>-40°C ≤ $T_A$ ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| DC10 | $V_{DD}$ | **Supply Voltage** | 1.8 | — | 3.6 | V | |
| DC12 | $V_{DR}$ | **RAM Data Retention Voltage(2)** | 1.5 | — | — | V | |
| DC16 | $V_{POR}$ | **$V_{DD}$ Start Voltage** to Ensure Internal Power-on Reset Signal | $V_{SS}$ | — | 0.7 | V | |
| DC17 | $SV_{DD}$ | **$V_{DD}$ Rise Rate** to Ensure Internal Power-on Reset Signal | 0.05 | — | — | V/ms | 0-3.3V in 0.1s<br>0-2.5V in 60 ms |
| | $V_{BG}$ | **Band Gap Voltage Reference** | 1.14 | 1.2 | 1.26 | V | |

**Note 1:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** This is the limit to which $V_{DD}$ can be lowered without losing RAM data.

**TABLE 26-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 1.8V to 3.6V<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** | |
| | VOL | **Output Low Voltage** | | | | | | |
| DO10 | | All I/O Pins | — | — | 0.4 | V | IOL = 4.0 mA | VDD = 3.6V |
| | | | — | — | 0.4 | V | IOL = 3.5 mA | VDD = 2.0V |
| DO16 | | OSC2/CLKO | — | — | 0.4 | V | IOL = 1.2 mA | VDD = 3.6V |
| | | | — | — | 0.4 | V | IOL = 0.4 mA | VDD = 2.0V |
| | VOH | **Output High Voltage** | | | | | | |
| DO20 | | All I/O Pins | 3 | — | — | V | IOH = -3.0 mA | VDD = 3.6V |
| | | | 1.6 | — | — | V | IOH = -1.0 mA | VDD = 2.0V |
| DO26 | | OSC2/CLKO | 3 | — | — | V | IOH = -1.0 mA | VDD = 3.6V |
| | | | 1.6 | — | — | V | IOH = -0.5 mA | VDD = 2.0V |

**Note 1:** Data in "Typ" column is at +25°C unless otherwise stated.

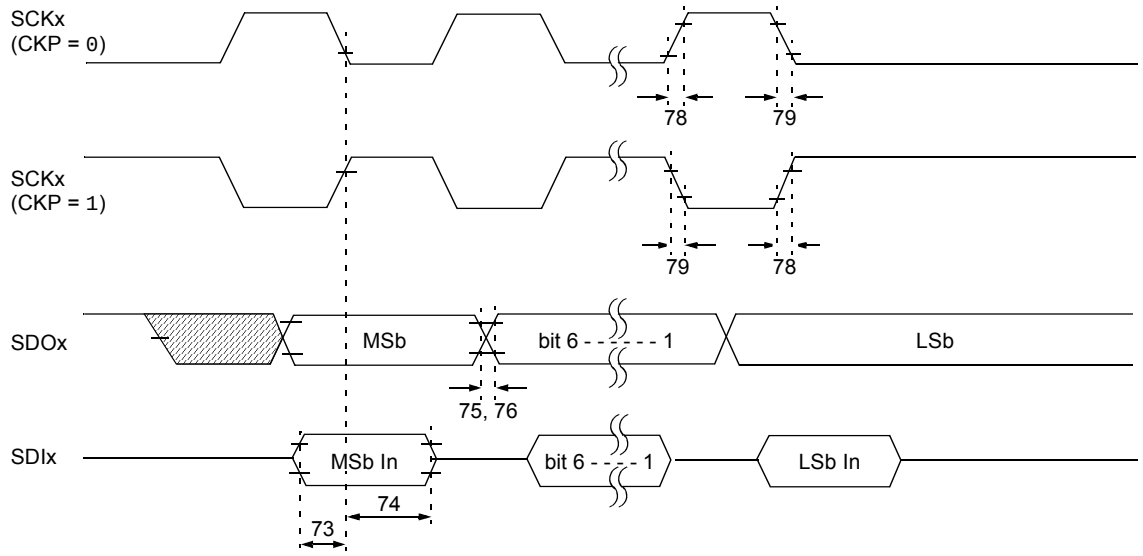
**TABLE 26-12: DC CHARACTERISTICS: PROGRAM MEMORY**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 1.8V to 3.6V<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| | | **Program Flash Memory** | | | | | |
| D130 | EP | Cell Endurance | 10,000(2) | — | — | E/W | |
| D131 | VPR | VDD for Read | VMIN | — | 3.6 | V | VMIN = Minimum operating voltage |
| D133A | TIW | Self-Timed Write Cycle Time | — | 2 | — | ms | |
| D134 | TRETD | Characteristic Retention | 40 | — | — | Year | Provided no other specifications are violated |
| D135 | IDDP | Supply Current During Programming | — | 10 | — | mA | |

**Note 1:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**2:** Self-write and block erase.

**FIGURE 26-7: EXAMPLE SPI MASTER MODE TIMING (CKE = 0)**




**Note:** Refer to Figure 26-3 for load conditions.

**TABLE 26-27: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 0)**

| Param No. | Symbol | Characteristic | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| 73 | TDIV2SCH, TDIV2SCL | Setup Time of SDIx Data Input to SCKx Edge | 20 | — | ns | |
| 74 | TSCH2DIL, TSCL2DIL | Hold Time of SDIx Data Input to SCKx Edge | 40 | — | ns | |
| 75 | TDOR | SDOx Data Output Rise Time | — | 25 | ns | |
| 76 | TDOF | SDOx Data Output Fall Time | — | 25 | ns | |
| 78 | TSCR | SCKx Output Rise Time (Master mode) | — | 25 | ns | |
| 79 | TSCF | SCKx Output Fall Time (Master mode) | — | 25 | ns | |
| | FSCK | SCKx Frequency | — | 10 | MHz | |

**TABLE 26-32: I²C™ BUS DATA REQUIREMENTS (SLAVE MODE)**

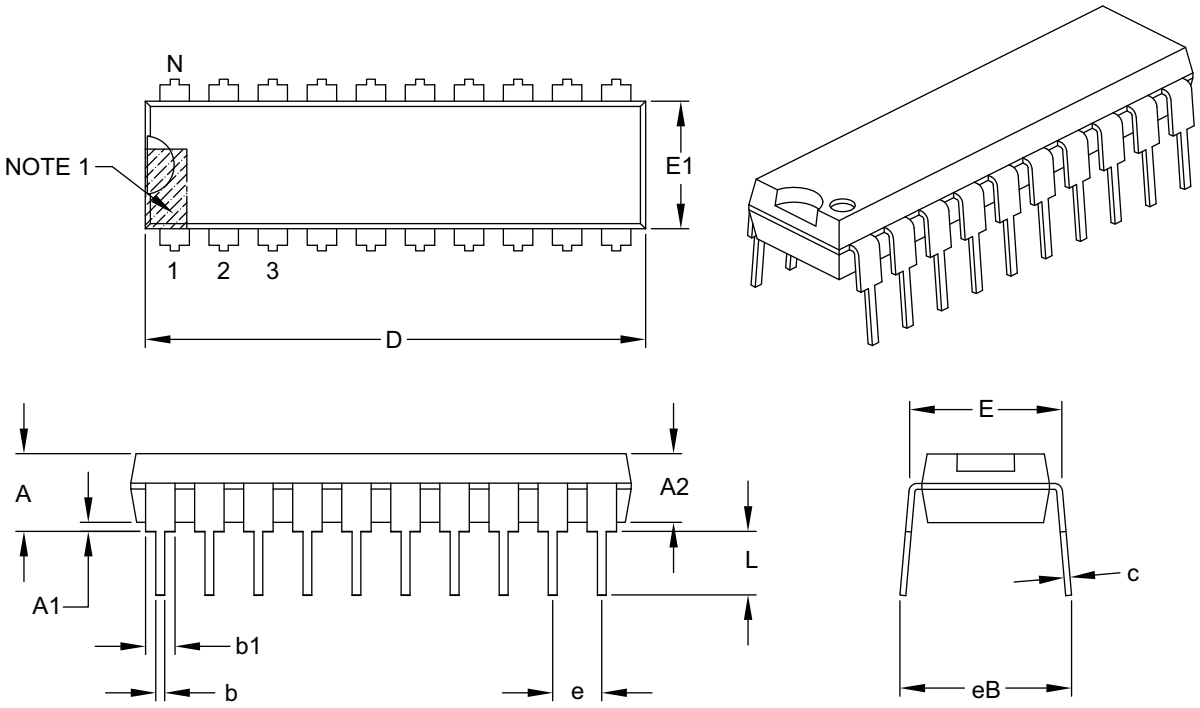
| Param. No. | Symbol | Characteristic | | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 100 | THIGH | Clock High Time | 100 kHz mode | 4.0 | — | µs | Must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 0.6 | — | µs | Must operate at a minimum of 10 MHz |
| | | | MSSP module | 1.5 | — | TCY | |
| 101 | TLOW | Clock Low Time | 100 kHz mode | 4.7 | — | µs | Must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 1.3 | — | µs | Must operate at a minimum of 10 MHz |
| | | | MSSP module | 1.5 | — | TCY | |
| 102 | TR | SDAx and SCLx Rise Time | 100 kHz mode | — | 1000 | ns | |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | CB is specified to be from 10 to 400 pF |
| 103 | TF | SDAx and SCLx Fall Time | 100 kHz mode | — | 300 | ns | |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | CB is specified to be from 10 to 400 pF |
| 90 | TSU:STA | Start Condition Setup Time | 100 kHz mode | 4.7 | — | µs | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | 0.6 | — | µs | |
| 91 | THD:STA | Start Condition Hold Time | 100 kHz mode | 4.0 | — | µs | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | 0.6 | — | µs | |
| 106 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | ns | |
| | | | 400 kHz mode | 0 | 0.9 | µs | |
| 107 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | **(Note 2)** |
| | | | 400 kHz mode | 100 | — | ns | |
| 92 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | 4.7 | — | µs | |
| | | | 400 kHz mode | 0.6 | — | µs | |
| 109 | TAA | Output Valid from Clock | 100 kHz mode | — | 3500 | ns | **(Note 1)** |
| | | | 400 kHz mode | — | — | ns | |
| 110 | TBUF | Bus Free Time | 100 kHz mode | 4.7 | — | µs | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | µs | |
| D102 | CB | Bus Capacitive Loading | | — | 400 | pF | |

**Note 1:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCLx to avoid unintended generation of Start or Stop conditions.

**2:** A Fast mode I²C™ bus device can be used in a Standard mode I²C bus system, but the requirement, TSU:DAT ≥ 250 ns, must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLx signal. If such a device does stretch the LOW period of the SCLx signal, it must output the next data bit to the SDAx line, TR max. + TSU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCLx line is released.

## 20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 20 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .300 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .980 | 1.030 | 1.060 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .045 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-019B

## R



## S