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Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VQFN Exposed Pad
Supplier Device Package	20-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f08kl301-i-mq

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4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® devices and improve data space memory usage efficiency, the PIC24F instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address (EA) calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] will result in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

Data byte reads will read the complete word, which contains the byte, using the LSB of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and the registers are organized as two parallel, byte-wide entities with shared (word) address decode, but separate write lines. Data byte writes only write to the corresponding side of the array or register, which matches the byte address.

All word accesses must be aligned to an even address. Mis-aligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a mis-aligned read or write is attempted, an address error trap will be generated. If the error occurred on a read, the instruction underway is completed; if it occurred on a write, the instruction will be executed, but the write will not occur. In either case, a trap is then executed, allowing the system and/or user to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB; the MSB is not modified.

A Sign-Extend (SE) instruction is provided to allow the users to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, users

can clear the MSB of any W register by executing a Zero-Extend (\mathbb{ZE}) instruction on the appropriate address.

Although most instructions are capable of operating on word or byte data sizes, it should be noted that some instructions operate only on words.

4.2.3 NEAR DATA SPACE

The 8-Kbyte area between 0000h and 1FFFh is referred to as the Near Data Space (NDS). Locations in this space are directly addressable via a 13-bit absolute address field within all memory direct instructions. The remainder of the data space is addressable indirectly. Additionally, the whole data space is addressable using MOV instructions, which support Memory Direct Addressing (MDA) with a 16-bit address field. For PIC24F16KL402 family devices, the entire implemented data memory lies in Near Data Space.

4.2.4 SFR SPACE

The first 2 Kbytes of the Near Data Space, from 0000h to 07FFh, are primarily occupied with Special Function Registers (SFRs). These are used by the PIC24F core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by the module. Much of the SFR space contains unused addresses; these are read as '0'. The SFR space, where the SFRs are actually implemented, is provided in Table 4-2. Each implemented area indicates a 32-byte region, where at least one address is implemented as an SFR. A complete listing of implemented SFRs, including their addresses, is provided in Table 4-3 through Table 4-18.

TABLE 4-2:	IMPLEMENTED REGIONS OF SFR DATA SPACE
IADLE 4-2.	IMPLEMENTED REGIONS OF SER DATA SPACE

	SFR Space Address											
	xx00 xx20 xx40		xx40	xx60	xx60 xx80		xxC0	xxE0				
000h		Core		ICN	Interrupts			_				
100h	Timers	- TMR	_	_	_ C0	CP —	_	_				
200h	MSSP	UART	_	_	_	_	I/O	_				
300h	A	/D	_	_	_	_	_	_				
400h	_	_	_	_	_	_	_ AN	SEL —				
500h			_	_	_	_	_	_				
600h	ı	CMP —	-	_	_	_	1	_				
700h	_	_	System	NVM/PMD	_	_	_	_				

Legend: — = No implemented SFRs in this block.

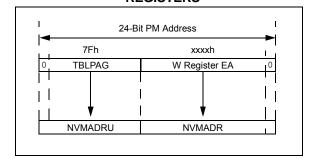
6.3 NVM Address Register

As with Flash program memory, the NVM Address Registers, NVMADRU and NVMADR, form the 24-bit Effective Address (EA) of the selected row or word for data EEPROM operations. The NVMADRU register is used to hold the upper 8 bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA. These registers are not mapped into the Special Function Register (SFR) space; instead, they directly capture the EA<23:0> of the last Table Write instruction that has been executed and selects the data EEPROM row to erase. Figure 6-1 depicts the program memory EA that is formed for programming and erase operations.

Like program memory operations, the Least Significant bit (LSb) of NVMADR is restricted to even addresses. This is because any given address in the data EEPROM space consists of only the lower word of the program memory width; the upper word, including the uppermost "phantom byte", is unavailable. This means that the LSb of a data EEPROM address will always be '0'.

Similarly, the Most Significant bit (MSb) of NVMADRU is always '0', since all addresses lie in the user program space.

FIGURE 6-1: DATA EEPROM
ADDRESSING WITH TBLPAG
AND NVM ADDRESS
REGISTERS



6.4 Data EEPROM Operations

The EEPROM block is accessed using Table Read and Table Write operations, similar to those used for program memory. The TBLWTH and TBLRDH instructions are not required for data EEPROM operations since the memory is only 16 bits wide (data on the lower address is valid only). The following programming operations can be performed on the data EEPROM:

- · Erase one, four or eight words
- Bulk erase the entire data EEPROM
- · Write one word
- · Read one word

Note: Unexpected results will be obtained if the user attempts to read the EEPROM while a programming or erase operation is underway.

The C30 C compiler includes library procedures to automatically perform the Table Read and Table Write operations, manage the Table Pointer and write buffers, and unlock and initiate memory write sequences. This eliminates the need to create assembler macros or time critical routines in C for each application.

The library procedures are used in the code examples detailed in the following sections. General descriptions of each process are provided for users who are not using the C30 compiler libraries.

REGISTER 8-26: IPC12: INTERRUPT PRIORITY CONTROL REGISTER 12

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
_	_	_	_	_	BCL2IP2 ⁽¹⁾	BCL2IP1 ⁽¹⁾	BCL2IP0 ⁽¹⁾
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
_	SSP2IP2 ⁽¹⁾	SSP2IP1 ⁽¹⁾	SSP2IP0 ⁽¹⁾	_	_	_	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 BCL2IP<2:0>: MSSP2 I²C™ Bus Collision Interrupt Priority bits⁽¹⁾

111 = Interrupt is Priority 7 (highest priority interrupt)

•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 SSP2IP<2:0>: MSSP2 SPI/I²C Event Interrupt Priority bits⁽¹⁾

111 = Interrupt is Priority 7 (highest priority interrupt)

•

_

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

Note 1: These bits are unimplemented on PIC24FXXKL10X and PIC24FXXKL20X devices.

REGISTER 9-4: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROEN	_	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	I	_	_	_		_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 ROEN: Reference Oscillator Output Enable bit

1 = Reference oscillator is enabled on REFO pin

0 = Reference oscillator is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 ROSSLP: Reference Oscillator Output Stop in Sleep bit

1 = Reference oscillator continues to run in Sleep

0 = Reference oscillator is disabled in Sleep

bit 12 ROSEL: Reference Oscillator Source Select bit

1 = Primary oscillator is used as the base clock⁽¹⁾

0 = System clock is used as the base clock; the base clock reflects any clock switching of the device

bit 11-8 RODIV<3:0>: Reference Oscillator Divisor Select bits

1111 = Base clock value divided by 32,768

1110 = Base clock value divided by 16,384

1101 = Base clock value divided by 8,192

1100 = Base clock value divided by 4,096

1011 = Base clock value divided by 2,048

1010 = Base clock value divided by 1,024

1001 = Base clock value divided by 512

1000 = Base clock value divided by 256

0111 = Base clock value divided by 128

0110 = Base clock value divided by 64

0101 = Base clock value divided by 32

0100 = Base clock value divided by 16

0011 = Base clock value divided by 8

0011 - Base clock value divided by 8 0010 = Base clock value divided by 4

0001 = Base clock value divided by 2

0000 = Base clock value

bit 7-0 **Unimplemented:** Read as '0'

Note 1: The crystal oscillator must be enabled using the FOSC<2:0> bits; the crystal maintains the operation in Sleep mode.

10.4 Doze Mode

Generally, changing clock speed and invoking one of the power-saving modes are the preferred strategies for reducing power consumption. There may be circumstances, however, where this is not practical. For example, it may be necessary for an application to maintain uninterrupted, synchronous communication, even while it is doing nothing else. Reducing system clock speed may introduce communication errors, while using a power-saving mode may stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default.

It is also possible to use Doze mode to selectively reduce power consumption in event driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption. Meanwhile, the CPU Idles, waiting for something to invoke an interrupt routine. Enabling the automatic return to full-speed CPU operation on interrupts is enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

10.5 Selective Peripheral Module Control

Idle and Doze modes allow users to substantially reduce power consumption by slowing or stopping the CPU clock. Even so, peripheral modules still remain clocked and thus, consume power. There may be cases where the application needs what these modes do not provide: the allocation of power resources to CPU processing, with minimal power consumption from the peripherals.

PIC24F devices address this requirement by allowing peripheral modules to be selectively disabled, reducing or eliminating their power consumption. This can be done with two control bits:

- The Peripheral Enable bit, generically named, "XXXEN", located in the module's main control SER
- The Peripheral Module Disable (PMD) bit, generically named, "XXXMD", located in one of the PMD Control registers.

Both bits have similar functions in enabling or disabling its associated module. Setting the PMD bit for a module disables all clock sources to that module, reducing its power consumption to an absolute minimum. In this state, the control and status registers associated with the peripheral will also be disabled, so writes to those registers will have no effect, and read values will be invalid. Many peripheral modules have a corresponding PMD bit.

In contrast, disabling a module by clearing its XXXEN bit, disables its functionality, but leaves its registers available to be read and written to. Power consumption is reduced, but not by as much as when the PMD bits are used.

To achieve more selective power savings, peripheral modules can also be selectively disabled when the device enters Idle mode. This is done through the control bit of the generic name format, "XXXIDL". By default, all modules that can operate during Idle mode will do so. Using the disable on Idle feature disables the module while in Idle mode, allowing further reduction of power consumption during Idle mode. This enhances power savings for extremely critical power applications.

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
TON	_	TSIDL	_	_	_	T1ECS1 ⁽¹⁾	T1ECS0 ⁽¹⁾
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
_	TGATE	TCKPS1	TCKPS0	_	TSYNC	TCS	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 TON: Timer1 On bit

1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1

bit 14 Unimplemented: Read as '0'

bit 13 TSIDL: Timer1 Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode

0 = Continues module operation in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9-8 T1ECS <1:0>: Timer1 Extended Clock Select bits⁽¹⁾

11 = Reserved; do not use

10 = Timer1 uses the LPRC as the clock source

01 = Timer1 uses the external clock from T1CK

00 = Timer1 uses the Secondary Oscillator (SOSC) as the clock source

bit 7 **Unimplemented:** Read as '0'

bit 6 TGATE: Timer1 Gated Time Accumulation Enable bit

When TCS = 1: This bit is ignored. When TCS = 0:

1 = Gated time accumulation is enabled0 = Gated time accumulation is disabled

bit 5-4 TCKPS<1:0>: Timer1 Input Clock Prescale Select bits

11 = 1:256

10 = 1:64

01 = 1:8

00 = 1:1

bit 3 Unimplemented: Read as '0'

bit 2 TSYNC: Timer1 External Clock Input Synchronization Select bit

When TCS = 1:

1 = Synchronizes external clock input

0 = Does not synchronize external clock input

When TCS = 0: This bit is ignored.

bit 1 TCS: Timer1 Clock Source Select bit

1 = Timer1 clock source is selected by T1ECS<1:0>

0 = Internal clock (Fosc/2)

bit 0 **Unimplemented:** Read as '0'

Note 1: The T1ECSx bits are valid only when TCS = 1.

REGISTER 16-1: CCPxCON: CCPx CONTROL REGISTER (STANDARD CCP MODULES)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	DCxB1	DCxB0	CCPxM3 ⁽¹⁾	CCPxM2 ⁽¹⁾	CCPxM1 ⁽¹⁾	CCPxM0 ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-4 DCxB<1:0>: PWM Duty Cycle Bit 1 and Bit 0 for CCPx Module bits

Capture and Compare modes:

Unused.

PWM mode:

These bits are the two Least Significant bits (bit 1 and bit 0) of the 10-bit PWM duty cycle. The eight Most Significant bits (DCxB<9:2>) of the duty cycle are found in CCPRxL.

bit 3-0 CCPxM<3:0>: CCPx Module Mode Select bits⁽¹⁾

1111 = Reserved

1110 = Reserved

1101 = Reserved

1100 = PWM mode

1011 = Compare mode: Special Event Trigger; resets timer on CCPx match (CCPxIF bit is set)

1010 = Compare mode: Generates software interrupt on compare match (CCPxIF bit is set, CCPx pin reflects I/O state)

1001 = Compare mode: Initializes CCPx pin high; on compare match, forces CCPx pin low (CCPxIF bit is set)

1000 = Compare mode: Initializes CCPx pin low; on compare match, forces CCPx pin high (CCPxIF bit is set)

0111 = Capture mode: Every 16th rising edge

0110 = Capture mode: Every 4th rising edge

0101 = Capture mode: Every rising edge

0100 = Capture mode: Every falling edge

0011 = Reserved

0010 = Compare mode: Toggles output on match (CCPxIF bit is set)

0001 = Reserved

0000 = Capture/Compare/PWM is disabled (resets CCPx module)

Note 1: CCPxM<3:0> = 1011 will only reset the timer and not start the A/D conversion on a CCPx match.

NOTES:

18.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note:

This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Universal Asynchronous Receiver Transmitter, refer to the "dsPIC33/PIC24 Family Reference Manual", "UART" (DS39708).

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in this PIC24F device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. This module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA $^{\otimes}$ encoder and decoder.

The primary features of the UART module are:

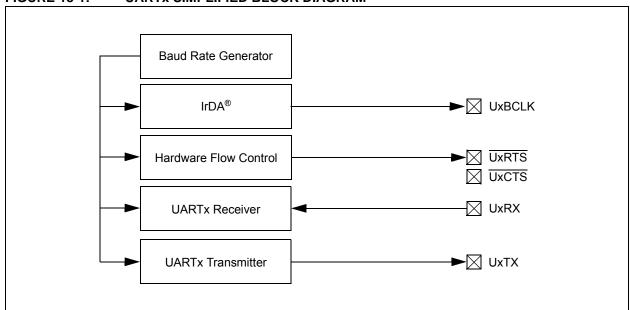
- Full-Duplex, 8-Bit or 9-Bit Data Transmission Through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- · One or Two Stop bits
- Hardware Flow Control Option with UxCTS and UxRTS Pins

- Fully Integrated Baud Rate Generator (IBRG) with 16-Bit Prescaler
- Baud Rates Ranging from 1 Mbps to 15 bps at 16 MIPS
- Two-Level Deep, First-In-First-Out (FIFO)
 Transmit Data Buffer
- · Two-Level Deep, FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit mode with Address Detect (9th bit = 1)
- · Transmit and Receive Interrupts
- · Loopback mode for Diagnostic Support
- · Support for Sync and Break Characters
- · Supports Automatic Baud Rate Detection
- · IrDA Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA[®] Support

A simplified block diagram of the UART module is shown in Figure 18-1. The UART module consists of these important hardware elements:

- · Baud Rate Generator
- Asynchronous Transmitter
- · Asynchronous Receiver





REGISTER 18-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0, HSC	R-1, HSC
UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1, HSC	R-0, HSC	R-0, HSC	R/C-0, HS	R-0, HSC
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0

Legend: HC = Hardware Clearable bit

HS = Hardware Settable bit C = Clearable bit HSC = Hardware Settable/Clearable bit R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15,13 UTXISEL<1:0>: UARTx Transmission Interrupt Mode Selection bits

- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14 UTXINV: IrDA® Encoder Transmit Polarity Inversion bit

If IREN = 0:

- 1 = UxTX Idle '0'
- 0 = UxTX Idle '1'

If IREN = $\underline{1}$:

- 1 = UxTX Idle '1'
- 0 = UxTX Idle '0'

bit 12 **Unimplemented:** Read as '0'

- bit 11 UTXBRK: UARTx Transmit Break bit
 - 1 = Sends Sync Break on next transmission Start bit, followed by twelve '0' bits; followed by Stop bit; cleared by hardware upon completion
 - 0 = Sync Break transmission is disabled or completed

bit 10 UTXEN: UARTx Transmit Enable bit

- 1 = Transmit is enabled; UxTX pin is controlled by UARTx
- 0 = Transmit is disabled; any pending transmission is aborted and the buffer is reset. UxTX pin is controlled by the PORT register.

bit 9 UTXBF: UARTx Transmit Buffer Full Status bit (read-only)

- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)

- 1 = Transmit Shift Register is empty and the transmit buffer is empty (the last transmission has completed)
- 0 = Transmit Shift Register is not empty; a transmission is in progress or queued

bit 7-6 URXISEL<1:0>: UARTx Receive Interrupt Mode Selection bits

- 11 = Interrupt is set on the RSR transfer, making the receive buffer full (i.e., has 2 data characters)
- 10 = Reserved
- 01 = Reserved
- 00 = Interrupt is set when any character is received and transferred from the RSR to the receive buffer; receive buffer has one or more characters

22.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

Note:

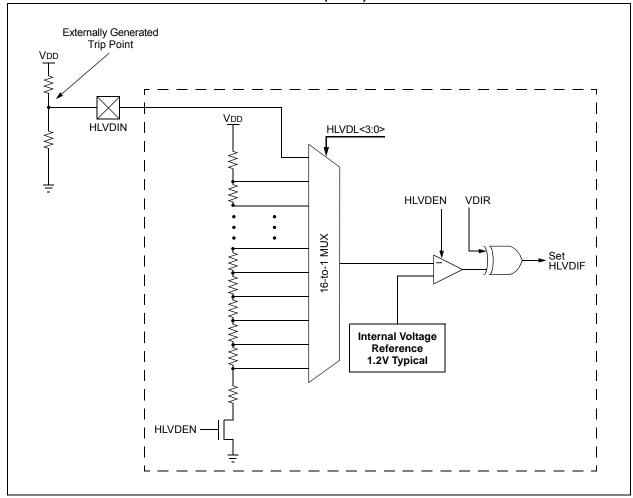
This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the High/Low-Voltage Detect, refer to the "dsPIC33/PIC24 Family Reference Manual", "High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)" (DS39725).

The High/Low-Voltage Detect module (HLVD) is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change.

An interrupt flag is set if the device experiences an excursion past the trip point in the direction of change. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

The HLVD Control register (see Register 22-1) completely controls the operation of the HLVD module. This allows the circuitry to be "turned off" by the user under software control, which minimizes the current consumption for the device.

FIGURE 22-1: HIGH/LOW-VOLTAGE DETECT (HLVD) MODULE BLOCK DIAGRAM



23.3 Unique ID

A read-only Unique ID value is stored at addresses, 800802h through 800808h. This factory programmed value is unique to each microcontroller produced in the PIC24F16KL402 family. To access this region, use Table Read instructions or Program Space Visibility.

To ensure a globally Unique ID across other Microchip microcontroller families, the "Unique ID" value should be further concatenated with the family and Device ID values stored at address, FF0000h.

REGISTER 23-8: DEVID: DEVICE ID REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 23							bit 16

R	R	R	R	R	R	R	R
FAMID7	FAMID6	FAMID5	FAMID4	FAMID3	FAMID2	FAMID1	FAMID0
bit 15							bit 8

R	R	R	R	R	R	R	R
DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 23-16 Unimplemented: Read as '0'

bit 15-8 **FAMID<7:0>:** Device Family Identifier bits

01001011 = PIC24F16KL402 family

bit 7-0 **DEV<7:0>:** Individual Device Identifier bits

00000001 = PIC24F04KL100

00000010 = PIC24F04KL101

00000101 = PIC24F08KL200 00000110 = PIC24F08KL201

00001010 = PIC24F08KL301

00000000 = PIC24F08KL302

00001110 = PIC24F08KL401

00000100 = PIC24F08KL402

00011110 = PIC24F16KL401

00010100 = PIC24F16KL402

TABLE 26-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHA	ARACTI	ERISTICS	Standard Operating te		-40°C ≤	≤ TA ≤ +8	o 3.6V 5°C for Industrial 25°C for Extended		
Param No.	Sym	Characteristic	Min Typ ⁽¹⁾ Max Units Conditions						
	VIL	Input Low Voltage ⁽⁴⁾							
DI10		I/O Pins	Vss	_	0.2 Vdd	V			
DI15		MCLR	Vss	_	0.2 VDD	V			
DI16		OSCI (XT mode)	Vss	_	0.2 Vdd	V			
DI17		OSCI (HS mode)	Vss	_	0.2 Vdd	V			
DI18		I/O Pins with I ² C™ Buffer	Vss	_	0.3 VDD	V	SMBus disabled		
DI19		I/O Pins with SMBus Buffer	Vss	_	0.8	V	SMBus enabled		
DI20	ViH	Input High Voltage ^(4,5) I/O Pins: with Analog Functions Digital Only	0.8 Vdd 0.8 Vdd		Vdd Vdd	V			
DI25		MCLR	0.8 VDD	_	Vdd	V			
DI26		OSCI (XT mode)	0.7 VDD	_	VDD	V			
DI27		OSCI (HS mode)	0.7 VDD	_	VDD	V			
DI28		I/O Pins with I ² C Buffer: with Analog Functions Digital Only	0.7 VDD 0.7 VDD		Vdd Vdd	V V			
DI29		I/O Pins with SMBus	2.1	_	VDD	V	$2.5V \le VPIN \le VDD$		
DI30	ICNPU	CNx Pull-up Current	50	250	500	μA	VDD = 3.3V, VPIN = VSS		
DI31	IPU	Maximum Load Current for Digital High Detection	_	_	30	μA	VDD = 2.0V		
		w/Internal Pull-up	_	_	1000	μΑ	VDD = 3.3V		
	lı∟	Input Leakage Current ^(2,3)							
DI50		I/O Ports	_	0.050	±0.100	μΑ	Vss ≤ VPIN ≤ VDD, Pin at high-impedance		
DI51		VREF+, VREF-, ANO, AN1	_	0.300	±0.500	μΑ	Vss ≤ VPIN ≤ VDD, Pin at high-impedance		

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

- 3: Negative current is defined as current sourced by the pin.
- 4: Refer to Table 1-4 and Table 1-5 for I/O pin buffer types.
- **5:** VIH requirements are met when the internal pull-ups are enabled.

^{2:} The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

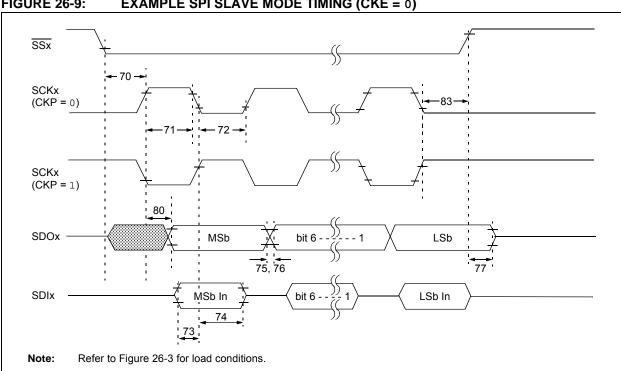


FIGURE 26-9: EXAMPLE SPI SLAVE MODE TIMING (CKE = 0)

TABLE 26-29: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING, CKE = 0)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	SSx ↓ to SCKx ↓ or SCKx ↑ Input		3 Tcy		ns	
70A	TssL2WB	SSx to Write to SSPxBUF		3 Tcy		ns	
71	TscH	SCKx Input High Time	Continuous	1.25 Tcy + 30	_	ns	
71A		(Slave mode)	Single Byte	40	_	ns	(Note 1)
72	TscL	SCKx Input Low Time	Continuous	1.25 Tcy + 30	_	ns	
72A		(Slave mode)	Single Byte	40	_	ns	(Note 1)
73	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx	20	_	ns		
73A	Тв2в	Last Clock Edge of Byte 1 to the First Clock	ck Edge of Byte 2	1.5 Tcy + 40	_	ns	(Note 2)
74	TscH2DIL, TscL2DIL	Hold Time of SDIx Data Input to SCKx I	Edge	40		ns	
75	TDOR	SDOx Data Output Rise Time		_	25	ns	
76	TDOF	SDOx Data Output Fall Time		_	25	ns	
77	TssH2DoZ	SSx ↑ to SDOx Output High-Impedance	;	10	50	ns	
80	TscH2DoV, TscL2DoV	SDOx Data Output Valid after SCKx Edge		_	50	ns	
83	TscH2ssH, TscL2ssH	SSx ↑ after SCKx Edge		1.5 Tcy + 40	_	ns	
	Fsck	SCKx Frequency		_	10	MHz	

Requires the use of Parameter 73A. Note 1:

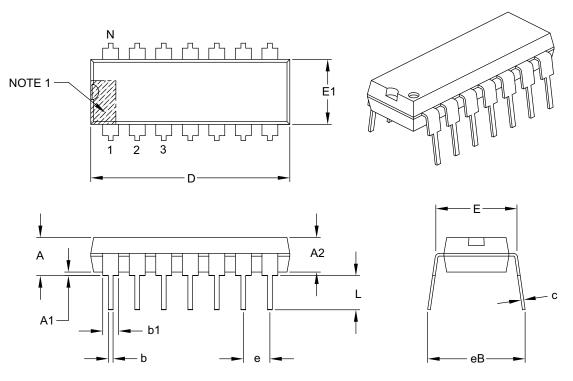
2: Only if Parameters 71A and 72A are used.

27.2 Package Details

The following sections give the technical details of the packages.

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES	
Dimensi	on Limits	MIN	NOM	MAX
Number of Pins	N		14	
Pitch	е		.100 BSC	
Top to Seating Plane	Α	_	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	_	_
Shoulder to Shoulder Width	Е	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	С	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	_	.430

Notes

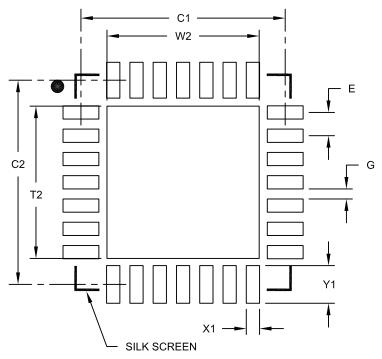
- 1. Pin 1 visual index feature may vary, but must be located with the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS				
Dimension	Limits	MIN	NOM	MAX	
Contact Pitch	Е		0.65 BSC		
Optional Center Pad Width	W2			4.25	
Optional Center Pad Length	T2			4.25	
Contact Pad Spacing	C1		5.70		
Contact Pad Spacing	C2		5.70		
Contact Pad Width (X28)	X1			0.37	
Contact Pad Length (X28)	Y1			1.00	
Distance Between Pads	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

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