Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f08kl301-i-p

TABLE 1-2: DEVICE FEATURES FOR PIC24F16KL40X/30X DEVICES

Features	PIC24F16KL402	PIC24F08KL402	PIC24F08KL302	PIC24F16KL401	PIC24F08KL401	PIC24F08KL301
Operating Frequency	DC – 32 MHz					
Program Memory (bytes)	16K	8K	8K	16K	8K	8K
Program Memory (instructions)	5632	2816	2816	5632	2816	2816
Data Memory (bytes)	1024	1024	1024	1024	1024	1024
Data EEPROM Memory (bytes)	512	512	256	512	512	256
Interrupt Sources (soft vectors/NMI traps)	31 (27/4)	31 (27/4)	30 (26/4)	31 (27/4)	31 (27/4)	30 (26/4)
I/O Ports	PORTA<7:0> PORTB<15:0>			PORTA<6:0> PORTB<15:12,9:7,4,2:0>		
Total I/O Pins	24			18		
Timers (8/16-bit)	2/2	2/2	2/2	2/2	2/2	2/2
Capture/Compare/PWM modules:						
Total	3	3	3	3	3	3
Enhanced CCP	1	1	1	1	1	1
Input Change Notification Interrupt	23	23	23	17	17	17
Serial Communications:						
UART	2	2	2	2	2	2
MSSP	2	2	2	2	2	2
10-Bit Analog-to-Digital Module (input channels)	12	12	—	12	12	—
Analog Comparators	2	2	2	2	2	2
Resets (and delays)	POR, BOR, RESET Instruction, $\overline{\text{MCLR}}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)					
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations					
Packages	28-Pin SPDIP/SSOP/SOIC/QFN			20-Pin PDIP/SSOP/SOIC/QFN		

TABLE 1-5: PIC24F16KL20X/10X FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Buffer	Description
	20-Pin PDIP/ SSOP/ SOIC	20-Pin QFN	14-Pin PDIP/ TSSOP			
SCK1	15	12	8	I/O	ST	MSSP1 SPI Serial Input/Output Clock
SCL1	12	9	8	I/O	I^2C	MSSP1 I^2C Clock Input/Output
SCLKI	10	7	12	I	ST	Digital Secondary Clock Input
SDA1	13	10	9	I/O	I^2C	MSSP1 I^2C Data Input/Output
SDI1	17	14	11	I	ST	MSSP1 SPI Serial Data Input
SDO1	16	13	9	O	—	MSSP1 SPI Serial Data Output
SOSCI	9	6	11	I	ANA	Secondary Oscillator Input
SOSCO	10	7	12	O	ANA	Secondary Oscillator Output
$\overline{SS1}$	12	9	12	O	—	SPI1 Slave Select
T1CK	13	10	9	I	ST	Timer1 Clock
T3CK	18	15	12	I	ST	Timer3 Clock
T3G	6	3	11	I	ST	Timer3 External Gate Input
$\overline{U1CTS}$	12	9	8	I	ST	UART1 Clear-to-Send Input
$\overline{U1RTS}$	13	10	9	O	—	UART1 Request-to-Send Output
U1RX	6	3	12	I	ST	UART1 Receive
U1TX	11	8	11	O	—	UART1 Transmit
ULPWU	3	1	3	I	ANA	Ultra Low-Power Wake-up Input
V_{DD}	20	17	14	P	—	Positive Supply for Peripheral Digital Logic and I/O Pins
V_{REF+}	2	19	2	I	ANA	A/D Reference Voltage Input (+)
V_{REF-}	3	20	3	I	ANA	A/D Reference Voltage Input (-)
V_{SS}	19	16	13	P	—	Ground Reference for Logic and I/O Pins

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C = I^2C™/SMBus input buffer

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC24F16KL402 family of 16-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Power Supply Pins"**)
- All AVDD and AVSS pins, regardless of whether or not the analog device features are used
  (see **Section 2.2 "Power Supply Pins"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.3 "Master Clear (MCLR) Pin"**)

These pins must also be connected if they are being used in the end application:

- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.4 "ICSP Pins"**)
- OSCI and OSCO pins when an external oscillator source is used
  (see **Section 2.5 "External Oscillator Pins"**)

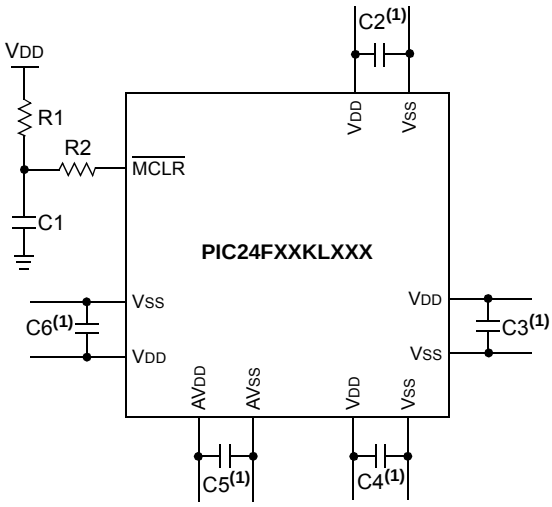
Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for analog modules is implemented

Note:	The AVDD and AVSS pins must always be connected, regardless of whether any of the analog modules are being used.

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS



Key (all values are recommendations):

C1 through C6: 0.1 μF, 20V ceramic

R1: 10 kΩ

R2: 100Ω to 470Ω

Note 1: The example shown is for a PIC24F device with five VDD/VSS and AVDD/AVSS pairs. Other devices may have more or less pairs; adjust the number of decoupling capacitors appropriately.

TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	—	—	—	—	—	—	—	—	—	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	NVMIF	—	AD1IF	U1TXIF	U1RXIF	—	—	T3IF	T2IF	CCP2IF	—	—	T1IF	CCP1IF	—	INT0IF	0000
IFS1	0086	U2TXIF	U2RXIF	INT2IF	—	T4IF(1)	—	CCP3IF(1)	—	—	—	—	INT1IF	CNIF	CMIF	BCL1IF	SSP1IF	0000
IFS2	0088	—	—	—	—	—	—	—	—	—	—	T3GIF	—	—	—	—	—	0000
IFS3	008A	—	—	—	—	—	—	—	—	—	—	—	—	—	BCL2IF(1)	SSP2IF(1)	—	0000
IFS4	008C	—	—	—	—	—	—	—	HLVDIF	—	—	—	—	—	U2ERIF	U1ERIF	—	0000
IFS5	008E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ULPWUIF	0000
IEC0	0094	NVMIE	—	AD1IE	U1TXIE	U1RXIE	—	—	T3IE	T2IE	CCP2IE	—	—	T1IE	CCP1IE	—	INT0IE	0000
IEC1	0096	U2TXIE	U2RXIE	INT2IE	—	T4IE(1)	—	CCP3IE(1)	—	—	—	—	INT1IE	CNIE	CMIE	BCL1IE	SSP1IE	0000
IEC2	0098	—	—	—	—	—	—	—	—	—	—	T3GIE	—	—	—	—	—	0000
IEC3	009A	—	—	—	—	—	—	—	—	—	—	—	—	—	BCL2IE(1)	SSP2IE(1)	—	0000
IEC4	009C	—	—	—	—	—	—	—	HLVDIE	—	—	—	—	—	U2ERIE	U1ERIE	—	0000
IEC5	009E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ULPWUIE	0000
IPC0	00A4	—	T1IP2	T1IP1	T1IP0	—	CCP1IP2	CCP1IP1	CCP1IP0	—	—	—	—	—	INT0IP2	INT0IP1	INT0IP0	4404
IPC1	00A6	—	T2IP2	T2IP1	T2IP0	—	CCP2IP2	CCP2IP1	CCP2IP0	—	—	—	—	—	—	—	—	4400
IPC2	00A8	—	U1RXIP2	U1RXIP1	U1RXIP0	—	—	—	—	—	—	—	—	—	T3IP2	T3IP1	T3IP0	4004
IPC3	00AA	—	NVMIP2	NVMIP1	NVMIP0	—	—	—	—	—	AD1IP2	AD1IP1	AD1IP0	—	U1TXIP2	U1TXIP1	U1TXIP0	4044
IPC4	00AC	—	CNIP2	CNIP1	CNIP0	—	CMIP2	CMIP1	CMIP0	—	BCL1IP2	BCL1IP1	BCL1IP0	—	SSP1IP2	SSP1IP1	SS1IP0	4444
IPC5	00AE	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0	0004
IPC6	00B0	—	T4IP2(1)	T4IP1(1)	T4IP0(1)	—	—	—	—	—	CCP3IP2(1)	CCP3IP1(1)	CCP3IP0(1)	—	—	—	—	4040
IPC7	00B2	—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0	—	INT2IP2	INT2IP1	INT2IP0	—	—	—	—	4440
IPC9	00B6	—	—	—	—	—	—	—	—	—	T3GIP2	T3GIP1	T3GIP0	—	—	—	—	0040
IPC12	00BC	—	—	—	—	—	BCL2IP2(1)	BCL2IP1(1)	BCL2IP0(1)	—	SSP2IP2(1)	SSP2IP1(1)	SSP2IP0(1)	—	—	—	—	0440
IPC16	00C4	—	—	—	—	—	U2ERIP2	U2ERIP1	U2ERIP0	—	U1ERIP2	U1ERIP1	U1ERIP0	—	—	—	—	0440
IPC18	00C8	—	—	—	—	—	—	—	—	—	—	—	—	—	HLVDIP2	HLVDIP1	HLVDIP0	0004
IPC20	00CC	—	—	—	—	—	—	—	—	—	—	—	—	—	ULPWUIP2	ULPWUIP1	ULPWUIP0	0004
INTTREG	00E0	CPUIRQ	r	VHOLD	—	ILR3	ILR2	ILR1	ILR0	—	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0	0000

Legend: — = unimplemented, read as '0', r = reserved. Reset values are shown in hexadecimal.

Note 1: These bits are unimplemented on PIC24FXXKL10X and PIC24FXXKL20X family devices; read as '0'.

TABLE 4-8: MSSP REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SSP1BUF	0200	—	—	—	—	—	—	—	—	MSSP1 Receive Buffer/Transmit Register								00xx
SSP1CON1	0202	—	—	—	—	—	—	—	—	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000
SSP1CON2	0204	—	—	—	—	—	—	—	—	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000
SSP1CON3	0206	—	—	—	—	—	—	—	—	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
SSP1STAT	0208	—	—	—	—	—	—	—	—	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000
SSP1ADD	020A	—	—	—	—	—	—	—	—	MSSP1 Address Register (I^2C™ Slave Mode) MSSP1 Baud Rate Reload Register (I^2C Master Mode)								0000
SSP1MSK	020C	—	—	—	—	—	—	—	—	MSSP1 Address Mask Register (I^2C Slave Mode)								00FF
SSP2BUF(1)	0210	—	—	—	—	—	—	—	—	MSSP2 Receive Buffer/Transmit Register								00xx
SSP2CON1(1)	0212	—	—	—	—	—	—	—	—	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000
SSP2CON2(1)	0214	—	—	—	—	—	—	—	—	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000
SSP2CON3(1)	0216	—	—	—	—	—	—	—	—	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
SSP2STAT(1)	0218	—	—	—	—	—	—	—	—	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000
SSP2ADD(1)	021A	—	—	—	—	—	—	—	—	MSSP2 Address Register (I^2C Slave Mode) MSSP2 Baud Rate Reload Register (I^2C Master Mode)								0000
SSP2MSK(1)	021C	—	—	—	—	—	—	—	—	MSSP2 Address Mask Register (I^2C Slave Mode)								00FF

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These bits and/or registers are unimplemented on PIC24FXXKL10X and PIC24FXXKL20X family devices; read as '0'.

TABLE 4-9: UART REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	0228	Baud Rate Generator Prescaler Register																0000
U2MODE	0230	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	—	—	—	—	—	—	—	UART2 Transmit Register									xxxx
U2RXREG	0236	—	—	—	—	—	—	—	UART2 Receive Register									0000
U2BRG	0238	Baud Rate Generator Prescaler Register																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

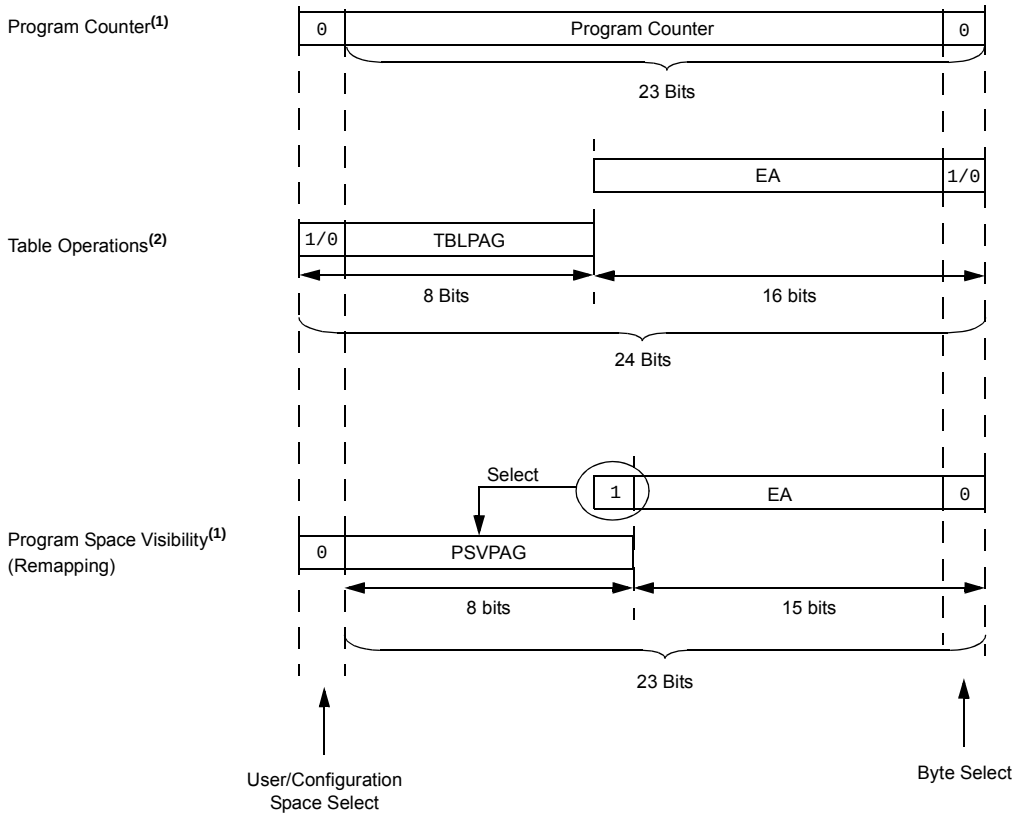
TABLE 4-20: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		<23>	<22:16>	<15>	<14:1>	<0>
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx xxxx		xxxx xxxx xxxx xxxx		
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		1xxx xxxx		xxxx xxxx xxxx xxxx		
Program Space Visibility (Block Remap/Read)	User	0	PSVPAG<7:0>(2)		Data EA<14:0>(1)	
		0	xxxx xxxx		xxx xxxx xxxx xxxx	

Note 1: Data EA<15> is always '1' in this case, but is not used in calculating the program space address. Bit 15 of the address is PSVPAG<0>.

2: PSVPAG can have only two values ('00' to access program memory and FF to access data EEPROM) on PIC24F16KL402 family devices.

FIGURE 4-5: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



Note 1: The LSb of program space addresses is always fixed as '0' in order to maintain word alignment of data in the program and data spaces.

2: Table operations are not required to be word-aligned. Table read operations are permitted in the configuration memory space.

6.4.3 READING THE DATA EEPROM

To read a word from data EEPROM, the Table Read instruction is used. Since the EEPROM array is only 16 bits wide, only the TBLRDL instruction is needed. The read operation is performed by loading TBLPAG and WREG with the address of the EEPROM location followed by a TBLRDL instruction.

A typical read sequence using the Table Pointer management (`builtin_tblpage` and `builtin_tbloffset`) and Table Read (`builtin_tblrdl`) procedures from the C30 compiler library is provided in Example 6-5.

Program Space Visibility (PSV) can also be used to read locations in the data EEPROM.

EXAMPLE 6-5: READING THE DATA EEPROM USING THE TBLRD COMMAND

```
int __attribute__ ((space(eedata))) eeData = 0x1234;     // Global variable located in EEPROM
    int data;                                            // Data read from EEPROM
    unsigned int offset;

    // Set up a pointer to the EEPROM location to be erased
    TBLPAG = __builtin_tblpage(&eeData);                 // Initialize EE Data page pointer
    offset = __builtin_tbloffset(&eeData);               // Initizlize lower word of address
    data =   __builtin_tblrdl(offset);                   // Write EEPROM data to write latch
```

REGISTER 8-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
NSTDIS	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
—	—	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled

bit 14-5 **Unimplemented:** Read as ‘0’

bit 4 **MATHERR:** Arithmetic Error Trap Status bit
1 = Overflow trap has occurred
0 = Overflow trap has not occurred

bit 3 **ADDRERR:** Address Error Trap Status bit
1 = Address error trap has occurred
0 = Address error trap has not occurred

bit 2 **STKERR:** Stack Error Trap Status bit
1 = Stack error trap has occurred
0 = Stack error trap has not occurred

bit 1 **OSCFAIL:** Oscillator Failure Trap Status bit
1 = Oscillator failure trap has occurred
0 = Oscillator failure trap has not occurred

bit 0 **Unimplemented:** Read as ‘0’

REGISTER 8-12: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	U-0
U2TXIE(1)	U2RXIE(1)	INT2IE	—	T4IE(1)	—	CCP3IE(1)	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT1IE	CNIE	CMIE	BCL1IE	SSP1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **U2TXIE:** UART2 Transmitter Interrupt Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 14 **U2RXIE:** UART2 Receiver Interrupt Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13 **INT2IE:** External Interrupt 2 Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12 **Unimplemented:** Read as '0'

bit 11 **T4IE:** Timer4 Interrupt Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 10 **Unimplemented:** Read as '0'

bit 9 **CCP3IE:** Capture/Compare/PWM3 Interrupt Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 8-5 **Unimplemented:** Read as '0'

bit 4 **INT1IE:** External Interrupt 1 Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 3 **CNIE:** Input Change Notification Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **CMIE:** Comparator Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **BCL1IE:** MSSP1 I^2C™ Bus Collision Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **SSP1IE:** MSSP1 SPI/I^2C Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

Note 1: These bits are unimplemented on PIC24FXXKL10X and PIC24FXXKL20X devices.

REGISTER 8-15: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	HLVDIE
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0
—	—	—	—	—	U2ERIE(1)	U1ERIE	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **HLVDIE:** High/Low-Voltage Detect Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **U2ERIE:** UART2 Error Interrupt Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **U1ERIE:** UART1 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit is unimplemented on PIC24FXXKL10X and PIC24FXXKL20X devices.

REGISTER 8-16: IEC5: INTERRUPT ENABLE CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	ULPWUIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-1 **Unimplemented:** Read as '0'

bit 0 **ULPWUIE:** Ultra Low-Power Wake-up Interrupt Enable Bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

REGISTER 8-18: IPC1: INTERRUPT PRIORITY CONTROL REGISTER 1

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T2IP2	T2IP1	T2IP0	—	CCP2IP2	CCP2IP1	CCP2IP0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **T2IP<2:0>:** Timer2 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **CCP2IP<2:0>:** Capture/Compare/PWM2 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 8-21: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CNIP2	CNIP1	CNIP0	—	CMIP2	CMIP1	CMIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	BCL1IP2	BCL1IP1	BCL1IP0	—	SSP1IP2	SSP1IP1	SSP1IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CNIP<2:0>:** Input Change Notification Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **CMIP<2:0>:** Comparator Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **BCL1IP<2:0>:** MSSP1 I^2C™ Bus Collision Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **SSP1IP<2:0>:** MSSP1 SPI/I^2C Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-22: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **INT1IP<2:0>:** External Interrupt 1 Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

REGISTER 17-6: SSPxCON3: MSSPx CONTROL REGISTER 3 (SPI MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ACKTIM	PCIE	SCIE	BOEN(1)	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **ACKTIM:** Acknowledge Time Status bit (I^2C™ mode only)
Unused in SPI mode.

bit 6 **PCIE**: Stop Condition Interrupt Enable bit (I^2C mode only)
Unused in SPI mode.

bit 5 **SCIE**: Start Condition Interrupt Enable bit (I^2C mode only)
Unused in SPI mode.

bit 4 **BOEN:** Buffer Overwrite Enable bit(1)
In SPI Slave mode:
1 = SSPxBUF updates every time that a new data byte is shifted in, ignoring the BF bit
0 = If a new byte is received with the BF bit of the SSPxSTAT register already set, the SSPOV bit of the SSPxCON1 register is set and the buffer is not updated

bit 3 **SDAHT:** SDAx Hold Time Selection bit (I^2C mode only)
Unused in SPI mode.

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
Unused in SPI mode.

bit 1 **AHEN:** Address Hold Enable bit (I^2C Slave mode only)
Unused in SPI mode.

bit 0 **DHEN:** Data Hold Enable bit (Slave mode only)
Unused in SPI mode.

Note 1: For daisy-chained SPI operation: Allows the user to ignore all but the last received byte. SSPOV is still set when a new byte is received and BF = 1, but hardware continues to write the most recent byte to SSPxBUF.

18.2 Transmitting in 8-Bit Data Mode

1. Set up the UART:
   a) Write appropriate values for data, parity and Stop bits.
   b) Write appropriate baud rate value to the UxBRG register.
   c) Set up transmit and receive interrupt enable and priority bits.
2. Enable the UART.
3. Set the UTXEN bit (causes a transmit interrupt, two cycles after being set).
4. Write data byte to lower byte of UxTXREG word. The value will be immediately transferred to the Transmit Shift Register (TSR) and the serial bit stream will start shifting out with the next rising edge of the baud clock.
5. Alternately, the data byte may be transferred while UTXEN = 0 and then, the user may set UTXEN. This will cause the serial bit stream to begin immediately, because the baud clock will start from a cleared state.
6. A transmit interrupt will be generated as per interrupt control bit, UTXISELx.

18.3 Transmitting in 9-Bit Data Mode

1. Set up the UART (as described in **Section 18.2 "Transmitting in 8-Bit Data Mode"**).
2. Enable the UART.
3. Set the UTXEN bit (causes a transmit interrupt, two cycles after being set).
4. Write UxTXREG as a 16-bit value only.
5. A word write to UxTXREG triggers the transfer of the 9-bit data to the TSR. The serial bit stream will start shifting out with the first rising edge of the baud clock.
6. A transmit interrupt will be generated as per the setting of control bit, UTXISELx.

18.4 Break and Sync Transmit Sequence

The following sequence will send a message frame header made up of a Break, followed by an auto-baud Sync byte.

1. Configure the UART for the desired mode.
2. Set UTXEN and UTXBRK – sets up the Break character.
3. Load the UxTXREG with a dummy character to initiate transmission (value is ignored).
4. Write '55h' to UxTXREG – loads the Sync character into the transmit FIFO.
5. After the Break has been sent, the UTXBRK bit is reset by hardware. The Sync character now transmits.

18.5 Receiving in 8-Bit or 9-Bit Data Mode

1. Set up the UART (as described in **Section 18.2 "Transmitting in 8-Bit Data Mode"**).
2. Enable the UART.
3. A receive interrupt will be generated when one or more data characters have been received as per interrupt control bit, URXISELx.
4. Read the OERR bit to determine if an overrun error has occurred. The OERR bit must be reset in software.
5. Read UxRXREG.

The act of reading the UxRXREG character will move the next character to the top of the receive FIFO, including a new set of PERR and FERR values.

18.6 Operation of $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Control Pins

UARTx Clear-to-Send ($\overline{\text{UxCTS}}$) and Request-to-Send ($\overline{\text{UxRTS}}$) are the two hardware-controlled pins that are associated with the UART module. These two pins allow the UART to operate in Simplex and Flow Control modes. They are implemented to control the transmission and reception between the Data Terminal Equipment (DTE). The UEN<1:0> bits in the UxMODE register configure these pins.

18.7 Infrared Support

The UART module provides two types of infrared UART support: one is the IrDA clock output to support an external IrDA encoder and decoder device (legacy module support), and the other is the full implementation of the IrDA encoder and decoder.

As the IrDA modes require a 16x baud clock, they will only work when the BRGH bit (UxMODE<3>) is '0'.

18.7.1 EXTERNAL IrDA SUPPORT – IrDA CLOCK OUTPUT

To support external IrDA encoder and decoder devices, the UxBCLK pin (same as the $\overline{\text{UxRTS}}$ pin) can be configured to generate the 16x baud clock. When UEN<1:0> = 11, the UxBCLK pin will output the 16x baud clock if the UART module is enabled; it can be used to support the IrDA codec chip.

18.7.2 BUILT-IN IrDA ENCODER AND DECODER

The UART has full implementation of the IrDA encoder and decoder as part of the UART module. The built-in IrDA encoder and decoder functionality is enabled using the IREN bit (UxMODE<12>). When enabled (IREN = 1), the receive pin (UxRX) acts as the input from the infrared receiver. The transmit pin (UxTX) acts as the output to the infrared transmitter.

REGISTER 19-2: AD1CON2: A/D CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0
VCFG2	VCFG1	VCFG0	OFFCAL(1)	—	CSCNA	—	—
bit 15							bit 8

R-x	U-0	R/W-0	R/W-0	R/W-0	R/W-0	r-0	R/W-0
r	—	SMPI3	SMPI2	SMPI1	SMPI0	r	ALTS
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

VCFG<2:0>	VR+	VR-
000	AVDD	AVSS
001	External VREF+ pin	AVSS
010	AVDD	External VREF- pin
011	External VREF+ pin	External VREF- pin
1xx	AVDD	AVSS

bit 12 **OFFCAL:** Offset Calibration bit(1)
1 = Conversions to get the offset calibration value
0 = Conversions to get the actual input value

bit 11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** Scan Input Selections for MUX A Input Multiplexer bit
1 = Scans inputs
0 = Does not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **Reserved:** Ignore this value

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits
1111 =
•
• = Reserved, do not use (may cause conversion data loss)
•
0010 =
0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **Reserved:** Always maintain as '0'

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses MUX A input multiplexer settings for the first sample, then alternates between MUX B and MUX A input multiplexer settings for all subsequent samples
0 = Always uses MUX A input multiplexer settings

Note 1: When the OFFCAL bit is set, inputs are disconnected and tied to AVSS. This sets the inputs of the A/D to zero. Then, the user can perform a conversion. Use of the Calibration mode is not affected by AD1PCFG contents nor channel input selection. Any analog input switches are disconnected from the A/D Converter in this mode. The conversion result is stored by the user software and used to compensate subsequent conversions. This can be done by adding the two's complement of the result obtained with the OFFCAL bit set to all normal A/D conversions.

NOTES:

REGISTER 20-1: CMxCON: COMPARATOR x CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R-0
CON	COE	CPOL	CLPWR	—	—	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1(1)	EVPOL0(1)	—	CREF	—	—	CCH1	CCH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12 **CLPWR:** Comparator Low-Power Mode Select bit
1 = Comparator operates in Low-Power mode
0 = Comparator does not operate in Low-Power mode

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
1 = Comparator event defined by EVPOL<1:0> has occurred; subsequent triggers and interrupts are disabled until the bit is cleared
0 = Comparator event has not occurred

bit 8 **COUT:** Comparator Output bit
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits(1)
11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/event/interrupt is generated on the high-to-low transition of the comparator output
01 = Trigger/event/Interrupt is generated on the low-to-high transition of the comparator output
00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Reference Select bits (non-inverting input)
1 = Non-inverting input connects to the internal CVREF voltage
0 = Non-inverting input connects to the CxINA pin

Note 1: If EVPOL<1:0> is set to a value other than '00', the first interrupt generated will occur on any transition of COUT, regardless of if it is a rising or falling edge. Subsequent interrupts will occur based on the EVPOLx bits setting.

2: Unimplemented on 14-pin (PIC24FXXKL100/200) devices.

TABLE 26-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

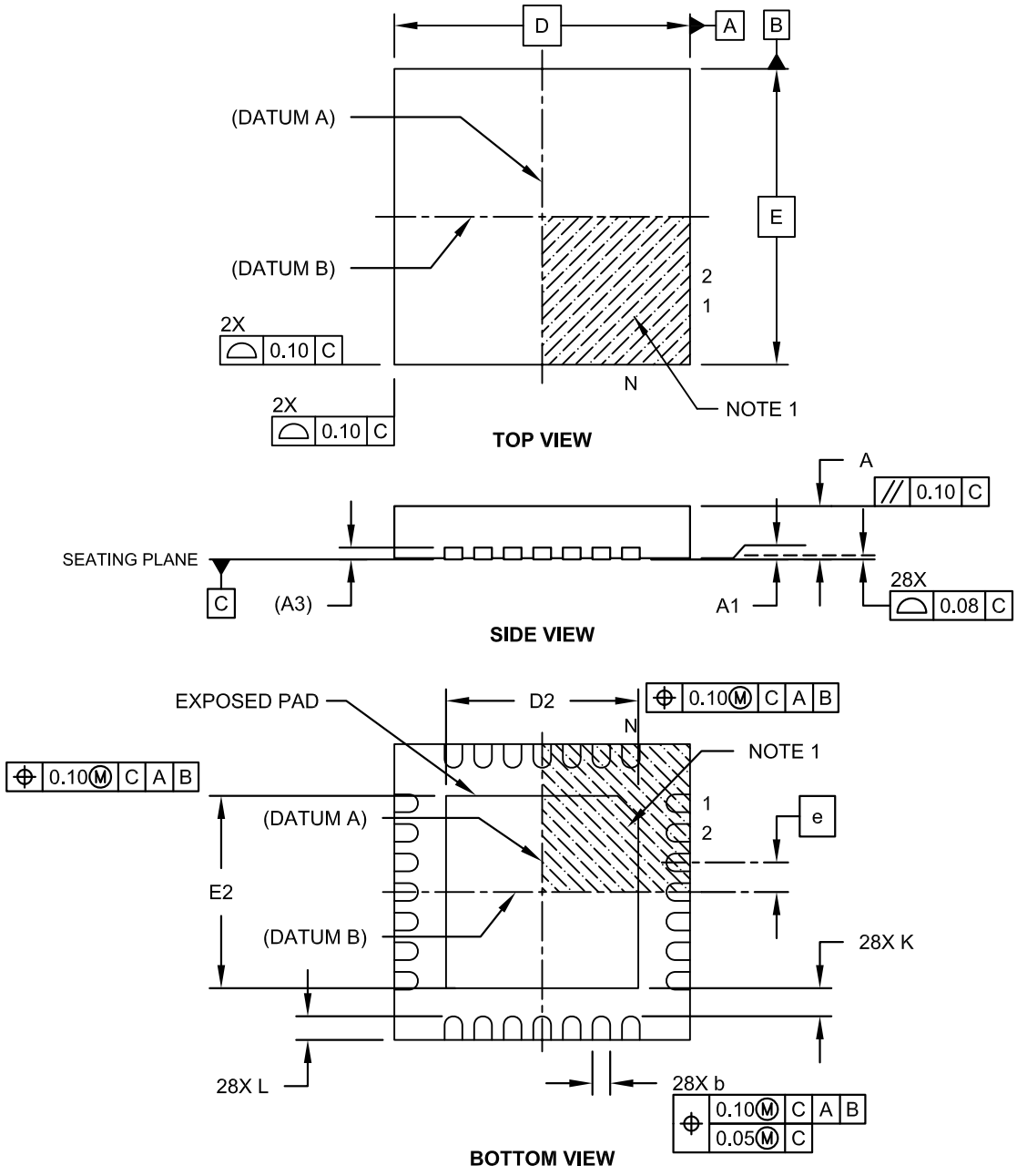
DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Power-Down Current (I_{PD})						
DC60	0.01	0.20	µA	-40°C	1.8V	Sleep Mode(2)
	0.03	0.20	µA	+25°C		
	0.06	0.87	µA	+60°C		
	0.20	1.35	µA	+85°C		
	—	8.00	µA	+125ºC		
	0.01	0.54	µA	-40°C	3.3V	
	0.03	0.54	µA	+25°C		
	0.08	1.68	µA	+60°C		
	0.25	2.45	µA	+85°C		
	—	10.00	µA	+125ºC		

Note 1: Data in the Typical column is at 3.3V, +25°C unless otherwise stated.

2: Base I_{PD} is measured with all peripherals and clocks disabled. All I/Os are configured as outputs and set low; PMDx bits are set to '1' and WDT, etc., are all disabled

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-140B Sheet 1 of 2