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#### Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24f08kl401-e-ss">https://www.e-xfl.com/product-detail/microchip-technology/pic24f08kl401-e-ss</a>

# PIC24F16KL402 FAMILY

## REGISTER 3-2: CORCON: CPU CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0	R/W-0	U-0	U-0
—	—	—	—	IPL3 <sup>(1)</sup>	PSV	—	—
bit 7							bit 0

<b>Legend:</b>	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

- bit 15-4      **Unimplemented:** Read as '0'
- bit 3      **IPL3:** CPU Interrupt Priority Level Status bit<sup>(1)</sup>  
             1 = CPU Interrupt Priority Level is greater than 7  
             0 = CPU Interrupt Priority Level is 7 or less
- bit 2      **PSV:** Program Space Visibility in Data Space Enable bit  
             1 = Program space is visible in data space  
             0 = Program space is not visible in data space
- bit 1-0      **Unimplemented:** Read as '0'

**Note 1:** User interrupts are disabled when IPL3 = 1.

## 3.3 Arithmetic Logic Unit (ALU)

The PIC24F ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU may affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array, or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

The PIC24F CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware division for a 16-bit divisor.

### 3.3.1 MULTIPLIER

The ALU contains a high-speed, 17-bit x 17-bit multiplier. It supports unsigned, signed or mixed sign operation in several Multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

# PIC24F16KL402 FAMILY

## 4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address, as shown in Figure 4-2.

Program memory addresses are always word-aligned on the lower word, and addresses are incremented or decremented by two during code execution. This arrangement also provides compatibility with data memory space addressing and makes it possible to access data in the program memory space.

## 4.1.2 HARD MEMORY VECTORS

All PIC24F devices reserve the addresses between 00000h and 000200h for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user at 000000h, with the actual address for the start of code at 000002h.

PIC24F devices also have two Interrupt Vector Tables (IVT), located from 000004h to 0000FFh and 000104h to 0001FFh. These vector tables allow each of the many device interrupt sources to be handled by separate ISRs. A more detailed discussion of the Interrupt Vector Tables is provided in **Section 8.1 “Interrupt Vector Table (IVT)”**.

## 4.1.3 DATA EEPROM

In the PIC24F16KL402 family, the data EEPROM is mapped to the top of the user program memory space, starting at address, 7FFE00, and expanding up to address, 7FFFFF.

The data EEPROM is organized as 16-bit wide memory and 256 words deep. This memory is accessed using Table Read and Table Write operations, similar to the user code memory.

## 4.1.4 DEVICE CONFIGURATION WORDS

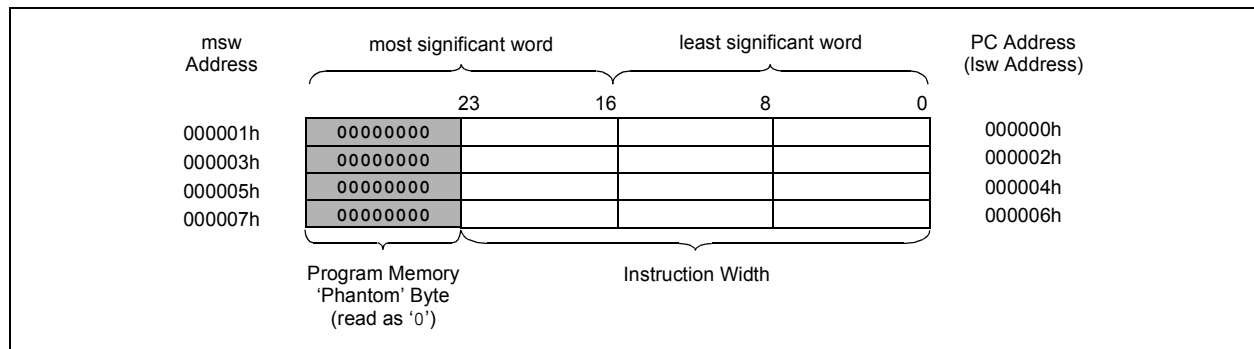
Table 4-1 provides the addresses of the device Configuration Words for the PIC24F16KL402 family. Their location in the memory map is shown in Figure 4-1.

For more information on device Configuration Words, see **Section 23.0 “Special Features”**.

**TABLE 4-1: DEVICE CONFIGURATION WORDS FOR PIC24F16KL402 FAMILY DEVICES**

Configuration Words	Configuration Word Addresses
FBS	F80000
FGS	F80004
FOSCSEL	F80006
FOSC	F80008
FWDT	F8000A
FPOR	F8000C
FICD	F8000E

**FIGURE 4-2: PROGRAM MEMORY ORGANIZATION**



# PIC24F16KL402 FAMILY

## 4.3.2 DATA ACCESS FROM PROGRAM MEMORY AND DATA EEPROM MEMORY USING TABLE INSTRUCTIONS

The **TBLRDL** and **TBLWTL** instructions offer a direct method of reading or writing the lower word of any address within the program memory without going through data space. It also offers a direct method of reading or writing a word of any address within data EEPROM memory. The **TBLRDH** and **TBLWTH** instructions are the only method to read or write the upper 8 bits of a program space word as data.

**Note:** The **TBLRDH** and **TBLWTH** instructions are not used while accessing data EEPROM memory.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two, 16-bit word-wide address spaces, residing side by side, each with the same address range. **TBLRDL** and **TBLWTL** access the space which contains the least significant data word, and **TBLRDH** and **TBLWTH** access the space which contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

1. **TBLRDL** (Table Read Low): In Word mode, it maps the lower word of the program space location ( $P<15:0>$ ) to a data address ( $D<15:0>$ ).

In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when the byte select is '1'; the lower byte is selected when it is '0'.

2. **TBLRDH** (Table Read High): In Word mode, it maps the entire upper word of a program address ( $P<23:16>$ ) to a data address. Note that  $D<15:8>$ , the 'phantom' byte, will always be '0'.

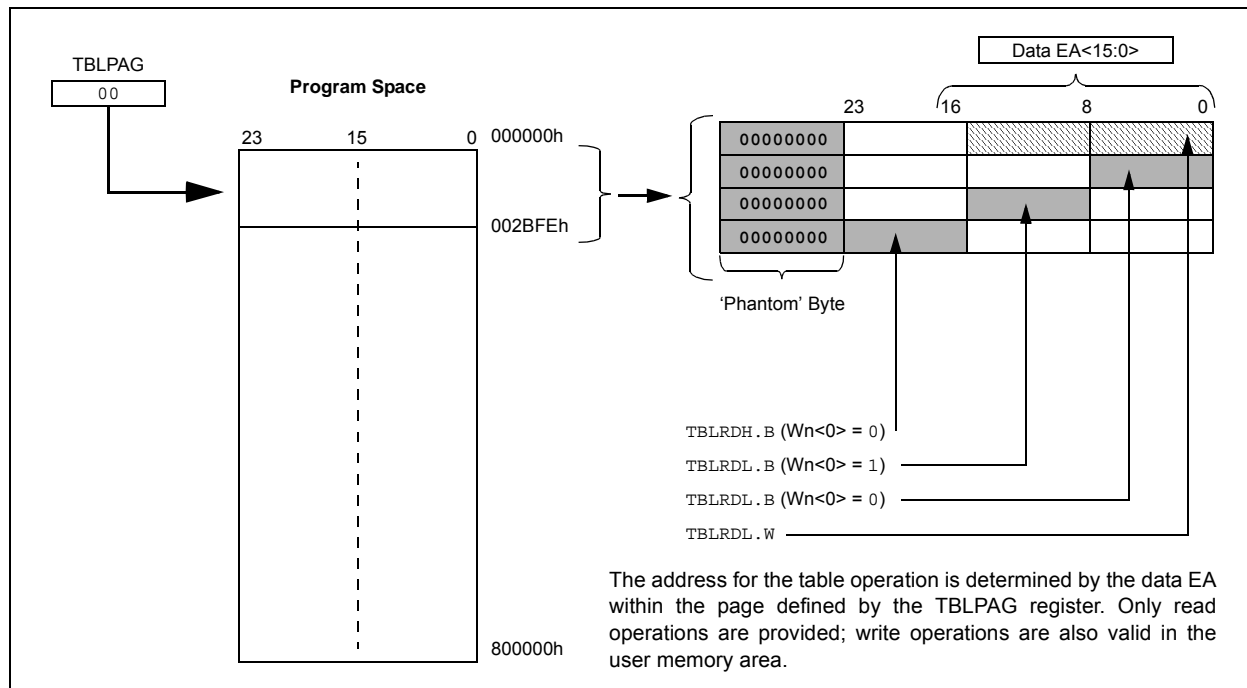
In Byte mode, it maps the upper or lower byte of the program word to  $D<7:0>$  of the data address, as above. Note that the data will always be '0' when the upper 'phantom' byte is selected (byte select = 1).

In a similar fashion, two table instructions, **TBLWTH** and **TBLWTL**, are used to write individual bytes or words to a program space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Memory Page Address register (**TBLPAG**). **TBLPAG** covers the entire program memory space of the device, including user and configuration spaces. When **TBLPAG<7> = 0**, the table page is located in the user memory space. When **TBLPAG<7> = 1**, the page is located in configuration space.

**Note:** Only Table Read operations will execute in the configuration memory space, and only then, in implemented areas, such as the Device ID. Table write operations are not allowed.

**FIGURE 4-6: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS**



## 6.0 DATA EEPROM MEMORY

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Data EEPROM, refer to the “*dsPIC33/PIC24 Family Reference Manual*”, “**Data EEPROM**” (DS39720).

The data EEPROM memory is a Nonvolatile Memory (NVM), separate from the program and volatile data RAM. Data EEPROM memory is based on the same Flash technology as program memory, and is optimized for both long retention and a higher number of erase/write cycles.

The data EEPROM is mapped to the top of the user program memory space, with the top address at program memory address, 7FFFFFFh. For PIC24FXXKL4XX devices, the size of the data EEPROM is 256 words (7FFE00h to 7FFFFFFh). For PIC24FXXKL3XX devices, the size of the data EEPROM is 128 words (7FFF00h to 7FFFFFFh). The data EEPROM is not implemented in PIC24F08KL20X or PIC24F04KL10X devices.

The data EEPROM is organized as 16-bit wide memory. Each word is directly addressable, and is readable and writable during normal operation over the entire VDD range.

Unlike the Flash program memory, normal program execution is not stopped during a data EEPROM program or erase operation.

The data EEPROM programming operations are controlled using the three NVM Control registers:

- NVMCON: Nonvolatile Memory Control Register
- NVMKEY: Nonvolatile Memory Key Register
- NVMADR: Nonvolatile Memory Address Register

### EXAMPLE 6-1: DATA EEPROM UNLOCK SEQUENCE

```
//Disable Interrupts For 5 instructions
asm volatile("disi #5");
//Issue Unlock Sequence
asm volatile ("mov #0x55, W0      \n"
              "mov W0, NVMKEY     \n"
              "mov #0xAA, W1      \n"
              "mov W1, NVMKEY     \n");
// Perform Write/Erase operations
asm volatile ("bset NVMCON, #WR  \n"
              "nop                \n"
              "nop                \n");
```

## 6.1 NVMCON Register

The NVMCON register (Register 6-1) is also the primary control register for data EEPROM program/erase operations. The upper byte contains the control bits used to start the program or erase cycle, and the flag bit to indicate if the operation was successfully performed. The lower byte of NVMCOM configures the type of NVM operation that will be performed.

## 6.2 NVMKEY Register

The NVMKEY is a write-only register that is used to prevent accidental writes or erasures of data EEPROM locations.

To start any programming or erase sequence, the following instructions must be executed first, in the exact order provided:

1. Write 55h to NVMKEY.
2. Write AAh to NVMKEY.

After this sequence, a write will be allowed to the NVMCON register for one instruction cycle. In most cases, the user will simply need to set the WR bit in the NVMCON register to start the program or erase cycle. Interrupts should be disabled during the unlock sequence.

The MPLAB® C30 C compiler provides a defined library procedure (`builtin_write_NVM`) to perform the unlock sequence. Example 6-1 illustrates how the unlock sequence can be performed with in-line assembly.

# PIC24F16KL402 FAMILY

## REGISTER 6-1: NVMCON: NONVOLATILE MEMORY CONTROL REGISTER

R/SO-0, HC	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	PGMONLY	—	—	—	—
bit 15				bit 8			

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ERASE	NVMOP5 <sup>(1)</sup>	NVMOP4 <sup>(1)</sup>	NVMOP3 <sup>(1)</sup>	NVMOP2 <sup>(1)</sup>	NVMOP1 <sup>(1)</sup>	NVMOP0 <sup>(1)</sup>
bit 7				bit 0			

<b>Legend:</b>	HC = Hardware Clearable bit	U = Unimplemented bit, read as '0'
R = Readable bit	W = Writable bit	SO = Settable Only bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

- bit 15      **WR:** Write Control bit (program or erase)  
1 = Initiates a data EEPROM erase or write cycle (can be set but not cleared in software)  
0 = Write cycle is complete (cleared automatically by hardware)
- bit 14      **WREN:** Write Enable bit (erase or program)  
1 = Enables an erase or program operation  
0 = No operation allowed (device clears this bit on completion of the write/erase operation)
- bit 13      **WRERR:** Flash Error Flag bit  
1 = A write operation is prematurely terminated (any  $\overline{\text{MCLR}}$  or WDT Reset during programming operation)  
0 = The write operation completed successfully
- bit 12      **PGMONLY:** Program Only Enable bit  
1 = Write operation is executed without erasing target address(es) first  
0 = Automatic erase-before-write; write operations are preceded automatically by an erase of target address(es)
- bit 11-7      **Unimplemented:** Read as '0'
- bit 6      **ERASE:** Erase Operation Select bit  
1 = Performs an erase operation when WR is set  
0 = Performs a write operation when WR is set
- bit 5-0      **NVMOP<5:0>:** Programming Operation Command Byte bits<sup>(1)</sup>  
Erase Operations (when ERASE bit is '1'):  
011010 = Erases 8 words  
011001 = Erases 4 words  
011000 = Erases 1 word  
0100xx = Erases entire data EEPROM  
Programming Operations (when ERASE bit is '0'):  
001xxx = Writes 1 word

**Note 1:** These NVMOP configurations are unimplemented on PIC24F04KL10X and PIC24F08KL20X devices.

# PIC24F16KL402 FAMILY

## 6.4.1 ERASE DATA EEPROM

The data EEPROM can be fully erased, or can be partially erased, at three different sizes: one word, four words or eight words. The bits, NVMOP<1:0> (NVMCON<1:0>), decide the number of words to be erased. To erase partially from the data EEPROM, the following sequence must be followed:

1. Configure NVMCON to erase the required number of words: one, four or eight.
2. Load TBLPAG and WREG with the EEPROM address to be erased.
3. Clear the NVMIF status bit and enable the NVM interrupt (optional).
4. Write the key sequence to NVMKEY.
5. Set the WR bit to begin the erase cycle.
6. Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).

A typical erase sequence is provided in Example 6-2. This example shows how to do a one-word erase. Similarly, a four-word erase and an eight-word erase can be done. This example uses C library procedures to manage the Table Pointer (`builtin_tblpage` and `builtin_tbloffset`) and the Erase Page Pointer (`builtin_tblwtl`). The memory unlock sequence (`builtin_write_NVM`) also sets the WR bit to initiate the operation and returns control when complete.

### EXAMPLE 6-2: SINGLE-WORD ERASE

```
int __attribute__((space(eedata))) eeData = 0x1234; // Global variable located in EEPROM
unsigned int offset;

// Set up NVMCON to erase one word of data EEPROM
NVMCON = 0x4058;

// Set up a pointer to the EEPROM location to be erased
TBLPAG = __builtin_tblpage(&eeData);           // Initialize EE Data page pointer
offset = __builtin_tbloffset(&eeData);          // Initialize lower word of address
__builtin_tblwtl(offset, 0);                     // Write EEPROM data to write latch

asm volatile ("disi #5");                        // Disable Interrupts For 5 Instructions
__builtin_write_NVM();                          // Issue Unlock Sequence & Start Write Cycle
while(NVMCONbits.WR=1);                        // Optional: Poll WR bit to wait for
                                                // write sequence to complete
```

# PIC24F16KL402 FAMILY

## REGISTER 8-13: IEC2: INTERRUPT ENABLE CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	T3GIE	—	—	—	—	—
bit 7							bit 0

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-6      **Unimplemented:** Read as '0'  
 bit 5      **T3GIF:** Timer3 External Gate Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled  
 bit 4-0      **Unimplemented:** Read as '0'

## REGISTER 8-14: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0
—	—	—	—	—	BCL2IE <sup>(1)</sup>	SSP2IE <sup>(1)</sup>	—
bit 7							bit 0

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-3      **Unimplemented:** Read as '0'  
 bit 2      **BCL2IE:** MSSP2 I<sup>2</sup>C™ Bus Collision Interrupt Enable bit<sup>(1)</sup>  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled  
 bit 1      **SSP2IF:** MSSP2 SPI/I<sup>2</sup>C Event Interrupt Enable bit<sup>(1)</sup>  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled  
 bit 0      **Unimplemented:** Read as '0'

**Note 1:** These bits are unimplemented on PIC24FXXKL10X and PIC24FXXKL20X devices.



# PIC24F16KL402 FAMILY

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## REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 7	<b>CLKLOCK:</b> Clock Selection Lock Enable bit <u>If FSCM is Enabled (FCKSM1 = 1):</u> 1 = Clock and PLL selections are locked 0 = Clock and PLL selections are not locked and may be modified by setting the OSWEN bit <u>If FSCM is Disabled (FCKSM1 = 0):</u> Clock and PLL selections are never locked and may be modified by setting the OSWEN bit.
bit 6	<b>Unimplemented:</b> Read as '0'
bit 5	<b>LOCK:</b> PLL Lock Status bit <sup>(2)</sup> 1 = PLL module is in lock or the PLL module start-up timer is satisfied 0 = PLL module is out of lock, the PLL start-up timer is running or PLL is disabled
bit 4	<b>Unimplemented:</b> Read as '0'
bit 3	<b>CF:</b> Clock Fail Detect bit 1 = FSCM has detected a clock failure 0 = No clock failure has been detected
bit 2	<b>SOSCDRV:</b> Secondary Oscillator Drive Strength bit <sup>(3)</sup> 1 = High-power SOSC circuit is selected 0 = Low/high-power select is done via the SOSCSRC Configuration bit
bit 1	<b>SOSCEN:</b> 32 kHz Secondary Oscillator (SOSC) Enable bit 1 = Enables secondary oscillator 0 = Disables secondary oscillator
bit 0	<b>OSWEN:</b> Oscillator Switch Enable bit 1 = Initiates an oscillator switch to the clock source specified by the NOSC<2:0> bits 0 = Oscillator switch is complete

- Note 1:** Reset values for these bits are determined by the FNOSC<2:0> Configuration bits.
- 2:** Also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.
- 3:** When SOSC is selected to run from a digital clock input rather than an external crystal (SOSCSRC = 0), this bit has no effect.

## 9.4 Clock Switching Operation

With few limitations, applications are free to switch between any of the four clock sources (POSC, SOSC, FRC and LPRC) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC24F devices have a safeguard lock built into the switching process.

**Note:** The Primary Oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMDx Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

### 9.4.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in the FOSC Configuration register must be programmed to '0'. (Refer to **Section 23.0 "Special Features"** for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and FSCM function are disabled; this is the default setting.

The NOSCx control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSCx bits (OSCCON<14:12>) will reflect the clock source selected by the FNOSCx Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

### 9.4.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

1. If desired, read the COSCx bits (OSCCON<14:12>) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
3. Write the appropriate value to the NOSCx bits (OSCCON<10:8>) for the new oscillator source.
4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
5. Set the OSWEN bit to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically, as follows:

1. The clock switching hardware compares the COSCx bits with the new value of the NOSCx bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
2. If a valid clock switch has been initiated, the LOCK (OSCCON<5>) and CF (OSCCON<3>) bits are cleared.
3. The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware will wait until the OST expires. If the new source is using the PLL, then the hardware waits until a PLL lock is detected (LOCK = 1).
4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSCx bits value is transferred to the COSCx bits.
6. The old clock source is turned off at this time, with the exception of LPRC (if WDT or FSCM, with LPRC as a clock source, are enabled) or SOSC (if SOSSEN remains enabled).

**Note 1:** The processor will continue to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.

- 2: Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

# PIC24F16KL402 FAMILY

## 11.3 Input Change Notification

The Input Change Notification (ICN) function of the I/O ports allows the PIC24F16KL402 family of devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature is capable of detecting input Change-of-States, even in Sleep mode, when the clocks are disabled. Depending on the device pin count, there are up to 23 external signals that may be selected (enabled) for generating an interrupt request on a Change-of-State.

There are six control registers associated with the Change Notification (CN) module. The CNEN1 and CNEN2 registers contain the interrupt enable control bits for each of the CN input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin also has a weak pull-up/pull-down connected to it. The pull-ups act as a current source that is connected to the pin. The pull-downs act as a current sink to eliminate the need for external resistors when push button or keypad devices are connected.

On any pin, only the pull-up resistor or the pull-down resistor should be enabled, but not both of them. If the push button or the keypad is connected to VDD, enable the pull-down, or if they are connected to VSS, enable the pull-up resistors. The pull-ups are enabled separately using the CNPU1 and CNPU2 registers, which contain the control bits for each of the CN pins.

Setting any of the control bits enables the weak pull-ups for the corresponding pins. The pull-downs are enabled separately, using the CNPD1 and CNPD2 registers, which contain the control bits for each of the CN pins. Setting any of the control bits enables the weak pull-downs for the corresponding pins.

When the internal pull-up is selected, the pin uses VDD as the pull-up source voltage. When the internal pull-down is selected, the pins are pulled down to VSS by an internal resistor. Make sure that there is no external pull-up source/pull-down sink when the internal pull-ups/pull-downs are enabled.

**Note:** Pull-ups and pull-downs on Change Notification pins should always be disabled whenever the port pin is configured as a digital output.

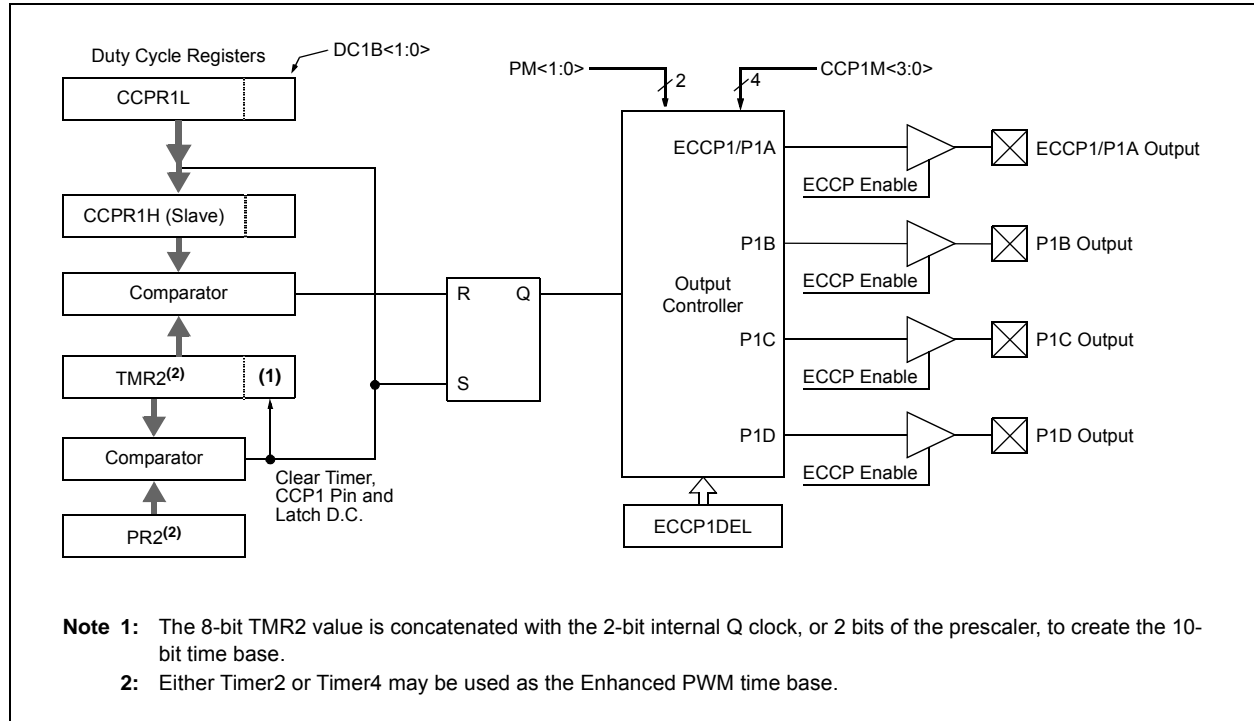
### EXAMPLE 11-1: PORT WRITE/READ EXAMPLE (ASSEMBLY LANGUAGE)

```
MOV    #0xFF00, W0          ; Configure PORTB<15:8> as inputs and PORTB<7:0> as outputs
MOV    W0, TRISB
MOV    #0x00FF, W0          ; Enable PORTB<15:8> digital input buffers
MOV    W0, ANSB
NOP                                ; Delay 1 cycle
BTSS   PORTB, #13           ; Next Instruction
```

### EXAMPLE 11-2: PORT WRITE/READ EXAMPLE (C LANGUAGE)

```
TRISB = 0xFF00;              // Configure PORTB<15:8> as inputs and PORTB<7:0> as outputs
ANSB = 0x00FF;               // Enable PORTB<15:8> digital input buffers
NOP();                       // Delay 1 cycle
if(PORTBbits.RB13 == 1)     // execute following code if PORTB pin 13 is set.
{
}
}
```

**FIGURE 16-4: SIMPLIFIED BLOCK DIAGRAM OF ENHANCED PWM MODE**



# PIC24F16KL402 FAMILY

## REGISTER 17-1: SSPxSTAT: MSSPx STATUS REGISTER (SPI MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE <sup>(1)</sup>	D/ $\bar{A}$	P	S	R/ $\bar{W}$	UA	BF
bit 7						bit 0	

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **SMP:** Sample bit

SPI Master mode:

1 = Input data is sampled at the end of data output time

0 = Input data is sampled at the middle of data output time

SPI Slave mode:

SMP must be cleared when SPI is used in Slave mode.

bit 6 **CKE:** SPI Clock Select bit<sup>(1)</sup>

1 = Transmit occurs on transition from active to Idle clock state

0 = Transmit occurs on transition from Idle to active clock state

bit 5 **D/ $\bar{A}$ :** Data/Address bit

Used in I<sup>2</sup>C™ mode only.

bit 4 **P:** Stop bit

Used in I<sup>2</sup>C mode only. This bit is cleared when the MSSPx module is disabled; SSPEN is cleared.

bit 3 **S:** Start bit

Used in I<sup>2</sup>C mode only.

bit 2 **R/ $\bar{W}$ :** Read/Write Information bit

Used in I<sup>2</sup>C mode only.

bit 1 **UA:** Update Address bit

Used in I<sup>2</sup>C mode only.

bit 0 **BF:** Buffer Full Status bit

1 = Receive is complete, SSPxBUF is full

0 = Receive is not complete, SSPxBUF is empty

**Note 1:** The polarity of the clock state is set by the CKP bit (SSPxCON1<4>).

## 18.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Universal Asynchronous Receiver Transmitter, refer to the “*dsPIC33/PIC24 Family Reference Manual*”, “**UART**” (DS39708).

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in this PIC24F device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. This module also supports a hardware flow control option with the UxCTS and UxRTS pins, and also includes an IrDA® encoder and decoder.

The primary features of the UART module are:

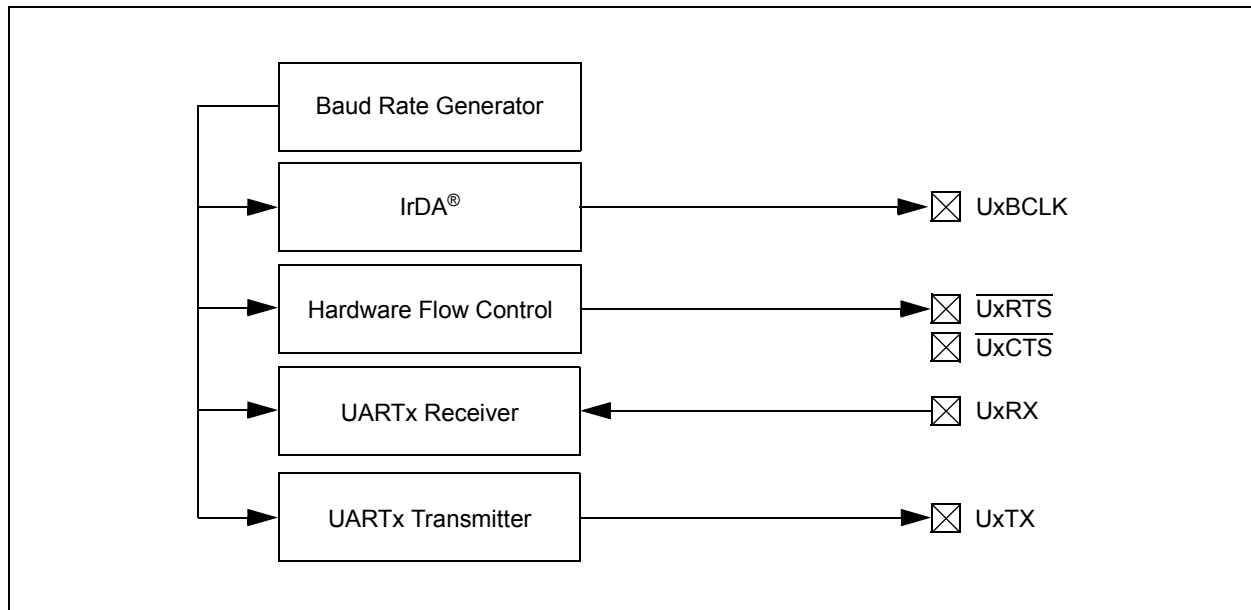
- Full-Duplex, 8-Bit or 9-Bit Data Transmission Through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with UxCTS and UxRTS Pins

- Fully Integrated Baud Rate Generator (IBRG) with 16-Bit Prescaler
- Baud Rates Ranging from 1 Mbps to 15 bps at 16 MIPS
- Two-Level Deep, First-In-First-Out (FIFO) Transmit Data Buffer
- Two-Level Deep, FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit mode with Address Detect (9<sup>th</sup> bit = 1)
- Transmit and Receive Interrupts
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Supports Automatic Baud Rate Detection
- IrDA Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA® Support

A simplified block diagram of the UART module is shown in Figure 18-1. The UART module consists of these important hardware elements:

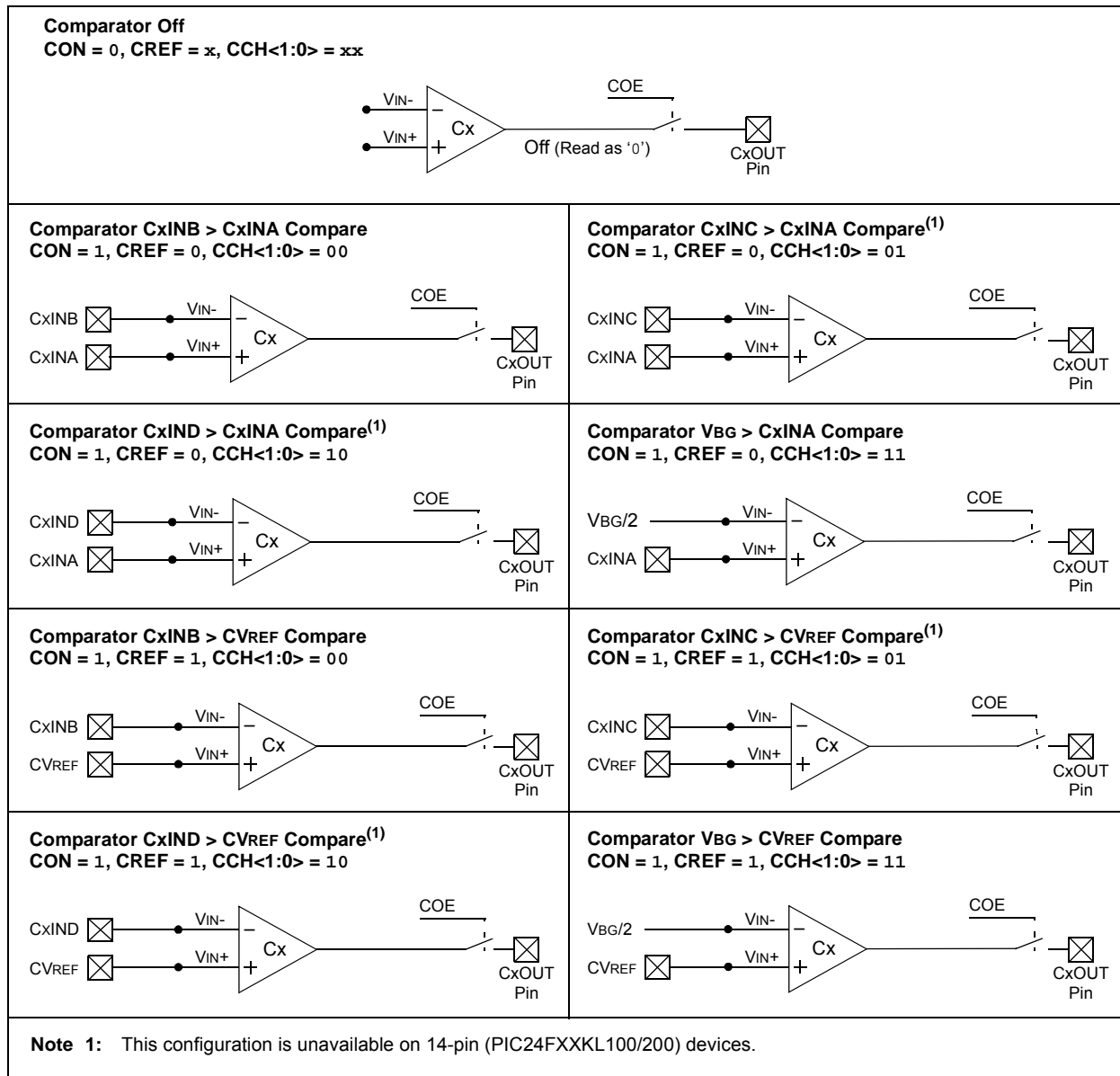
- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

**FIGURE 18-1: UARTx SIMPLIFIED BLOCK DIAGRAM**



# PIC24F16KL402 FAMILY

**FIGURE 20-2: INDIVIDUAL COMPARATOR CONFIGURATIONS**



# PIC24F16KL402 FAMILY

## REGISTER 23-9: DEVREV: DEVICE REVISION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23				bit 16			

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	R	R	R	R
—	—	—	—	REV3	REV2	REV1	REV0
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 23-4      **Unimplemented:** Read as '0'

bit 3-0      **REV<3:0>:** Revision Identifier bits



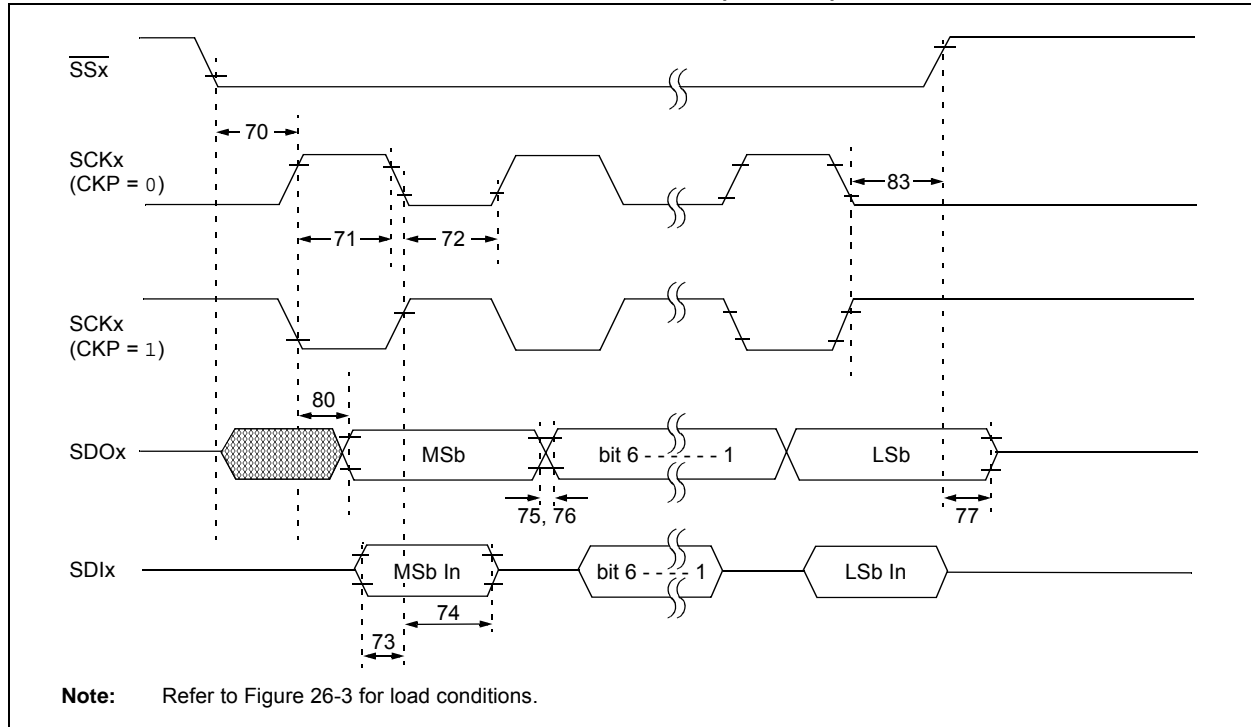
# PIC24F16KL402 FAMILY

**TABLE 25-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
BTSS	BTSS $f, \#bit4$	Bit Test $f$ , Skip if Set	1	1 (2 or 3)	None
	BTSS $Ws, \#bit4$	Bit Test $Ws$ , Skip if Set	1	1 (2 or 3)	None
BTST	BTST $f, \#bit4$	Bit Test $f$	1	1	Z
	BTST.C $Ws, \#bit4$	Bit Test $Ws$ to C	1	1	C
	BTST.Z $Ws, \#bit4$	Bit Test $Ws$ to Z	1	1	Z
	BTST.C $Ws, Wb$	Bit Test $Ws < Wb >$ to C	1	1	C
	BTST.Z $Ws, Wb$	Bit Test $Ws < Wb >$ to Z	1	1	Z
BTSTS	BTSTS $f, \#bit4$	Bit Test then Set $f$	1	1	Z
	BTSTS.C $Ws, \#bit4$	Bit Test $Ws$ to C, then Set	1	1	C
	BTSTS.Z $Ws, \#bit4$	Bit Test $Ws$ to Z, then Set	1	1	Z
CALL	CALL $lit23$	Call Subroutine	2	2	None
	CALL $Wn$	Call Indirect Subroutine	1	2	None
CLR	CLR $f$	$f = 0x0000$	1	1	None
	CLR WREG	WREG = $0x0000$	1	1	None
	CLR $Ws$	$Ws = 0x0000$	1	1	None
CLRWDT	CLRWDT	Clear Watchdog Timer	1	1	WDTO, Sleep
COM	COM $f$	$f = \bar{f}$	1	1	N, Z
	COM $f, WREG$	WREG = $\bar{f}$	1	1	N, Z
	COM $Ws, Wd$	$Wd = \overline{Ws}$	1	1	N, Z
CP	CP $f$	Compare $f$ with WREG	1	1	C, DC, N, OV, Z
	CP $Wb, \#lit5$	Compare $Wb$ with $lit5$	1	1	C, DC, N, OV, Z
	CP $Wb, Ws$	Compare $Wb$ with $Ws$ ( $Wb - Ws$ )	1	1	C, DC, N, OV, Z
CP0	CP0 $f$	Compare $f$ with $0x0000$	1	1	C, DC, N, OV, Z
	CP0 $Ws$	Compare $Ws$ with $0x0000$	1	1	C, DC, N, OV, Z
CPB	CPB $f$	Compare $f$ with WREG, with Borrow	1	1	C, DC, N, OV, Z
	CPB $Wb, \#lit5$	Compare $Wb$ with $lit5$ , with Borrow	1	1	C, DC, N, OV, Z
	CPB $Wb, Ws$	Compare $Wb$ with $Ws$ , with Borrow ( $Wb - Ws - C$ )	1	1	C, DC, N, OV, Z
CPSEQ	CPSEQ $Wb, Wn$	Compare $Wb$ with $Wn$ , Skip if =	1	1 (2 or 3)	None
CPSGT	CPSGT $Wb, Wn$	Compare $Wb$ with $Wn$ , Skip if >	1	1 (2 or 3)	None
CPSLT	CPSLT $Wb, Wn$	Compare $Wb$ with $Wn$ , Skip if <	1	1 (2 or 3)	None
CPSNE	CPSNE $Wb, Wn$	Compare $Wb$ with $Wn$ , Skip if $\neq$	1	1 (2 or 3)	None
DAW	DAW.B $Wn$	$Wn =$ Decimal Adjust $Wn$	1	1	C
DEC	DEC $f$	$f = f - 1$	1	1	C, DC, N, OV, Z
	DEC $f, WREG$	WREG = $f - 1$	1	1	C, DC, N, OV, Z
	DEC $Ws, Wd$	$Wd = Ws - 1$	1	1	C, DC, N, OV, Z
DEC2	DEC2 $f$	$f = f - 2$	1	1	C, DC, N, OV, Z
	DEC2 $f, WREG$	WREG = $f - 2$	1	1	C, DC, N, OV, Z
	DEC2 $Ws, Wd$	$Wd = Ws - 2$	1	1	C, DC, N, OV, Z
DISI	DISI $\#lit14$	Disable Interrupts for $k$ Instruction Cycles	1	1	None
DIV	DIV.SW $Wm, Wn$	Signed 16/16-bit Integer Divide	1	18	N, Z, C, OV
	DIV.SD $Wm, Wn$	Signed 32/16-bit Integer Divide	1	18	N, Z, C, OV
	DIV.UW $Wm, Wn$	Unsigned 16/16-bit Integer Divide	1	18	N, Z, C, OV
	DIV.UD $Wm, Wn$	Unsigned 32/16-bit Integer Divide	1	18	N, Z, C, OV
EXCH	EXCH $Wns, Wnd$	Swap $Wns$ with $Wnd$	1	1	None
FF1L	FF1L $Ws, Wnd$	Find First One from Left (MSb) Side	1	1	C
FF1R	FF1R $Ws, Wnd$	Find First One from Right (LSb) Side	1	1	C

# PIC24F16KL402 FAMILY

**FIGURE 26-9: EXAMPLE SPI SLAVE MODE TIMING (CKE = 0)**



**TABLE 26-29: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING, CKE = 0)**

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
70	TssL2sch, TssL2scL	$\overline{SSx} \downarrow$ to SCKx $\downarrow$ or SCKx $\uparrow$ Input	3 Tcy	—	ns	
70A	TssL2WB	$\overline{SSx}$ to Write to SSPxBUF	3 Tcy	—	ns	
71	Tsch	SCKx Input High Time	Continuous	1.25 Tcy + 30	—	ns
71A		(Slave mode)	Single Byte	40	—	ns (Note 1)
72	TscL	SCKx Input Low Time	Continuous	1.25 Tcy + 30	—	ns
72A		(Slave mode)	Single Byte	40	—	ns (Note 1)
73	TdIV2sch, TdIV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	ns	
73A	Tb2B	Last Clock Edge of Byte 1 to the First Clock Edge of Byte 2	1.5 Tcy + 40	—	ns	(Note 2)
74	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	40	—	ns	
75	TdoR	SDOx Data Output Rise Time	—	25	ns	
76	TdoF	SDOx Data Output Fall Time	—	25	ns	
77	TssH2doZ	$\overline{SSx} \uparrow$ to SDOx Output High-Impedance	10	50	ns	
80	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	50	ns	
83	Tsch2ssH, TscL2ssH	$\overline{SSx} \uparrow$ after SCKx Edge	1.5 Tcy + 40	—	ns	
	Fsck	SCKx Frequency	—	10	MHz	

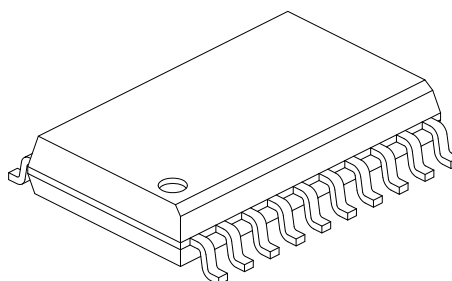
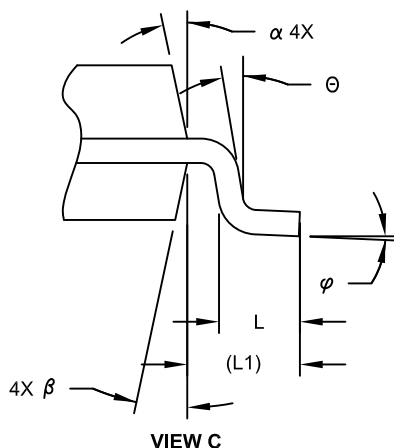
**Note 1:** Requires the use of Parameter 73A.

**2:** Only if Parameters 71A and 72A are used.

# PIC24F16KL402 FAMILY

## 20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	12.80 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.20	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

### Notes:

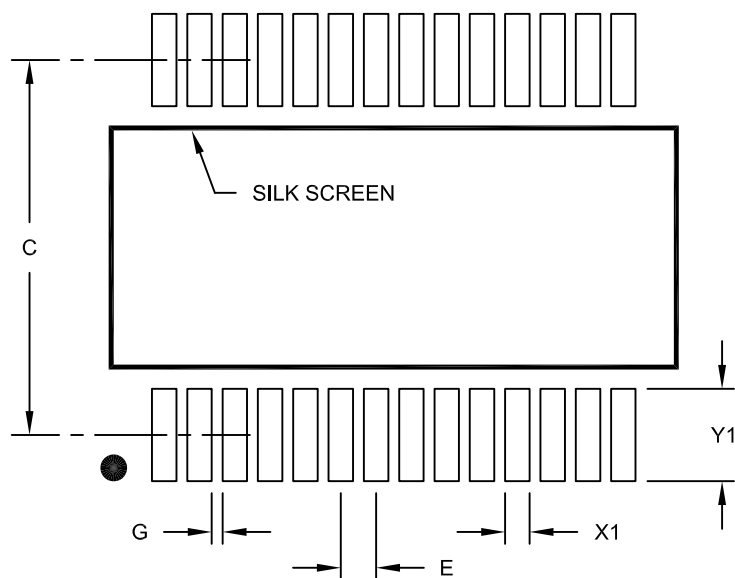
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-094C Sheet 2 of 2

# PIC24F16KL402 FAMILY

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

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