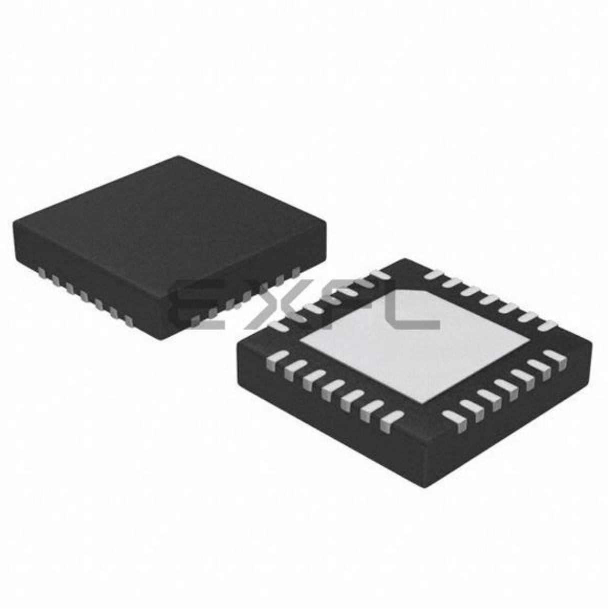
Microchip Technology - PIC24F08KL402-E/MQ Datasheet



Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VFQFN Exposed Pad
Supplier Device Package	28-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f08kl402-e-mq

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1.2 Other Special Features

- **Communications:** The PIC24F16KL402 family incorporates multiple serial communication peripherals to handle a range of application requirements. The MSSP module implements both SPI and I^2C™ protocols, and supports both Master and Slave modes of operation for each. Devices also include one of two UARTs with built-in IrDA® encoders/decoders.
- **Analog Features:** Select members of the PIC24F16KL402 family include a 10-bit A/D Converter module. The A/D module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, as well as faster sampling speeds.
  The comparator modules are configurable for a wide range of operations and can be used as either a single or double comparator module.

1.3 Details on Individual Family Members

Devices in the PIC24F16KL402 family are available in 14-pin, 20-pin and 28-pin packages. The general block diagram for all devices is shown in Figure 1-1.

The PIC24F16KL402 family may be thought of as four different device groups, each offering a slightly different set of features. These differ from each other in multiple ways:

- The size of the Flash program memory
- The presence and size of data EEPROM
- The presence of an A/D Converter and the number of external analog channels available
- The number of analog comparators
- The number of general purpose timers
- The number and type of CCP modules (i.e., CCP vs. ECCP)
- The number of serial communications modules (both MSSPs and UARTs)

The general differences between the different sub-families are shown in Table 1-1. The feature sets for specific devices are summarized in Table 1-2 and Table 1-3.

A list of the individual pin features available on the PIC24F16KL402 family devices, sorted by function, is provided in Table 1-4 (for PIC24FXXKL40X/30X devices) and Table 1-5 (for PIC24FXXKL20X/10X devices). Note that these tables show the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of this data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

TABLE 1-1: FEATURE COMPARISON FOR PIC24F16KL402 FAMILY GROUPS

Device Group	Program Memory (bytes)	Data EEPROM (bytes)	Timers (8/16-bit)	CCP and ECCP	Serial (MSSP/ UART)	A/D (channels)	Comparators
PIC24FXXKL10X	4K	—	1/2	2/0	1/1	—	1
PIC24FXXKL20X	8K	—	1/2	2/0	1/1	7 or 12	1
PIC24FXXKL30X	8K	256	2/2	2/1	2/2	—	2
PIC24FXXKL40X	8K or 16K	512	2/2	2/1	2/2	12	2

TABLE 1-4: PIC24F16KL40X/30X FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number				I/O	Buffer	Description
	20-Pin PDIP/ SSOP/ SOIC	20-Pin QFN	28-Pin SPDIP/ SSOP/ SOIC	28-Pin QFN			
CN0	10	7	12	9	I	ST	Interrupt-on-Change Inputs
CN1	9	6	11	8	I	ST	
CN2	2	19	2	27	I	ST	
CN3	3	20	3	28	I	ST	
CN4	4	1	4	1	I	ST	
CN5	5	2	5	2	I	ST	
CN6	6	3	6	3	I	ST	
CN7	—	—	7	4	I	ST	
CN8	14	11	20	17	I	ST	
CN9	—	—	19	16	I	ST	
CN11	18	15	26	23	I	ST	
CN12	17	14	25	22	I	ST	
CN13	16	13	24	21	I	ST	
CN14	15	12	23	20	I	ST	
CN15	—	—	22	19	I	ST	
CN16	—	—	21	18	I	ST	
CN21	13	10	18	15	I	ST	
CN22	12	9	17	14	I	ST	
CN23	11	8	16	13	I	ST	
CN24	—	—	15	12	I	ST	
CN27	—	—	14	11	I	ST	
CN29	8	5	10	7	I	ST	
CN30	7	4	9	6	I	ST	
CVREF	17	14	25	22	I	ANA	Comparator Voltage Reference Output
CVREF+	2	19	2	27	I	ANA	Comparator Reference Positive Input Voltage
CVREF-	3	20	3	28	I	ANA	Comparator Reference Negative Input Voltage
$\overline{\text{FLT0}}$	17	14	25	22	I	ST	ECCP1 Enhanced PWM Fault Input
HLVDIN	15	12	23	20	I	ST	High/Low-Voltage Detect Input
INT0	11	8	16	13	I	ST	Interrupt 0 Input
INT1	17	14	25	22	I	ST	Interrupt 1 Input
INT2	14	11	20	17	I	ST	Interrupt 2 Input
$\overline{\text{MCLR}}$	1	18	1	26	I	ST	Master Clear (device Reset) Input. This line is brought low to cause a Reset.
OSCI	7	4	9	6	I	ANA	Main Oscillator Input
OSCO	8	5	10	7	O	ANA	Main Oscillator Output
P1A	14	11	20	17	O	—	ECCP1 Output A (Enhanced PWM Mode)
P1B	5	2	21	18	O	—	ECCP1 Output B (Enhanced PWM Mode)
P1C	4	1	22	19	O	—	ECCP1 Output C (Enhanced PWM Mode)
P1D	16	13	18	15	O	—	ECCP1 Output D (Enhanced PWM Mode)

Legend: TTL = TTL input buffer
ANA = Analog level input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C™/SMBus input buffer

FIGURE 3-1: PIC24F CPU CORE BLOCK DIAGRAM

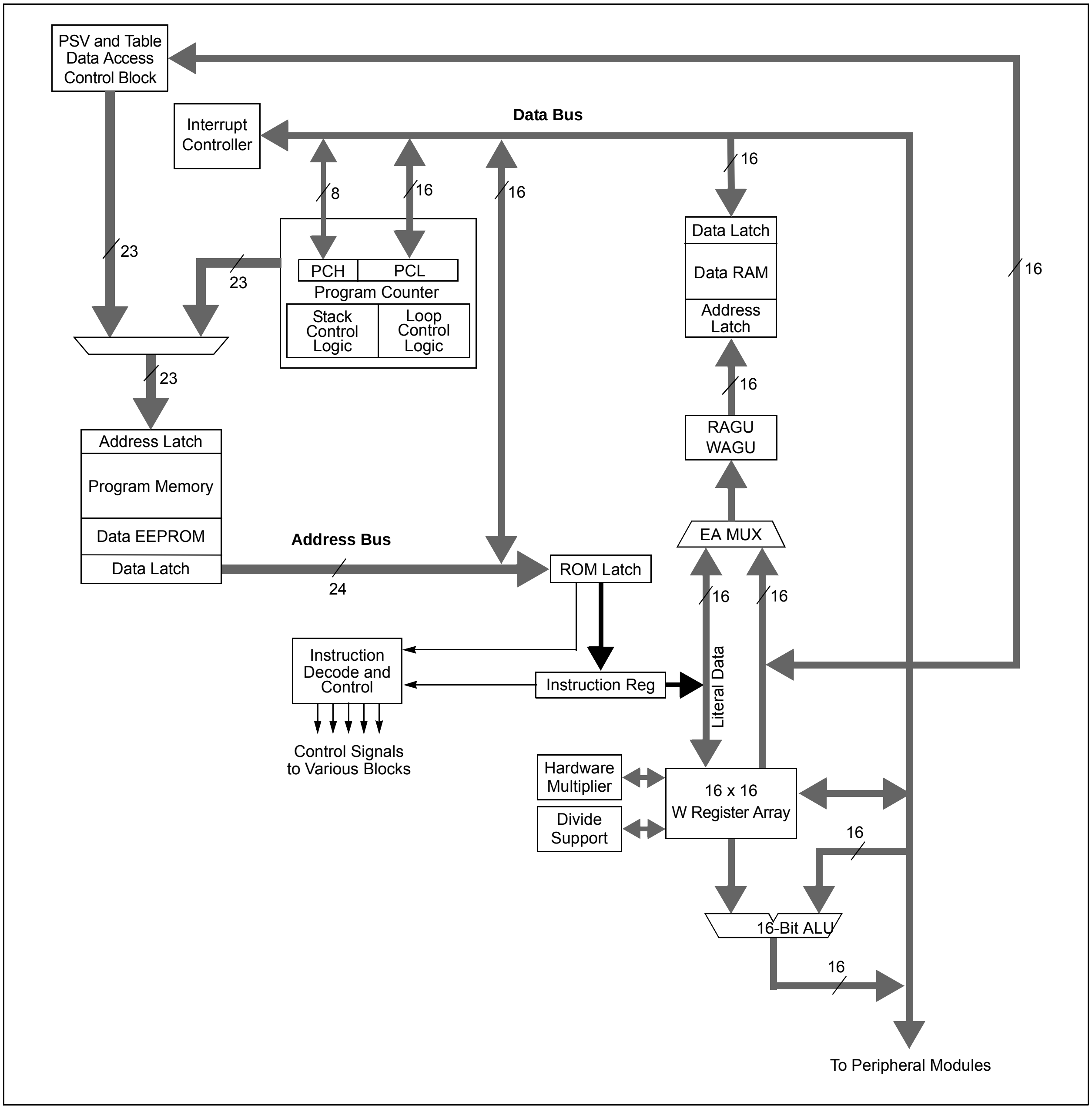


TABLE 3-1: CPU CORE REGISTERS

Register(s) Name	Description
W0 through W15	Working Register Array
PC	23-Bit Program Counter
SR	ALU STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
PSVPAG	Program Space Visibility Page Address Register
RCOUNT	REPEAT Loop Counter Register
CORCON	CPU Control Register

4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® devices and improve data space memory usage efficiency, the PIC24F instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address (EA) calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] will result in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

Data byte reads will read the complete word, which contains the byte, using the LSB of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and the registers are organized as two parallel, byte-wide entities with shared (word) address decode, but separate write lines. Data byte writes only write to the corresponding side of the array or register, which matches the byte address.

All word accesses must be aligned to an even address. Mis-aligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a mis-aligned read or write is attempted, an address error trap will be generated. If the error occurred on a read, the instruction underway is completed; if it occurred on a write, the instruction will be executed, but the write will not occur. In either case, a trap is then executed, allowing the system and/or user to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB; the MSB is not modified.

A Sign-Extend (`SE`) instruction is provided to allow the users to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, users can clear the MSB of any W register by executing a Zero-Extend (`ZE`) instruction on the appropriate address.

Although most instructions are capable of operating on word or byte data sizes, it should be noted that some instructions operate only on words.

4.2.3 NEAR DATA SPACE

The 8-Kbyte area between 0000h and 1FFFh is referred to as the Near Data Space (NDS). Locations in this space are directly addressable via a 13-bit absolute address field within all memory direct instructions. The remainder of the data space is addressable indirectly. Additionally, the whole data space is addressable using `MOV` instructions, which support Memory Direct Addressing (MDA) with a 16-bit address field. For PIC24F16KL402 family devices, the entire implemented data memory lies in Near Data Space.

4.2.4 SFR SPACE

The first 2 Kbytes of the Near Data Space, from 0000h to 07FFh, are primarily occupied with Special Function Registers (SFRs). These are used by the PIC24F core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by the module. Much of the SFR space contains unused addresses; these are read as '`0`'. The SFR space, where the SFRs are actually implemented, is provided in Table 4-2. Each implemented area indicates a 32-byte region, where at least one address is implemented as an SFR. A complete listing of implemented SFRs, including their addresses, is provided in Table 4-3 through Table 4-18.

TABLE 4-2: IMPLEMENTED REGIONS OF SFR DATA SPACE

<table>
<tr><th rowspan="2"></th><th colspan="16">SFR Space Address</th></tr>
<tr><th colspan="2">xx00</th><th colspan="2">xx20</th><th colspan="2">xx40</th><th colspan="2">xx60</th><th colspan="2">xx80</th><th colspan="2">xxA0</th><th colspan="2">xxC0</th><th colspan="2">xxE0</th></tr>
<tr><td>000h</td><td colspan="6">Core</td><td colspan="2">ICN</td><td colspan="6">Interrupts</td><td colspan="2">—</td></tr>
<tr><td>100h</td><td colspan="2">Timers</td><td>—</td><td>TMR</td><td colspan="2">—</td><td colspan="2">—</td><td>—</td><td colspan="2">CCP</td><td>—</td><td colspan="2">—</td><td colspan="2">—</td></tr>
<tr><td>200h</td><td colspan="2">MSSP</td><td colspan="2">UART</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">I/O</td><td colspan="2">—</td></tr>
<tr><td>300h</td><td colspan="4">A/D</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td></tr>
<tr><td>400h</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td>—</td><td colspan="2">ANSEL</td><td>—</td></tr>
<tr><td>500h</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td></tr>
<tr><td>600h</td><td colspan="2">—</td><td>CMP</td><td>—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td></tr>
<tr><td>700h</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">System</td><td colspan="2">NVM/PMD</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td><td colspan="2">—</td></tr>
</table>

Legend: — = No implemented SFRs in this block.

6.0 DATA EEPROM MEMORY

> **Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Data EEPROM, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Data EEPROM"** (DS39720).

The data EEPROM memory is a Nonvolatile Memory (NVM), separate from the program and volatile data RAM. Data EEPROM memory is based on the same Flash technology as program memory, and is optimized for both long retention and a higher number of erase/write cycles.

The data EEPROM is mapped to the top of the user program memory space, with the top address at program memory address, 7FFFFFh. For PIC24FXXKL4XX devices, the size of the data EEPROM is 256 words (7FFE00h to 7FFFFFh). For PIC24FXXKL3XX devices, the size of the data EEPROM is 128 words (7FFF00h to 7FFFFFh). The data EEPROM is not implemented in PIC24F08KL20X or PIC24F04KL10X devices.

The data EEPROM is organized as 16-bit wide memory. Each word is directly addressable, and is readable and writable during normal operation over the entire V_{DD} range.

Unlike the Flash program memory, normal program execution is not stopped during a data EEPROM program or erase operation.

The data EEPROM programming operations are controlled using the three NVM Control registers:

- NVMCON: Nonvolatile Memory Control Register
- NVMKEY: Nonvolatile Memory Key Register
- NVMADR: Nonvolatile Memory Address Register

6.1 NVMCON Register

The NVMCON register (Register 6-1) is also the primary control register for data EEPROM program/erase operations. The upper byte contains the control bits used to start the program or erase cycle, and the flag bit to indicate if the operation was successfully performed. The lower byte of NVMCOM configures the type of NVM operation that will be performed.

6.2 NVMKEY Register

The NVMKEY is a write-only register that is used to prevent accidental writes or erasures of data EEPROM locations.

To start any programming or erase sequence, the following instructions must be executed first, in the exact order provided:

1. Write 55h to NVMKEY.
2. Write AAh to NVMKEY.

After this sequence, a write will be allowed to the NVMCON register for one instruction cycle. In most cases, the user will simply need to set the WR bit in the NVMCON register to start the program or erase cycle. Interrupts should be disabled during the unlock sequence.

The MPLAB® C30 C compiler provides a defined library procedure (`builtin_write_NVM`) to perform the unlock sequence. Example 6-1 illustrates how the unlock sequence can be performed with in-line assembly.

EXAMPLE 6-1: DATA EEPROM UNLOCK SEQUENCE

```
//Disable Interrupts For 5 instructions
asm volatile("disi #5");
//Issue Unlock Sequence
asm volatile ("mov #0x55, W0      \n"
             "mov W0, NVMKEY      \n"
             "mov #0xAA, W1       \n"
             "mov W1, NVMKEY      \n");
// Perform Write/Erase operations
asm volatile ("bset NVMCON, #WR   \n"
             "nop                 \n"
             "nop                 \n");
```

7.4.2 DETECTING BOR

When BOR is enabled, the BOR bit (RCON<1>) is always reset to '`1`' on any BOR or POR event. This makes it difficult to determine if a BOR event has occurred just by reading the state of BOR alone. A more reliable method is to simultaneously check the state of both POR and BOR. This assumes that the POR and BOR bits are reset to '`0`' in the software, immediately after any POR event. If the BOR bit is '`1`' while POR is '`0`', it can be reliably assumed that a BOR event has occurred.

Note: Even when the device exits from Deep Sleep mode, both the POR and BOR are set.

7.4.3 DISABLING BOR IN SLEEP MODE

When BOREN<1:0> = `10`, BOR remains under hardware control and operates as previously described. However, whenever the device enters Sleep mode, BOR is automatically disabled. When the device returns to any other operating mode, BOR is automatically re-enabled.

This mode allows for applications to recover from brown-out situations, while actively executing code when the device requires BOR protection the most. At the same time, it saves additional power in Sleep mode by eliminating the small incremental BOR current.

REGISTER 8-21: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CNIP2	CNIP1	CNIP0	—	CMIP2	CMIP1	CMIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	BCL1IP2	BCL1IP1	BCL1IP0	—	SSP1IP2	SSP1IP1	SSP1IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘`0`’

bit 14-12 **CNIP<2:0>:** Input Change Notification Interrupt Priority bits

`111` = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
`001` = Interrupt is Priority 1
`000` = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘`0`’

bit 10-8 **CMIP<2:0>:** Comparator Interrupt Priority bits

`111` = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
`001` = Interrupt is Priority 1
`000` = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘`0`’

bit 6-4 **BCL1IP<2:0>:** MSSP1 I^2C™ Bus Collision Interrupt Priority bits

`111` = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
`001` = Interrupt is Priority 1
`000` = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘`0`’

bit 2-0 **SSP1IP<2:0>:** MSSP1 SPI/I^2C Event Interrupt Priority bits

`111` = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
`001` = Interrupt is Priority 1
`000` = Interrupt source is disabled

REGISTER 19-2: AD1CON2: A/D CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0
VCFG2	VCFG1	VCFG0	OFFCAL[1]	—	CSCNA	—	—
bit 15							bit 8

R-x	U-0	R/W-0	R/W-0	R/W-0	R/W-0	r-0	R/W-0
r	—	SMPI3	SMPI2	SMPI1	SMPI0	r	ALTS
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

VCFG<2:0>	VR+	VR-
`000`	AVDD	AVSS
`001`	External VREF+ pin	AVSS
`010`	AVDD	External VREF- pin
`011`	External VREF+ pin	External VREF- pin
`1xx`	AVDD	AVSS

bit 12 **OFFCAL:** Offset Calibration bit[1]

`1` = Conversions to get the offset calibration value
`0` = Conversions to get the actual input value

bit 11 **Unimplemented:** Read as ‘0’

bit 10 **CSCNA:** Scan Input Selections for MUX A Input Multiplexer bit

`1` = Scans inputs
`0` = Does not scan inputs

bit 9-8 **Unimplemented:** Read as ‘0’

bit 7 **Reserved:** Ignore this value

bit 6 **Unimplemented:** Read as ‘0’

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits

`1111` =
•
• = Reserved, do not use (may cause conversion data loss)
•
`0010` =
`0001` = Interrupts at the completion of conversion for each 2nd sample/convert sequence
`0000` = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **Reserved:** Always maintain as ‘0’

bit 0 **ALTS:** Alternate Input Sample Mode Select bit

`1` = Uses MUX A input multiplexer settings for the first sample, then alternates between MUX B and MUX A input multiplexer settings for all subsequent samples
`0` = Always uses MUX A input multiplexer settings

Note 1: When the OFFCAL bit is set, inputs are disconnected and tied to AVSS. This sets the inputs of the A/D to zero. Then, the user can perform a conversion. Use of the Calibration mode is not affected by AD1PCFG contents nor channel input selection. Any analog input switches are disconnected from the A/D Converter in this mode. The conversion result is stored by the user software and used to compensate subsequent conversions. This can be done by adding the two’s complement of the result obtained with the OFFCAL bit set to all normal A/D conversions.

NOTES:

REGISTER 20-1: CMxCON: COMPARATOR x CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R-0
CON	COE	CPOL	CLPWR	—	—	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1(1)	EVPOL0(1)	—	CREF	—	—	CCH1	CCH0
bit 7							bit 0

Legend:

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown

bit 15 **CON:** Comparator Enable bit

`1` = Comparator is enabled
`0` = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit

`1` = Comparator output is present on the CxOUT pin
`0` = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit

`1` = Comparator output is inverted
`0` = Comparator output is not inverted

bit 12 **CLPWR:** Comparator Low-Power Mode Select bit

`1` = Comparator operates in Low-Power mode
`0` = Comparator does not operate in Low-Power mode

bit 11-10 **Unimplemented:** Read as ‘`0`’

bit 9 **CEVT:** Comparator Event bit

`1` = Comparator event defined by EVPOL<1:0> has occurred; subsequent triggers and interrupts are disabled until the bit is cleared
`0` = Comparator event has not occurred

bit 8 **COUT:** Comparator Output bit

When CPOL = `0`:
`1` = VIN+ > VIN-
`0` = VIN+ < VIN-

When CPOL = `1`:
`1` = VIN+ < VIN-
`0` = VIN+ > VIN-

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits(1)

`11` = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = `0`)
`10` = Trigger/event/interrupt is generated on the high-to-low transition of the comparator output
`01` = Trigger/event/Interrupt is generated on the low-to-high transition of the comparator output
`00` = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as ‘`0`’

bit 4 **CREF:** Comparator Reference Select bits (non-inverting input)

`1` = Non-inverting input connects to the internal CVREF voltage
`0` = Non-inverting input connects to the CxINA pin

Note 1: If EVPOL<1:0> is set to a value other than ‘`00`’, the first interrupt generated will occur on any transition of COUT, regardless of if it is a rising or falling edge. Subsequent interrupts will occur based on the EVPOLx bits setting.

2: Unimplemented on 14-pin (PIC24FXXKL100/200) devices.

REGISTER 22-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
HLVDEN	—	HLSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VDIR	BGVST	IRVST	—	HLVDL3	HLVDL2	HLVDL1	HLVDL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **HLVDEN:** High/Low-Voltage Detect Power Enable bit

`1` = HLVD is enabled
`0` = HLVD is disabled

bit 14 **Unimplemented:** Read as ‘`0`’

bit 13 **HLSIDL:** HLVD Stop in Idle Mode bit

`1` = Discontinues module operation when the device enters Idle mode
`0` = Continues module operation in Idle mode

bit 12-8 **Unimplemented:** Read as ‘`0`’

bit 7 **VDIR:** Voltage Change Direction Select bit

`1` = Event occurs when the voltage equals or exceeds the trip point (HLVDL<3:0>)
`0` = Event occurs when the voltage equals or falls below the trip point (HLVDL<3:0>)

bit 6 **BGVST:** Band Gap Voltage Stable Flag bit

`1` = Indicates that the band gap voltage is stable
`0` = Indicates that the band gap voltage is unstable

bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit

`1` = Indicates that the internal reference voltage is stable and the High-Voltage Detect logic generates the interrupt flag at the specified voltage range
`0` = Indicates that the internal reference voltage is unstable and the High-Voltage Detect logic will not generate the interrupt flag at the specified voltage range, and the HLVD interrupt should not be enabled

bit 4 **Unimplemented:** Read as ‘`0`’

bit 3-0 **HLVDL<3:0>:** High/Low-Voltage Detection Limit bits

`1111` = External analog input is used (input comes from the HLVDIN pin)
`1110` = Trip Point 14[(1)]
`1101` = Trip Point 13[(1)]
`1100` = Trip Point 12[(1)]
.
.
.
`0000` = Trip Point 0[(1)]

Note 1: For the actual trip point, see **Section 26.0 “Electrical Characteristics”**.

REGISTER 23-5: FWDT: WATCHDOG TIMER CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
FWDTEN1	WINDIS	FWDTEN0	FWPSA	WDTPS3	WDTPS2	WDTPS1	WDTPS0
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7,5 **FWDTEN<1:0>:** Watchdog Timer Enable bits

`11` = WDT is enabled in hardware
`10` = WDT is controlled with the SWDTEN bit setting
`01` = WDT is enabled only while device is active; WDT is disabled in Sleep, SWDTEN bit is disabled
`00` = WDT is disabled in hardware; SWDTEN bit is disabled

bit 6 **WINDIS:** Windowed Watchdog Timer Disable bit

`1` = Standard WDT is selected; windowed WDT is disabled
`0` = Windowed WDT is enabled; note that executing a `CLRWDT` instruction while the WDT is disabled in hardware and software (FWDTEN<1:0> = `00` and SWDTEN (RCON<5> = `0`) will not cause a device Reset

bit 4 **FWPSA:** WDT Prescaler bit

`1` = WDT prescaler ratio of 1:128
`0` = WDT prescaler ratio of 1:32

bit 3-0 **WDTPS<3:0>:** Watchdog Timer Postscale Select bits

`1111` = 1:32,768
`1110` = 1:16,384
`1101` = 1:8,192
`1100` = 1:4,096
`1011` = 1:2,048
`1010` = 1:1,024
`1001` = 1:512
`1000` = 1:256
`0111` = 1:128
`0110` = 1:64
`0101` = 1:32
`0100` = 1:16
`0011` = 1:8
`0010` = 1:4
`0001` = 1:2
`0000` = 1:1

TABLE 25-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
`TBLRDH`	`TBLRDH`	`Ws,Wd`	Read Prog<23:16> to Wd<7:0>	1	2	None
`TBLRDL`	`TBLRDL`	`Ws,Wd`	Read Prog<15:0> to Wd	1	2	None
`TBLWTH`	`TBLWTH`	`Ws,Wd`	Write Ws<7:0> to Prog<23:16>	1	2	None
`TBLWTL`	`TBLWTL`	`Ws,Wd`	Write Ws to Prog<15:0>	1	2	None
`ULNK`	`ULNK`		Unlink Frame Pointer	1	1	None
`XOR`	`XOR`	`f`	f = f .XOR. WREG	1	1	N, Z
	`XOR`	`f,WREG`	WREG = f .XOR. WREG	1	1	N, Z
	`XOR`	`#lit10,Wn`	Wd = lit10 .XOR. Wd	1	1	N, Z
	`XOR`	`Wb,Ws,Wd`	Wd = Wb .XOR. Ws	1	1	N, Z
	`XOR`	`Wb,#lit5,Wd`	Wd = Wb .XOR. lit5	1	1	N, Z
`ZE`	`ZE`	`Ws,Wnd`	Wnd = Zero-Extend Ws	1	1	C, Z, N

TABLE 26-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)(2)

DC CHARACTERISTICS			**Standard Operating Conditions: 1.8V to 3.6V** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
IDD Current						
DC20	0.154	0.350	mA	1.8V	+85V°C	0.5 MIPS, FOSC = 1 MHz
	0.301	0.630		3.3V		
	—	.500	mA	1.8V	+125°C	
	—	.800		3.3V		
DC22	0.300	—	mA	1.8V	+85°C	1 MIPS, FOSC = 2 MHz
	0.585	—		3.3V		
DC24	7.76	12.0	mA	3.3V	+85°C	16 MIPS, FOSC = 32 MHz
	—	18.0		3.3V	+125°C	
DC26	1.44	—	mA	1.8V	+85°C	FRC (4 MIPS), FOSC = 8 MHz
	2.71	—		3.3V		
DC30	4.00	28.0	µA	1.8V	+85°C	LPRC (15.5 KIPS), FOSC = 31 kHz
	9.00	55.0		3.3V		
	—	45.0	µA	1.8V	+125°C	
	—	90.0		3.3V		

Note 1: Data in the Typical column is at 3.3V, +25°C, unless otherwise stated.

2: IDD is measured with all peripherals disabled. All I/Os are configured as outputs and set low; PMDx bits are set to '1' and WDT, etc., are all disabled.

TABLE 26-7: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)(2)

DC CHARACTERISTICS			**Standard Operating Conditions: 1.8V to 3.6V** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Idle Current (IIDLE)						
DC40	0.035	0.080	mA	1.8V	+85°C	0.5 MIPS, FOSC = 1 MHz
	0.077	0.150		3.3V		
	—	0.160	mA	1.8V	+125°C	
	—	0.300		3.3V		
DC42	0.076	—	mA	1.8V	+85°C	1 MIPS, FOSC = 2 MHz
	0.146	—		3.3V		
DC44	2.52	3.20	mA	3.3V	+85°C	16 MIPS, FOSC = 32 MHz
	—	5.00	mA	3.3V	+125°C	
DC46	0.45	—	mA	1.8V	+85°C	FRC (4 MIPS), FOSC = 8 MHz
	0.76	—	mA	3.3V		
DC50	0.87	18.0	µA	1.8V	+85°C	LPRC (15.5 KIPS), FOSC = 31 kHz
	1.55	40.0	µA	3.3V		
	—	27.0	µA	1.8V	+125°C	
	—	50.0	µA	3.3V		

Note 1: Data in the Typical column is at 3.3V, +25°C, unless otherwise stated.

2: IIDLE is measured with all I/Os configured as outputs and set low; PMDx bits are set to '1' and WDT, etc., are all disabled.

TABLE 26-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			**Standard Operating Conditions: 1.8V to 3.6V** Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	V_{IL}	**Input Low Voltage(4)**					
DI10		I/O Pins	V_{SS}	—	0.2 V_{DD}	V	
DI15		$\overline{MCLR}$	V_{SS}	—	0.2 V_{DD}	V	
DI16		OSCI (XT mode)	V_{SS}	—	0.2 V_{DD}	V	
DI17		OSCI (HS mode)	V_{SS}	—	0.2 V_{DD}	V	
DI18		I/O Pins with I^{2}C™ Buffer	V_{SS}	—	0.3 V_{DD}	V	SMBus disabled
DI19		I/O Pins with SMBus Buffer	V_{SS}	—	0.8	V	SMBus enabled
	V_{IH}	**Input High Voltage(4,5)**					
DI20		I/O Pins:					
		with Analog Functions	0.8 V_{DD}	—	V_{DD}	V	
		Digital Only	0.8 V_{DD}	—	V_{DD}	V	
DI25		$\overline{MCLR}$	0.8 V_{DD}	—	V_{DD}	V	
DI26		OSCI (XT mode)	0.7 V_{DD}	—	V_{DD}	V	
DI27		OSCI (HS mode)	0.7 V_{DD}	—	V_{DD}	V	
DI28		I/O Pins with I^{2}C Buffer:					
		with Analog Functions	0.7 V_{DD}	—	V_{DD}	V	
		Digital Only	0.7 V_{DD}	—	V_{DD}	V	
DI29		I/O Pins with SMBus	2.1	—	V_{DD}	V	2.5V ≤ V_{PIN} ≤ V_{DD}
DI30	I_{CNPU}	**CNx Pull-up Current**	50	250	500	µA	V_{DD} = 3.3V, V_{PIN} = V_{SS}
DI31	I_{PU}	**Maximum Load Current for Digital High Detection w/Internal Pull-up**	—	—	30	µA	V_{DD} = 2.0V
			—	—	1000	µA	V_{DD} = 3.3V
	I_{IL}	**Input Leakage Current(2,3)**					
DI50		I/O Ports	—	0.050	±0.100	µA	V_{SS} ≤ V_{PIN} ≤ V_{DD}, Pin at high-impedance
DI51		V_{REF+}, V_{REF-}, AN0, AN1	—	0.300	±0.500	µA	V_{SS} ≤ V_{PIN} ≤ V_{DD}, Pin at high-impedance

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

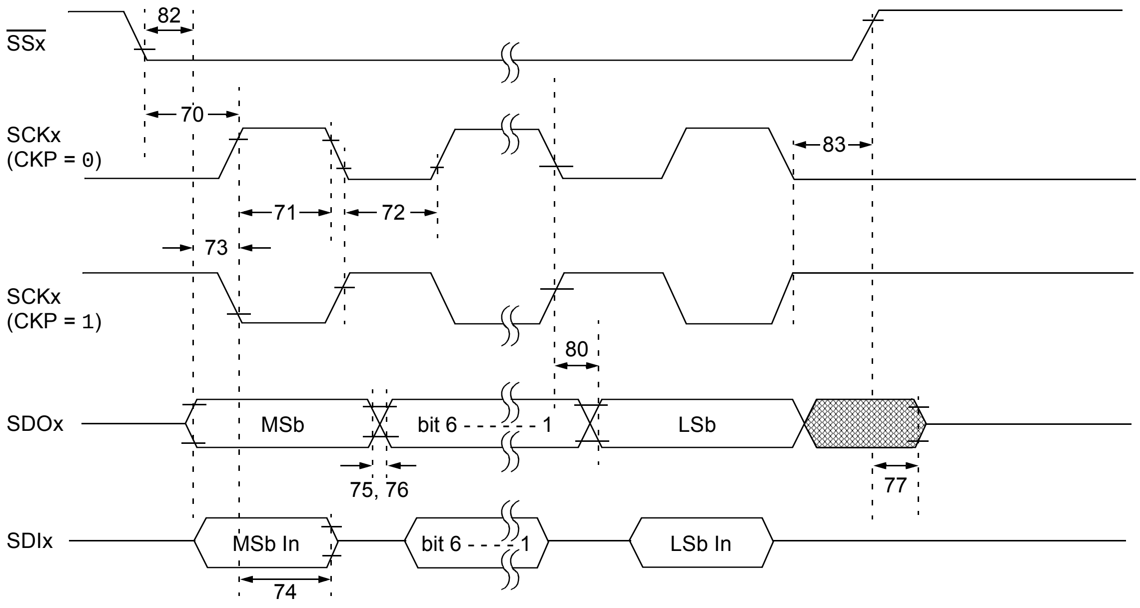
2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: Refer to Table 1-4 and Table 1-5 for I/O pin buffer types.

5: V_{IH} requirements are met when the internal pull-ups are enabled.

FIGURE 26-10: EXAMPLE SPI SLAVE MODE TIMING (CKE = 1)



Note: Refer to Figure 26-3 for load conditions.

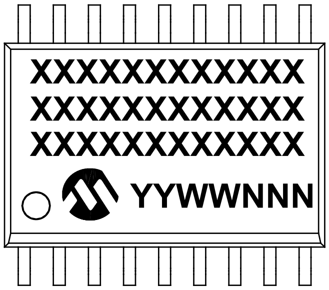
TABLE 26-30: EXAMPLE SPI SLAVE MODE REQUIREMENTS (CKE = 1)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{\text{SSx}}$ ↓ to SCKx ↓ or SCKx ↑ Input		3 Tcy	—	ns	
70A	TssL2WB	$\overline{\text{SSx}}$ to Write to SSPxBUF		3 Tcy	—	ns	
71	TscH	SCKx Input High Time (Slave mode)	Continuous	1.25 Tcy + 30	—	ns	
71A			Single Byte	40	—	ns	**(Note 1)**
72	TscL	SCKx Input Low Time (Slave mode)	Continuous	1.25 Tcy + 30	—	ns	
72A			Single Byte	40	—	ns	**(Note 1)**
73A	Tb2b	Last Clock Edge of Byte 1 to the First Clock Edge of Byte 2		1.5 Tcy + 40	—	ns	**(Note 2)**
74	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge		40	—	ns	
75	TdoR	SDOx Data Output Rise Time		—	25	ns	
76	TdoF	SDOx Data Output Fall Time		—	25	ns	
77	TssH2doZ	$\overline{\text{SSx}}$ ↑ to SDOx Output High-Impedance		10	50	ns	
80	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge		—	50	ns	
82	TssL2doV	SDOx Data Output Valid After $\overline{\text{SSx}}$ ↓ Edge		—	50	ns	
83	TscH2ssH, TscL2ssH	$\overline{\text{SSx}}$ ↑ After SCKx Edge		1.5 Tcy + 40	—	ns	
	Fsck	SCKx Frequency		—	10	MHz	

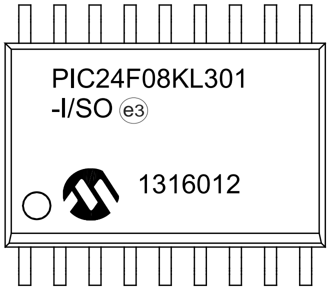
Note 1: Requires the use of Parameter 73A.

2: Only if Parameters 71A and 72A are used.

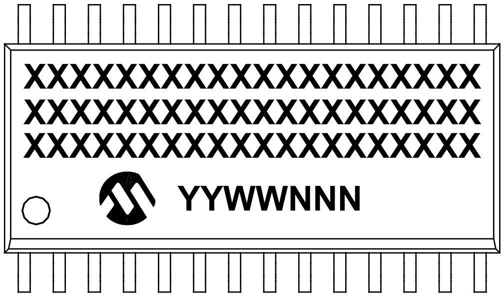
20-Lead SOIC (7.50 mm)



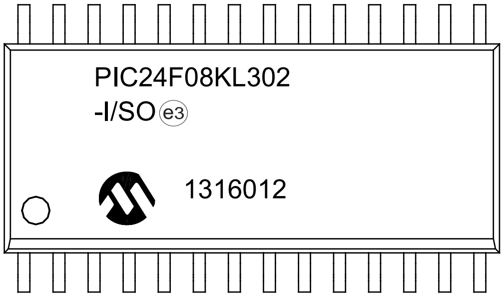
Example



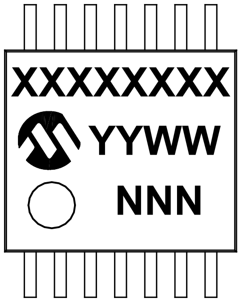
28-Lead SOIC (7.50 mm)



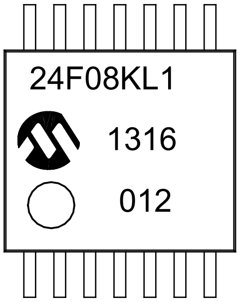
Example



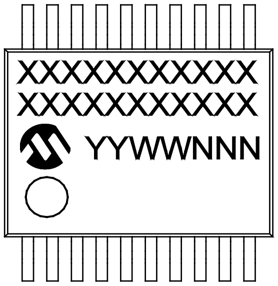
14-Lead TSSOP (4.4 mm)



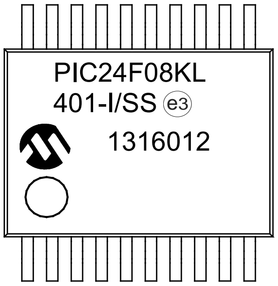
Example



20-Lead SSOP (5.30 mm)

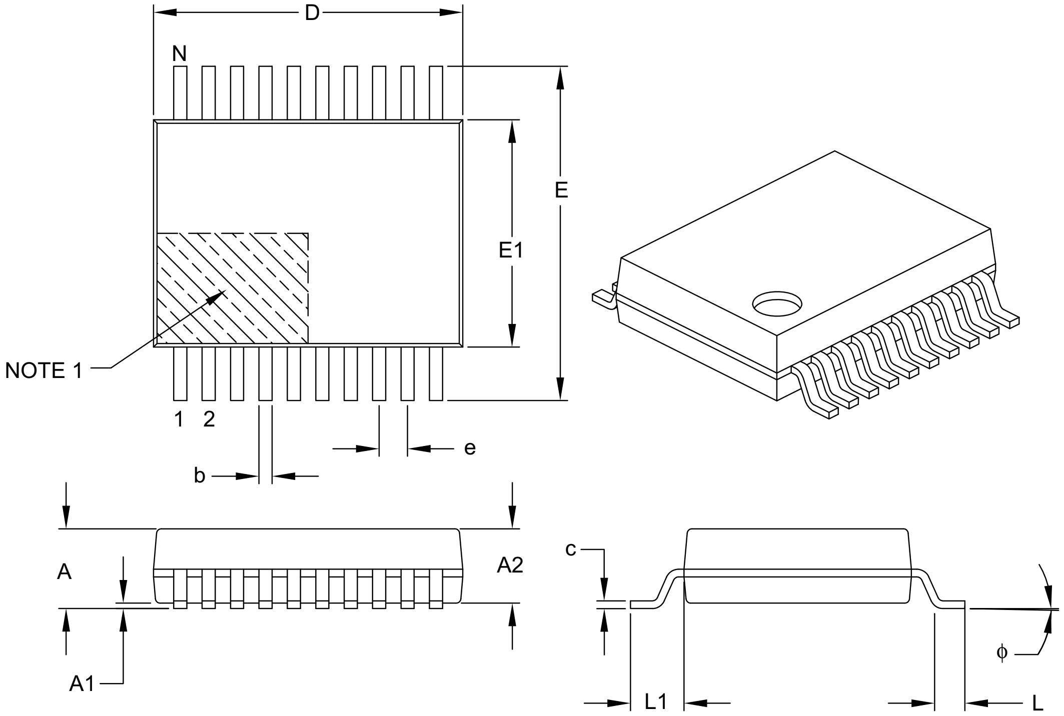


Example



20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

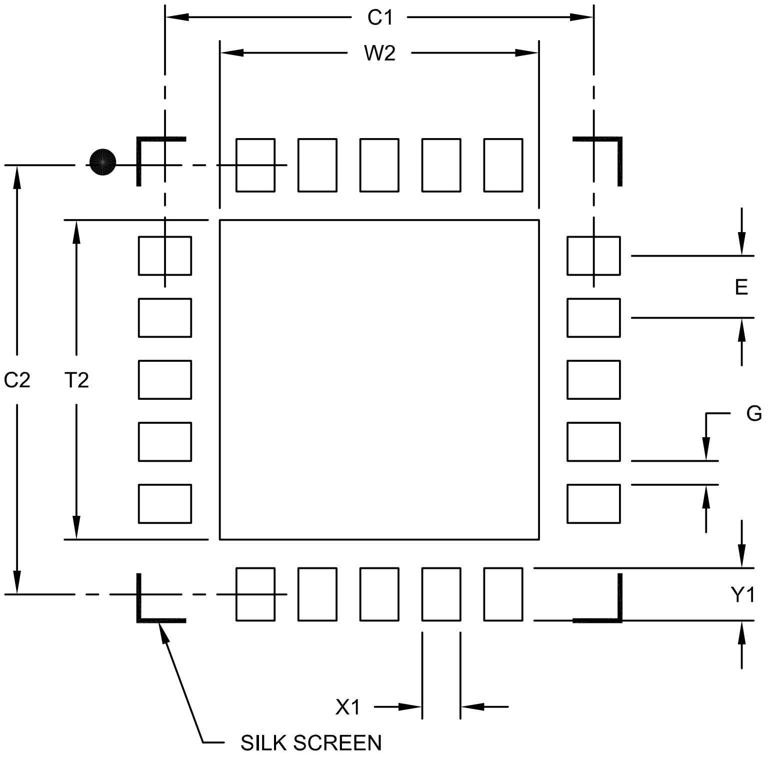
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

20-Lead Plastic Quad Flat, No Lead Package (MQ) - 5x5 mm Body [QFN] With 0.40mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			3.35
Optional Center Pad Length	T2			3.35
Contact Pad Spacing	C1		4.50	
Contact Pad Spacing	C2		4.50	
Contact Pad Width (X20)	X1			0.40
Contact Pad Length (X20)	Y1			0.55
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2139A