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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f08kl402-i-so

PIC24F16KL402 FAMILY

NOTES:

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1.2 Other Special Features

- **Communications:** The PIC24F16KL402 family incorporates multiple serial communication peripherals to handle a range of application requirements. The MSSP module implements both SPI and I²C™ protocols, and supports both Master and Slave modes of operation for each. Devices also include one of two UARTs with built-in IrDA® encoders/decoders.
- **Analog Features:** Select members of the PIC24F16KL402 family include a 10-bit A/D Converter module. The A/D module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, as well as faster sampling speeds. The comparator modules are configurable for a wide range of operations and can be used as either a single or double comparator module.

1.3 Details on Individual Family Members

Devices in the PIC24F16KL402 family are available in 14-pin, 20-pin and 28-pin packages. The general block diagram for all devices is shown in Figure 1-1.

The PIC24F16KL402 family may be thought of as four different device groups, each offering a slightly different set of features. These differ from each other in multiple ways:

- The size of the Flash program memory
- The presence and size of data EEPROM
- The presence of an A/D Converter and the number of external analog channels available
- The number of analog comparators
- The number of general purpose timers
- The number and type of CCP modules (i.e., CCP vs. ECCP)
- The number of serial communications modules (both MSSPs and UARTs)

The general differences between the different sub-families are shown in Table 1-1. The feature sets for specific devices are summarized in Table 1-2 and Table 1-3.

A list of the individual pin features available on the PIC24F16KL402 family devices, sorted by function, is provided in Table 1-4 (for PIC24FXXKL40X/30X devices) and Table 1-5 (for PIC24FXXKL20X/10X devices). Note that these tables show the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of this data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

TABLE 1-1: FEATURE COMPARISON FOR PIC24F16KL402 FAMILY GROUPS

Device Group	Program Memory (bytes)	Data EEPROM (bytes)	Timers (8/16-bit)	CCP and ECCP	Serial (MSSP/UART)	A/D (channels)	Comparators
PIC24FXXKL10X	4K	—	1/2	2/0	1/1	—	1
PIC24FXXKL20X	8K	—	1/2	2/0	1/1	7 or 12	1
PIC24FXXKL30X	8K	256	2/2	2/1	2/2	—	2
PIC24FXXKL40X	8K or 16K	512	2/2	2/1	2/2	12	2

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TABLE 1-3: DEVICE FEATURES FOR THE PIC24F16KL20X/10X DEVICES

Features	PIC24F08KL201	PIC24F04KL101	PIC24F08KL200	PIC24F04KL100
Operating Frequency	DC – 32 MHz			
Program Memory (bytes)	8K	4K	8K	4K
Program Memory (instructions)	2816	1408	2816	1408
Data Memory (bytes)	512	512	512	512
Data EEPROM Memory (bytes)	—	—	—	—
Interrupt Sources (soft vectors/NMI traps)	27 (23/4)	26 (22/4)	27 (23/4)	26 (22/4)
I/O Ports	PORTA<6:0> PORTB<15:12,9:7,4,2:0>		PORTA<5:0> PORTB<15:14,9:8,4,0>	
Total I/O Pins	17		12	
Timers (8/16-bit)	1/2	1/2	1/2	1/2
Capture/Compare/PWM modules:				
Total	2	2	2	2
Enhanced CCP	0	0	0	0
Input Change Notification Interrupt	17	17	11	11
Serial Communications:				
UART	1	1	1	1
MSSP	1	1	1	1
10-Bit Analog-to-Digital Module (input channels)	12	—	7	—
Analog Comparators	1	1	1	1
Resets (and delays)	POR, BOR, RESET Instruction, $\overline{\text{MCLR}}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)			
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations			
Packages	20-Pin PDIP/SSOP/SOIC/QFN		14-Pin PDIP/TSSOP	

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TABLE 1-5: PIC24F16KL20X/10X FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Buffer	Description
	20-Pin PDIP/ SSOP/ SOIC	20-Pin QFN	14-Pin PDIP/ TSSOP			
CVREF	17	14	11	I	ANA	Comparator Voltage Reference Output
CVREF+	2	19	2	I	ANA	Comparator Reference Positive Input Voltage
CVREF-	3	20	3	I	ANA	Comparator Reference Negative Input Voltage
HLVDIN	15	12	6	I	ST	High/Low-Voltage Detect Input
INT0	11	8	12	I	ST	Interrupt 0 Input
INT1	17	14	11	I	ST	Interrupt 1 Input
INT2	14	11	10	I	ST	Interrupt 2 Input
MCLR	1	18	1	I	ST	Master Clear (device Reset) Input. This line is brought low to cause a Reset.
OSCI	7	4	4	I	ANA	Main Oscillator Input
OSCO	8	5	5	O	ANA	Main Oscillator Output
PGEC1	5	2	—	I/O	ST	ICSP™ Clock 1
PCED1	4	1	—	I/O	ST	ICSP Data 1
PGEC2	2	19	2	I/O	ST	ICSP Clock 2
PGED2	3	20	3	I/O	ST	ICSP Data 2
PGEC3	10	7	7	I/O	ST	ICSP Clock 3
PGED3	9	6	6	I/O	ST	ICSP Data 3
RA0	2	19	2	I/O	ST	PORTA Pins
RA1	3	20	3	I/O	ST	
RA2	7	4	4	I/O	ST	
RA3	8	5	5	I/O	ST	
RA4	10	7	7	I/O	ST	
RA5	1	18	1	I	ST	
RA6	14	11	10	I/O	ST	
RB0	4	1	—	I/O	ST	PORTB Pins
RB1	5	2	—	I/O	ST	
RB2	6	3	—	I/O	ST	
RB4	9	6	6	I/O	ST	
RB7	11	8	—	I/O	ST	
RB8	12	9	8	I/O	ST	
RB9	13	10	9	I/O	ST	
RB12	15	12	—	I/O	ST	
RB13	16	13	—	I/O	ST	
RB14	17	14	11	I/O	ST	
RB15	18	15	12	I/O	ST	
REFO	18	15	12	O	—	Reference Clock Output

Legend: TTL = TTL input buffer
ANA = Analog level input/output

ST = Schmitt Trigger input buffer
I²C = I²C™/SMBus input buffer

TABLE 4-3: CPU CORE REGISTERS MAP

File Name	Start Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
WREG0	0000	Working Register 0																0000	
WREG1	0002	Working Register 1																0000	
WREG2	0004	Working Register 2																0000	
WREG3	0006	Working Register 3																0000	
WREG4	0008	Working Register 4																0000	
WREG5	000A	Working Register 5																0000	
WREG6	000C	Working Register 6																0000	
WREG7	000E	Working Register 7																0000	
WREG8	0010	Working Register 8																0000	
WREG9	0012	Working Register 9																0000	
WREG10	0014	Working Register 10																0000	
WREG11	0016	Working Register 11																0000	
WREG12	0018	Working Register 12																0000	
WREG13	001A	Working Register 13																0000	
WREG14	001C	Working Register 14																0000	
WREG15	001E	Working Register 15																—	0800
SPLIM	0020	Stack Pointer Limit Value Register																xxxxx	
PCL	002E	Program Counter Low Word Register																0000	
PCH	0030	—	—	—	—	—	—	—	—	—	Program Counter Register High Byte							0000	
TBLPAG	0032	—	—	—	—	—	—	—	—	Table Memory Page Address Register								0000	
PSVPAG	0034	—	—	—	—	—	—	—	—	Program Space Visibility Page Address Register								0000	
RCOUNT	0036	REPEAT Loop Counter Register																xxxxxx	
SR	0042	—	—	—	—	—	—	—	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000	
CORCON	0044	—	—	—	—	—	—	—	—	—	—	—	—	IPL3	PSV	—	—	0000	
DISICNT	0052	—	—	Disable Interrupts Counter Register														xxxxx	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 8-1: SR: ALU STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	DC ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2 ^(2,3)	IPL1 ^(2,3)	IPL0 ^(2,3)	RA ⁽¹⁾	N ⁽¹⁾	OV ⁽¹⁾	Z ⁽¹⁾	C ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits^(2,3)

111 = CPU Interrupt Priority Level is 7 (15); user interrupts disabled

110 = CPU Interrupt Priority Level is 6 (14)

101 = CPU Interrupt Priority Level is 5 (13)

100 = CPU Interrupt Priority Level is 4 (12)

011 = CPU Interrupt Priority Level is 3 (11)

010 = CPU Interrupt Priority Level is 2 (10)

001 = CPU Interrupt Priority Level is 1 (9)

000 = CPU Interrupt Priority Level is 0 (8)

Note 1: See Register 3-1 for the description of these bits, which are not dedicated to interrupt control functions.

2: The IPL bits are concatenated with the IPL3 bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the Interrupt Priority Level if IPL3 = 1.

3: The IPL Status bits are read-only when NSTDIS (INTCON1<15>) = 1.

Note: Bit 8 and bits 4 through 0 are described in **Section 3.0 "CPU"**.

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REGISTER 8-4: INTCON2: INTERRUPT CONTROL REGISTER2

R/W-0	R-0, HSC	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **ALTIVT:** Enable Alternate Interrupt Vector Table bit
1 = Uses Alternate Interrupt Vector Table
0 = Uses standard (default) vector table
- bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active
- bit 13-3 **Unimplemented:** Read as '0'
- bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge
- bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge
- bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

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REGISTER 8-22: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0
bit 7						bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3

Unimplemented: Read as '0'

bit 2-0

INT1IP<2:0>: External Interrupt 1 Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

-
-
-

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

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REGISTER 8-26: IPC12: INTERRUPT PRIORITY CONTROL REGISTER 12

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	BCL2IP2 ⁽¹⁾	BCL2IP1 ⁽¹⁾	BCL2IP0 ⁽¹⁾
bit 15						bit 8	

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	SSP2IP2 ⁽¹⁾	SSP2IP1 ⁽¹⁾	SSP2IP0 ⁽¹⁾	—	—	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **BCL2IP<2:0>:** MSSP2 I²C™ Bus Collision Interrupt Priority bits⁽¹⁾

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SSP2IP<2:0>:** MSSP2 SPI/I²C Event Interrupt Priority bits⁽¹⁾

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

Note 1: These bits are unimplemented on PIC24FXXKL10X and PIC24FXXKL20X devices.

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REGISTER 9-2: CLKDIV: CLOCK DIVIDER REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1
ROI	DOZE2	DOZE1	DOZE0	DOZEN ⁽¹⁾	RCDIV2	RCDIV1	RCDIV0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ROI:** Recover on Interrupt bit

1 = Interrupts clear the DOZEN bit, and reset the CPU and peripheral clock ratio to 1:1

0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE<2:0>:** CPU-to-Peripheral Clock Ratio Select bits

111 = 1:128

110 = 1:64

101 = 1:32

100 = 1:16

011 = 1:8

010 = 1:4

001 = 1:2

000 = 1:1

bit 11 **DOZEN:** DOZE Enable bit⁽¹⁾

1 = DOZE<2:0> bits specify the CPU-to-peripheral clock ratio

0 = CPU and the peripheral clock ratio are set to 1:1

bit 10-8 **RCDIV<2:0>:** FRC Postscaler Select bits

When COSC<2:0> (OSCCON<14:12>) = 111 or 001:

111 = 31.25 kHz (divide-by-256)

110 = 125 kHz (divide-by-64)

101 = 250 kHz (divide-by-32)

100 = 500 kHz (divide-by-16)

011 = 1 MHz (divide-by-8)

010 = 2 MHz (divide-by-4)

001 = 4 MHz (divide-by-2) (default)

000 = 8 MHz (divide-by-1)

When COSC<2:0> (OSCCON<14:12>) = 110:

111 = 1.95 kHz (divide-by-256)

110 = 7.81 kHz (divide-by-64)

101 = 15.62 kHz (divide-by-32)

100 = 31.25 kHz (divide-by-16)

011 = 62.5 kHz (divide-by-8)

010 = 125 kHz (divide-by-4)

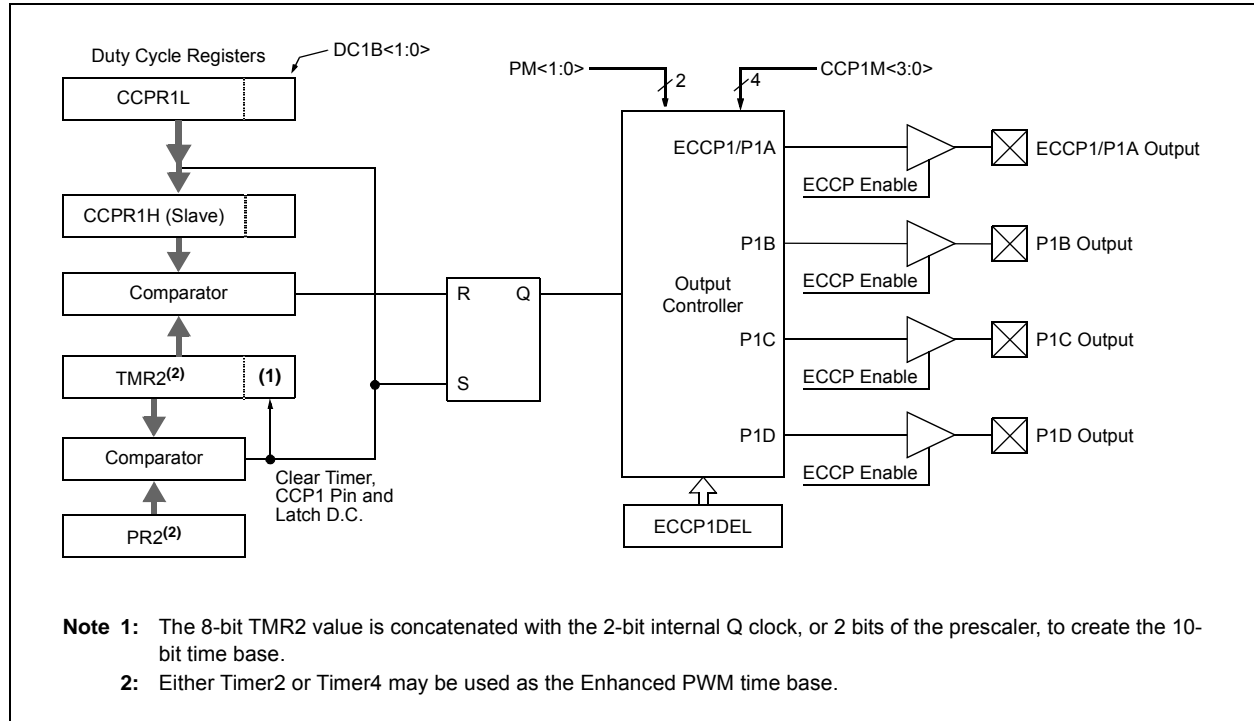
001 = 250 kHz (divide-by-2) (default)

000 = 500 kHz (divide-by-1)

bit 7-0 **Unimplemented:** Read as '0'

Note 1: This bit is automatically cleared when the ROI bit is set and an interrupt occurs.

FIGURE 16-4: SIMPLIFIED BLOCK DIAGRAM OF ENHANCED PWM MODE



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REGISTER 16-1: CCPxCON: CCPx CONTROL REGISTER (STANDARD CCP MODULES)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DCxB1	DCxB0	CCPxM3 ⁽¹⁾	CCPxM2 ⁽¹⁾	CCPxM1 ⁽¹⁾	CCPxM0 ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-4 **DCxB<1:0>:** PWM Duty Cycle Bit 1 and Bit 0 for CCPx Module bits

Capture and Compare modes:

Unused.

PWM mode:

These bits are the two Least Significant bits (bit 1 and bit 0) of the 10-bit PWM duty cycle. The eight Most Significant bits (DCxB<9:2>) of the duty cycle are found in CCPRxL.

bit 3-0 **CCPxM<3:0>:** CCPx Module Mode Select bits⁽¹⁾

1111 = Reserved

1110 = Reserved

1101 = Reserved

1100 = PWM mode

1011 = Compare mode: Special Event Trigger; resets timer on CCPx match (CCPxIF bit is set)

1010 = Compare mode: Generates software interrupt on compare match (CCPxIF bit is set, CCPx pin reflects I/O state)

1001 = Compare mode: Initializes CCPx pin high; on compare match, forces CCPx pin low (CCPxIF bit is set)

1000 = Compare mode: Initializes CCPx pin low; on compare match, forces CCPx pin high (CCPxIF bit is set)

0111 = Capture mode: Every 16th rising edge

0110 = Capture mode: Every 4th rising edge

0101 = Capture mode: Every rising edge

0100 = Capture mode: Every falling edge

0011 = Reserved

0010 = Compare mode: Toggles output on match (CCPxIF bit is set)

0001 = Reserved

0000 = Capture/Compare/PWM is disabled (resets CCPx module)

Note 1: CCPxM<3:0> = 1011 will only reset the timer and not start the A/D conversion on a CCPx match.

17.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on MSSP, refer to the “*dsPIC33/PIC24 Family Reference Manual*”.

The Master Synchronous Serial Port (MSSP) module is an 8-bit serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, Shift registers, display drivers, A/D Converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C™)
 - Full Master mode
 - Slave mode (with general address call)

The SPI interface supports these modes in hardware:

- Master mode
- Slave mode
- Daisy-Chaining Operation in Slave mode
- Synchronized Slave operation

The I²C interface supports the following modes in hardware:

- Master mode
- Multi-Master mode
- Slave mode with 10-Bit And 7-Bit Addressing and Address Masking
- Byte NACKing
- Selectable Address and Data Hold and Interrupt Masking

17.1 I/O Pin Configuration for SPI

In SPI Master mode, the MSSP module will assert control over any pins associated with the SDOx and SCKx outputs. This does not automatically disable other digital functions associated with the pin, and may result in the module driving the digital I/O port inputs. To prevent this, the MSSP module outputs must be disconnected from their output pins while the module is in SPI Master mode. While disabling the module temporarily may be an option, it may not be a practical solution in all applications.

The SDOx and SCKx outputs for the module can be selectively disabled by using the SDOxDIS and SCKxDIS bits in the PADCFG1 register (Register 17-10). Setting the bit disconnects the corresponding output for a particular module from its assigned pin.

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REGISTER 17-2: SSPxSTAT: MSSPx STATUS REGISTER (I²C™ MODE) (CONTINUED)

bit 0 **BF:** Buffer Full Status bit

In Transmit mode:

1 = Transmit is in progress, SSPxBUF is full

0 = Transmit is complete, SSPxBUF is empty

In Receive mode:

1 = SSPxBUF is full (does not include the $\overline{\text{ACK}}$ and Stop bits)

0 = SSPxBUF is empty (does not include the $\overline{\text{ACK}}$ and Stop bits)

- Note 1:** This bit is cleared on `RESET` and when `SSPEN` is cleared.
- 2:** This bit holds the $\text{R}/\overline{\text{W}}$ bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit or not $\overline{\text{ACK}}$ bit.
- 3:** ORing this bit with `SEN`, `RSEN`, `PEN`, `RCEN` or `ACKEN` will indicate if the MSSPx is in Active mode.

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REGISTER 18-1: UxMODE: UARTx MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0 ⁽²⁾	R/W-0 ⁽²⁾
UARTEN	—	USIDL	IREN ⁽¹⁾	RTSMD	—	UEN1	UEN0
bit 15						bit 8	

R/C-0, HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7						bit 0	

Legend:	C = Clearable bit	HC = Hardware Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15 **UARTEN:** UARTx Enable bit
1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>
0 = UARTx is disabled; all UARTx pins are controlled by port latches, UARTx power consumption is minimal
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **USIDL:** UARTx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode
- bit 12 **IREN:** IrDA[®] Encoder and Decoder Enable bit⁽¹⁾
1 = IrDA encoder and decoder are enabled
0 = IrDA encoder and decoder are disabled
- bit 11 **RTSMD:** Mode Selection for UxRTS Pin bit
1 = UxRTS pin is in Simplex mode
0 = UxRTS pin is in Flow Control mode
- bit 10 **Unimplemented:** Read as '0'
- bit 9-8 **UEN<1:0>:** UARTx Enable bits⁽²⁾
11 = UxTX, UxRX and UxBCLK pins are enabled and used; UxCTS pin is controlled by port latches
10 = UxTX, UxRX, UxCTS and UxRTS pins are enabled and used
01 = UxTX, UxRX and UxRTS pins are enabled and used; UxCTS pin is controlled by port latches
00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/UxBCLK pins are controlled by port latches
- bit 7 **WAKE:** Wake-up on Start Bit Detect During Sleep Mode Enable bit
1 = UARTx will continue to sample the UxRX pin; interrupt is generated on the falling edge, bit is cleared in hardware on the following rising edge
0 = No wake-up is enabled
- bit 6 **LPBACK:** UARTx Loopback Mode Select bit
1 = Enables Loopback mode
0 = Loopback mode is disabled
- bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h); cleared in hardware upon completion
0 = Baud rate measurement is disabled or completed
- bit 4 **RXINV:** Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

Note 1: This feature is only available for the 16x BRG mode (BRGH = 0).

2: Bit availability depends on pin availability.

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REGISTER 19-1: AD1CON1: A/D CONTROL REGISTER 1

R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
ADON ⁽¹⁾	—	ADSIDL	—	—	—	FORM1	FORM0
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0, HSC	R-0, HSC
SSRC2	SSRC1	SSRC0	—	—	ASAM	SAMP	DONE
bit 7						bit 0	

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **ADON:** A/D Operating Mode bit⁽¹⁾
 1 = A/D Converter module is operating
 0 = A/D Converter is off
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **ADSIDL:** A/D Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12-10 **Unimplemented:** Read as '0'
- bit 9-8 **FORM<1:0>:** Data Output Format bits
 11 = Signed fractional (sddd dddd dd00 0000)
 10 = Fractional (dddd dddd dd00 0000)
 01 = Signed integer (ssss sssd dddd dddd)
 00 = Integer (0000 00dd dddd dddd)
- bit 7-5 **SSRC<2:0>:** Conversion Trigger Source Select bits
 111 = Internal counter ends sampling and starts conversion (auto-convert)
 110 = Reserved
 101 = Reserved
 100 = Reserved
 011 = Reserved
 010 = Timer1 compare ends sampling and starts conversion
 001 = Active transition on INT0 pin ends sampling and starts conversion
 000 = Clearing the SAMP bit ends sampling and starts conversion
- bit 4-3 **Unimplemented:** Read as '0'
- bit 2 **ASAM:** A/D Sample Auto-Start bit
 1 = Sampling begins immediately after the last conversion completes; SAMP bit is auto-set
 0 = Sampling begins when the SAMP bit is set
- bit 1 **SAMP:** A/D Sample Enable bit
 1 = A/D Sample-and-Hold amplifier is sampling input
 0 = A/D Sample-and-Hold amplifier is holding
- bit 0 **DONE:** A/D Conversion Status bit
 1 = A/D conversion is done
 0 = A/D conversion is not done

Note 1: Values of ADC1BUFx registers will not retain their values once the ADON bit is cleared. Read out the conversion values from the buffer before disabling the module.

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REGISTER 22-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
HLVDEN	—	HLSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VDIR	BGVST	IRVST	—	HLVDL3	HLVDL2	HLVDL1	HLVDL0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **HLVDEN:** High/Low-Voltage Detect Power Enable bit

1 = HLVD is enabled

0 = HLVD is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **HLSIDL:** HLVD Stop in Idle Mode bit

1 = Discontinues module operation when the device enters Idle mode

0 = Continues module operation in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **VDIR:** Voltage Change Direction Select bit

1 = Event occurs when the voltage equals or exceeds the trip point (HLVDL<3:0>)

0 = Event occurs when the voltage equals or falls below the trip point (HLVDL<3:0>)

bit 6 **BGVST:** Band Gap Voltage Stable Flag bit

1 = Indicates that the band gap voltage is stable

0 = Indicates that the band gap voltage is unstable

bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit

1 = Indicates that the internal reference voltage is stable and the High-Voltage Detect logic generates the interrupt flag at the specified voltage range

0 = Indicates that the internal reference voltage is unstable and the High-Voltage Detect logic will not generate the interrupt flag at the specified voltage range, and the HLVD interrupt should not be enabled

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **HLVDL<3:0>:** High/Low-Voltage Detection Limit bits

1111 = External analog input is used (input comes from the HLVDIN pin)

1110 = Trip Point 14⁽¹⁾

1101 = Trip Point 13⁽¹⁾

1100 = Trip Point 12⁽¹⁾

.

.

.

0000 = Trip Point 0⁽¹⁾

Note 1: For the actual trip point, see **Section 26.0 “Electrical Characteristics”**.

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FIGURE 26-6: CAPTURE/COMPARE/PWM TIMINGS (ECCP1, ECCP2 MODULES)

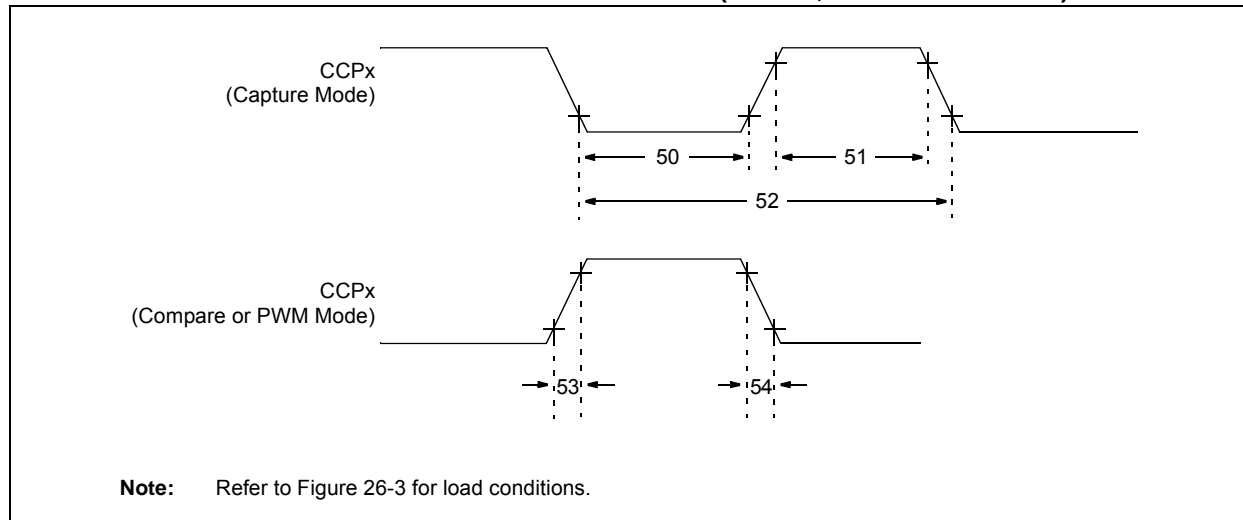


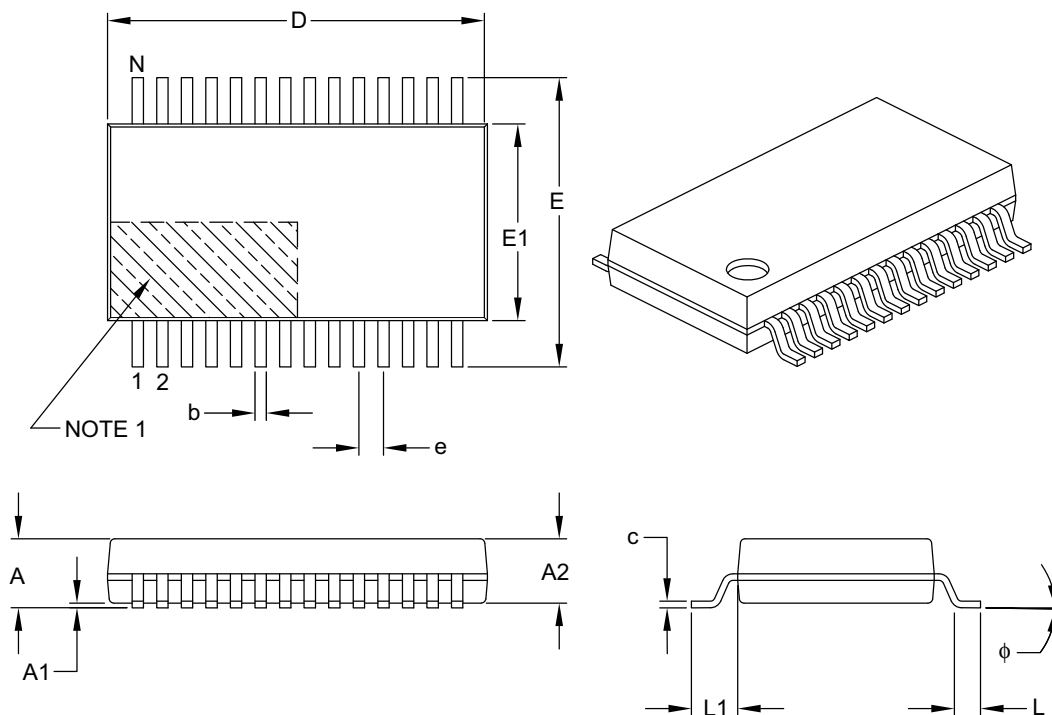
TABLE 26-26: CAPTURE/COMPARE/PWM REQUIREMENTS (ECCP1, ECCP2 MODULES)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
50	TccL	CCPx Input Low Time	No Prescaler	$0.5 T_{CY} + 20$	—	ns	
			With Prescaler	20	—	ns	
51	TccH	CCPx Input High Time	No Prescaler	$0.5 T_{CY} + 20$	—	ns	
			With Prescaler	20	—	ns	
52	TccP	CCPx Input Period		Greater of: 40 or $\frac{2 T_{CY} + 40}{N}$	—	ns	N = prescale value (1, 4 or 16)
53	TccR	CCPx Output Fall Time		—	25	ns	
54	TccF	CCPx Output Fall Time		—	25	ns	

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28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		28		
Pitch	e		0.65 BSC		
Overall Height	A		–	–	2.00
Molded Package Thickness	A2		1.65	1.75	1.85
Standoff	A1		0.05	–	–
Overall Width	E		7.40	7.80	8.20
Molded Package Width	E1		5.00	5.30	5.60
Overall Length	D		9.90	10.20	10.50
Foot Length	L		0.55	0.75	0.95
Footprint	L1		1.25 REF		
Lead Thickness	c		0.09	–	0.25
Foot Angle	φ		0°	4°	8°
Lead Width	b		0.22	–	0.38

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

PIC24F16KL402 FAMILY

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

	PIC	24	F	16	KL4	02	T	- I / PT	- XXX
Microchip Trademark	_____	_____	_____	_____	_____	_____	_____	_____	_____
Architecture	_____	_____	_____	_____	_____	_____	_____	_____	_____
Flash Memory Family	_____	_____	_____	_____	_____	_____	_____	_____	_____
Program Memory Size (Kbytes)	_____	_____	_____	_____	_____	_____	_____	_____	_____
Product Group	_____	_____	_____	_____	_____	_____	_____	_____	_____
Pin Count	_____	_____	_____	_____	_____	_____	_____	_____	_____
Tape and Reel Flag (if applicable)	_____	_____	_____	_____	_____	_____	_____	_____	_____
Temperature Range	_____	_____	_____	_____	_____	_____	_____	_____	_____
Package	_____	_____	_____	_____	_____	_____	_____	_____	_____
Pattern	_____	_____	_____	_____	_____	_____	_____	_____	_____

Architecture	24	= 16-bit modified Harvard without DSP
Flash Memory Family	F	= Standard voltage range Flash program memory
Product Group	KL4 KL3 KL2 KL1	= General purpose microcontrollers
Pin Count	00 01 02	= 14-pin = 20-pin = 28-pin
Temperature Range	I E	= -40°C to +85°C (Industrial) = -40°C to +125°C (Extended)
Package	SP SO SS ST ML, MQ P	= SPDIP = SOIC = SSOP = TSSOP = QFN = PDIP
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES	= Engineering Sample

Examples:

- a) PIC24F16KL402-I/ML: General Purpose, 16-Kbyte Program Memory, 28-Pin, Industrial Temperature, QFN Package
- b) PIC24F04KL101T-I/SS: General Purpose, 4-Kbyte Program Memory, 20-Pin, Industrial Temperature, SSOP Package, Tape-and-Reel