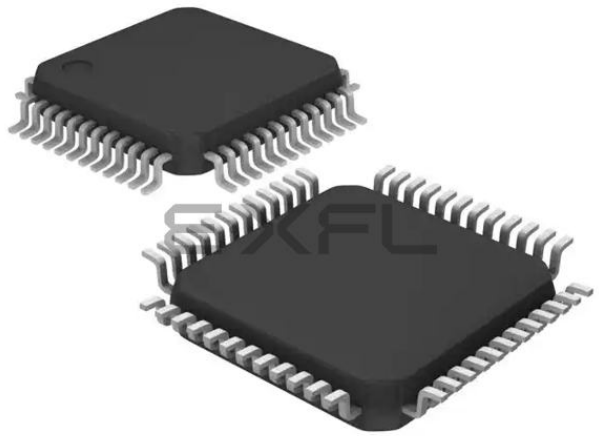

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVR, I²S, PWM
Number of I/O	41
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m0564le4ae

2 FEATURES

2.1 NuMicro® M0564 Features

- Core
  - ARM® Cortex®-M0 core running up to 72 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Supports programmable mask-able interrupts
  - Serial Wire Debug supports with 2 watch-points/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5V to 5.5V
- Flash Memory
  - Supports 256/128 KB application ROM (APROM)
  - Supports 4 KB Flash for loader (LDROM)
  - Supports 2 KB Security Protection Rom (SPROM)
  - Supports 12 bytes User Configuration block to control system initiation
  - Supports Data Flash with configurable memory size
  - Supports 2 KB page erase for all embedded flash
  - Supports In-System-Programming (ISP), In-Application-Programming (IAP) update embedded flash memory
  - Supports CRC-32 checksum calculation function
  - Supports flash all one verification function
  - Hardware external read protection of whole flash memory by Security Lock Bit
  - Supports 2-wired ICP update through SWD/ICE interface
- SRAM Memory
  - 20 KB embedded SRAM
  - Supports byte-, half-word- and word-access
  - Supports PDMA mode
- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Write divisor to trigger calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
- PDMA (Peripheral DMA)
  - Supports 5 independent configurable channels for automatic data transfer between memories and peripherals
  - Supports single and burst transfer type
  - Supports Normal and Scatter-Gather Transfer modes
  - Supports two types of priorities modes: Fixed-priority and Round-robin modes
  - Supports byte-, half-word- and word-access
  - Supports incrementing mode for the source and destination address for each channel
  - Supports time-out function for channel 0 and channel 1
  - Supports software and SPI/I2S, UART, USCI, ADC, PWM and TIMER request
- Clock Control

- Supports 16-bit resolution PWM counter, each timer provides 1 PWM counter
- Supports up, down and up/down counter operation type
- Supports one-shot or Auto-reload counter operation mode
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
- Supports interrupt when PWM counter match zero, period value or compared value, and brake condition happened
- Supports trigger ADC when PWM counter match zero, period value or compared value

- Watchdog Timer
  - Supports multiple clock sources from LIRC(default selection), HCLK/2048 and LXT
    8 selectable time-out period from 1.6ms ~ 26.0sec (depending on clock source)
  - Able to wake up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
  - Supports multiple clock sources from HCLK/2048 (default selection) and LIRC
    Window set by 6-bit counter with 11-bit prescale
  - Interrupt or reset selectable on time-out
- RTC
  - Supports separate battery power pin V_{BAT}
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Supports Alarm mask registers
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports wake-up function
- PWM
  - Supports maximum clock frequency up to144MHz
  - Supports up to two PWM modules, each module provides 6 output channels.
  - Supports independent mode for PWM output/Capture input channel
  - Supports complementary mode for 2 complementary paired PWM output channel
    - Dead-time insertion with 12-bit resolution
    - Two compared values during one period
  - Supports 12-bit pre-scalar from 1 to 4096
  - Supports 16-bit resolution PWM counter
    - Up, down and up/down counter operation type
  - Supports mask function and tri-state enable for each PWM pin
  - Supports brake function
    - Brake source from pin and system safety events: clock failed, Brown-out detection and CPU lockup.
    - Noise filter for brake source from pin
    - Edge detect brake source to control brake state until brake interrupt cleared
    - Level detect brake source to auto recover function after brake condition removed
  - Supports interrupt on the following events:
    - PWM counter match zero, period value or compared value
    - Brake condition happened
  - Supports trigger ADC on the following events:

channel
- Supports digital comparator to monitor conversion result and user can select whether to generate an interrupt when conversion result matches the compare register setting
- An A/D conversion can be triggered by:
  - Software enable
  - External pin (STADC)
  - Timer 0~3 overflow pulse trigger
  - PWM triggers with optional start delay period
- Supports 4 internal channels for
  - Operational amplifier output
  - Band-gap VBG input
  - Temperature sensor input
  - VBAT voltage measure
- Supports internal reference voltage: 2.048V, 2.560V, 3.072V and 4.096V
- Supports PDMA transfer

- Analog Comparator
  - Supports up to 2 rail-to-rail analog comparators
  - Supports 4 multiplexed I/O pins at positive node.
  - Supports I/O pin and internal voltages at negative node
  - Support selectable internal voltage reference from:
    - Band-gap V_{BG}
    - Voltage divider source from AV_{DD} and internal reference voltage.
  - Supports programmable hysteresis
  - Supports programmable speed and power consumption
  - Interrupts generated when compare results change, interrupt event condition is programmable.
  - Supports power-down wake-up
  - Supports triggers for break events and cycle-by-cycle control for PWM
- Cyclic Redundancy Calculation Unit
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - Programmable initial value
  - Supports programmable order reverse setting for input data and CRC checksum
  - Supports programmable 1's complement setting for input data and CRC checksum.
  - Supports 8/16/32-bit of data width
  - Interrupt generated once checksum error occurs
- User Configurable VDD1=1.8~5.5V IO Interface
  - Supports UART0, SPI0 and I2C0
- Supports 96-bit Unique ID (UID)
- Supports 128-bit Unique Customer ID (UCID)
- One built-in temperature sensor with 1℃ resolution
- Brown-out detector
  - With 8 levels: 4.3 V/ 3.7V/ 2.7V/ 2.2V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 2.0 V
- Power consumption
  - Chip power down current < 10 uA with RAM data retention.
  - V_{BAT} power domain operating current <1.5 uA
- Operating Temperature: -40℃~105℃

- Packages
  - All Green package (RoHS)
  - LQFP 100-pin
  - LQFP 64-pin(7mmx7mm)
  - LQFP 48-pin

4.2.2 NuMicro® M0564 Base Series LQFP64 Pin Diagram

Corresponding Part Number: M0564SE4AE, M0564SG4AE

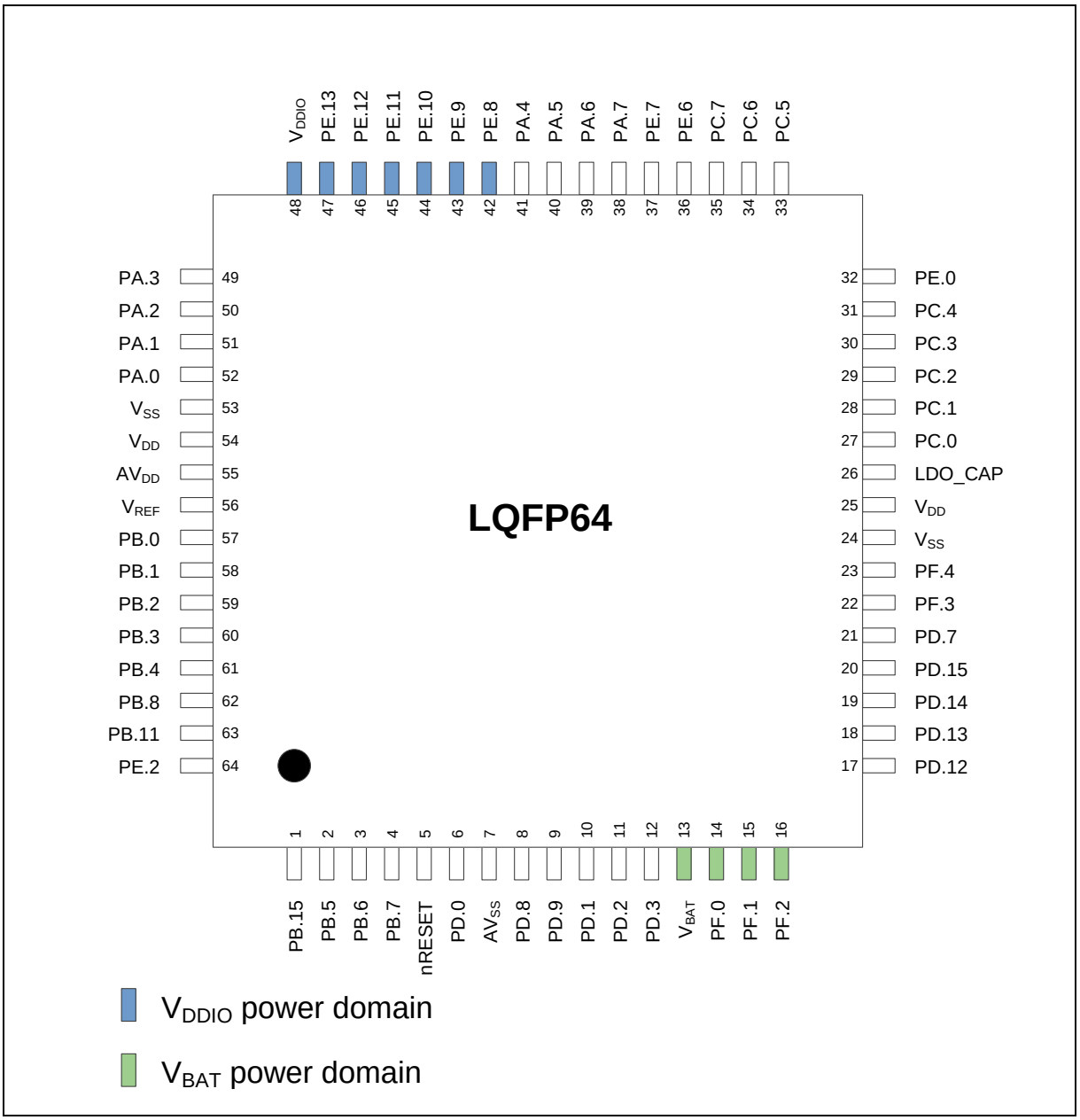


Figure 4.2-2 NuMicro® M0564 Base Series LQFP 64-pin Diagram

Group	Pin Name	GPIO	MFP	Type	Description
		PD.13	MFP3	I	
		PE.6	MFP3	I	
		PA.3	MFP2	I	
	UART0_TXD	PD.1	MFP3	O	UART0 data transmitter output pin.
		PD.12	MFP3	O	
		PE.7	MFP3	O	
		PA.2	MFP2	O	
	UART0_nCTS	PD.8	MFP3	I	UART0 clear to Send input pin.
		PD.14	MFP3	I	
		PA.2	MFP3	I	
	UART0_nRTS	PC.8	MFP3	O	UART0 request to Send output pin.
		PD.15	MFP3	O	
		PA.3	MFP3	O	
UART1	UART1_RXD	PA.9	MFP3	I	UART1 data receiver input pin.
		PE.9	MFP1	I	
		PE.13	MFP3	I	
		PA.1	MFP3	I	
		PA.12	MFP4	I	
		PB.2	MFP4	I	
	UART1_TXD	PA.8	MFP3	O	UART1 data transmitter output pin.
		PE.8	MFP1	O	
		PE.12	MFP3	O	
		PA.0	MFP3	O	
		PA.13	MFP4	O	
		PB.3	MFP4	O	
	UART1_nCTS	PA.10	MFP3	I	UART1 clear to Send input pin.
		PE.10	MFP3	I	
		PA.0	MFP1	I	
		PB.4	MFP4	I	
	UART1_nRTS	PA.11	MFP3	O	UART1 request to Send output pin.
		PE.11	MFP3	O	
		PA.1	MFP1	O	

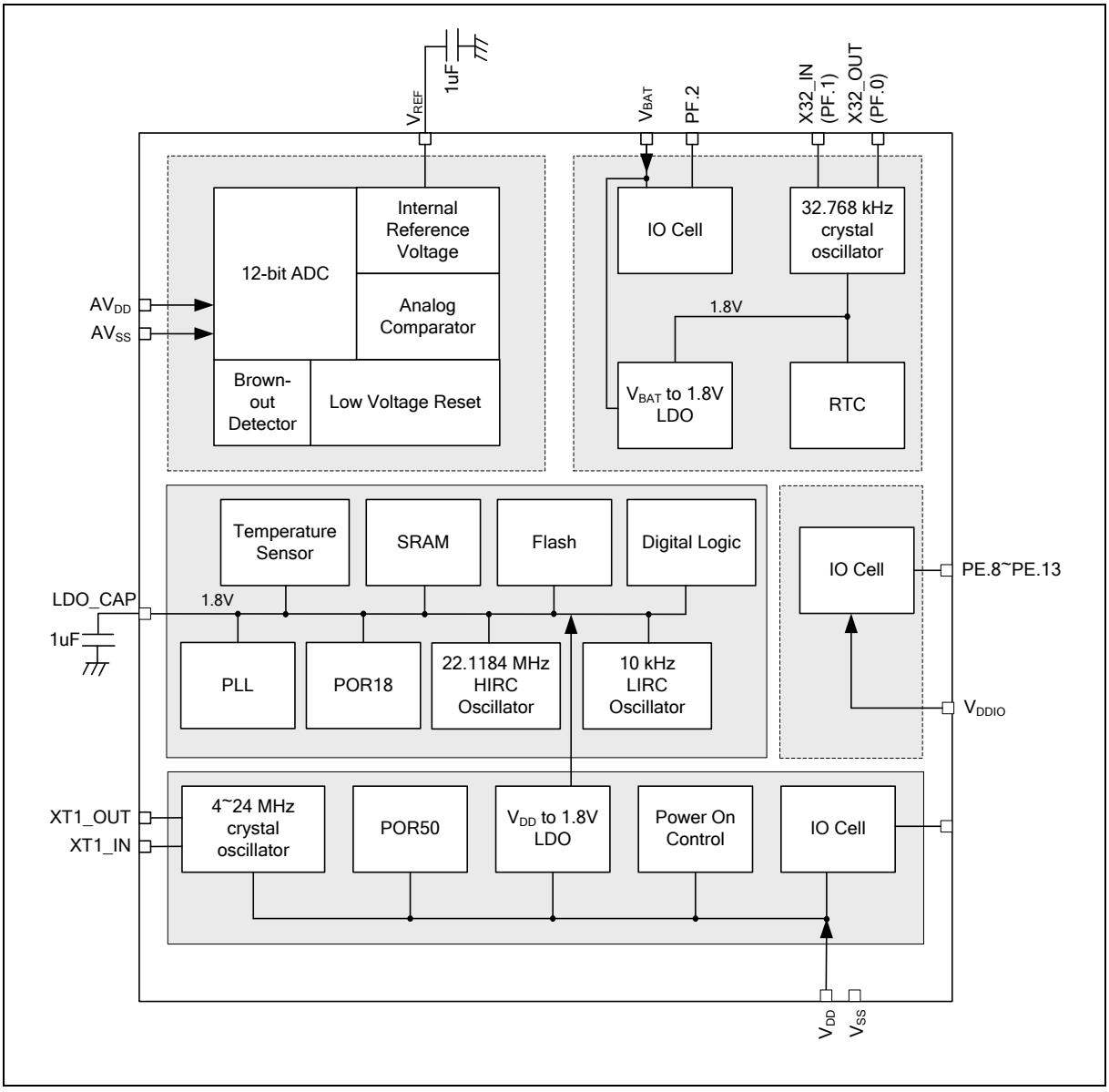


Figure 6.2-7 NuMicro® M0564 Power Distribution Diagram

according to the accurate LXT (32.768 kHz crystal oscillator), automatically gets accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 22.1184 MHz clock. In such case, if users do not want to use PLL as the system clock source, they need to solder 32.768 kHz crystal in system, and set FREQSEL (SYS_IRCTCTL0[1:0] trim frequency selection) to “01”, set REFCKSEL (SYS_IRCTCTL0[9] reference clock selection) to “0”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[0] HIRC frequency lock status) “1” indicates the HIRC0 output frequency is accurate within 0.25% deviation. To get better results, it is recommended to set both LOOPSEL (SYS_IRCTCTL[5:4] trim calculation loop) and RETRYCNT (SYS_IRCTCTL[7:6] trim value update limitation count) to “11”.

6.2.9 UART1_TXD modulation with PWM

This chip supports UART1_TXD to modulate with PWM channel. User can set MODPWMSEL(SYS_MODCTL[6:4]) to choice which PWM0 channel to modulate with UART1_TXD and set MODEN(SYS_MODCTL[0]) to enable modulation function. User can set TXDINV(UART_LINE[8]) to inverse UART1_TXD before moulating with PWM.

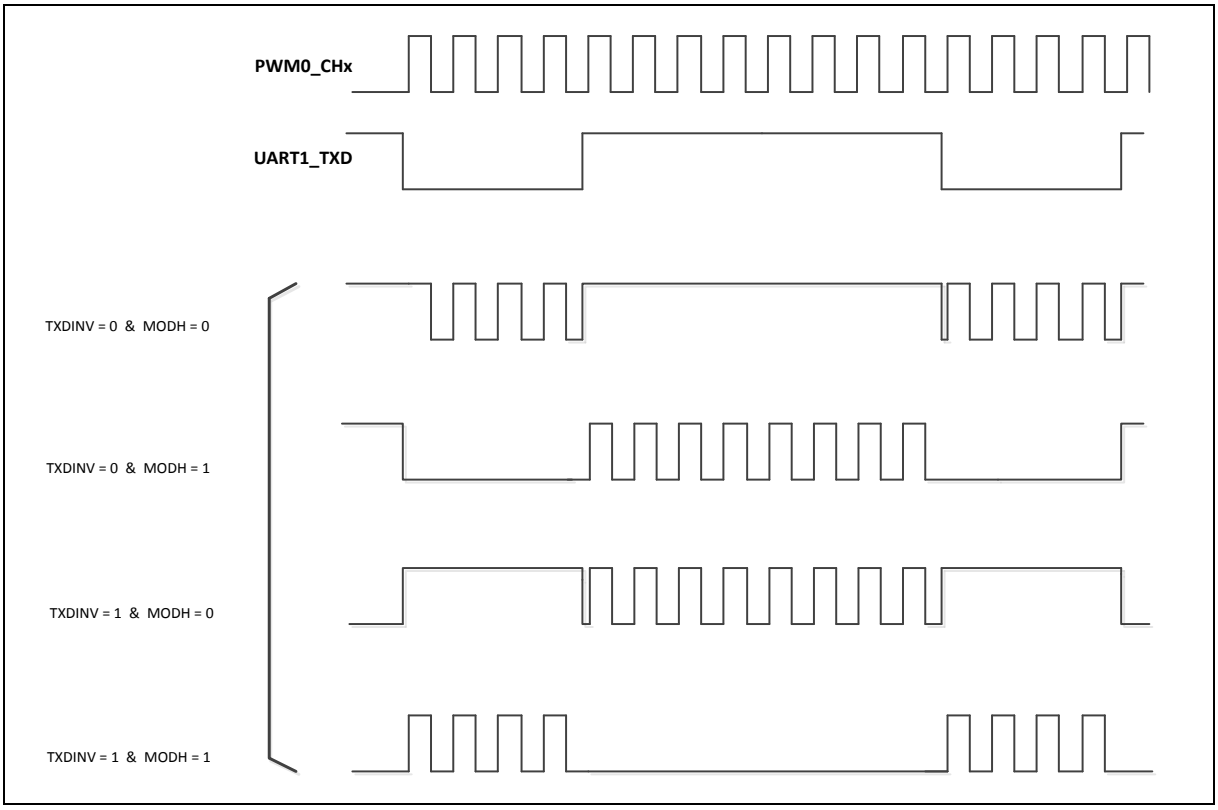


Figure 6.2-10 UART1_TXD Modulated with PWM Channel

6.2.10 Voltage Detector (VDET)

This chip supports low power comparator to detect external voltage. User can control Bandgap active interval and comparator active interval to achieve low power detection purpose. There is no debounce function in Power-down mode since no HCLK available in Power-down mode.

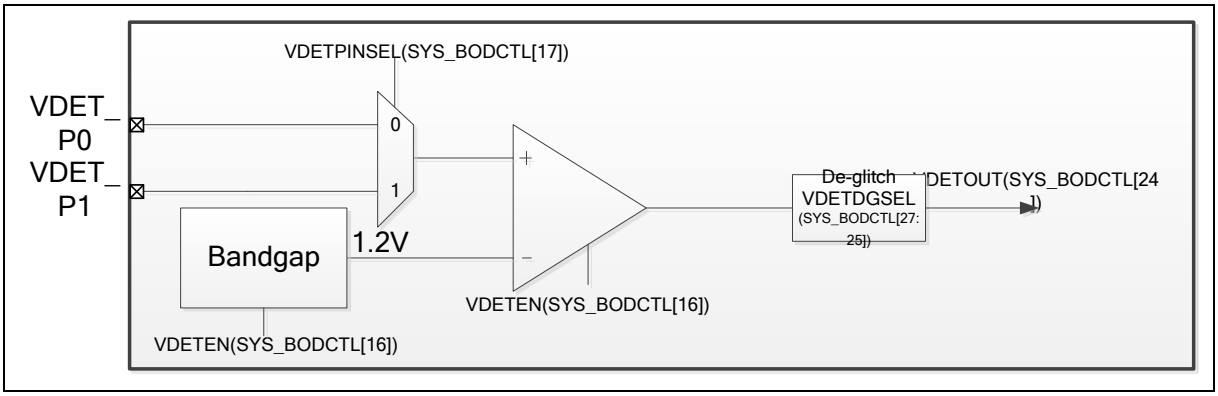


Figure 6.2-11 VDET Block Diagram

6.2.12 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”, which is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler Mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one’s priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.12.1 Exception Model and System Interrupt Map

Table 6.2-6 lists the exception model supported by the M0564 series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Type	Vector Number	Vector Address	Priority
Reset	1	0x00000004	-3
NMI	2	0x00000008	-2
Hard Fault	3	0x0000000C	-1
Reserved	4 ~ 10		Reserved
SVCall	11	0x0000002C	Configurable
Reserved	12 ~ 13		Reserved
PendSV	14	0x00000038	Configurable

6.4 Flash Memeory Controller (FMC)

6.4.1 Overview

The M0564 series is equipped with 128/256 Kbytes on-chip embedded flash for application and configurable Data Flash to store some application dependent data. A User Configuration block provides for system initiation. A 4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. A 2 Kbytes security protection ROM (SPROM) can conceal user program. A 4KB cache with zero wait cycle is used to improve flash access performance. This chip also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded flash updated.

6.4.2 Features

- Supports 128/256 Kbytes application ROM (APROM).
- Supports 4 Kbytes loader ROM (LDROM).
- Supports 2 Kbytes security protection ROM (SPROM) to conceal user program.
- Supports Data Flash with configurable memory size.
- Supports 12 bytes User Configuration block to control system initiation.
- Supports 2 Kbytes page erase for all embedded flash.
- Supports 32-bit/64-bit and multi-word flash programming function.
- Supports CRC-32 checksum calculation function.
- Supports flash all one verification function.
- Supports embedded SRAM remap to system vector memory.
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded flash memory.
- Supports cache memory to improve flash access performance and reduce power consumption.

6.7 CRC Controller (CRC)

6.7.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

6.7.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to program DATA (CRC_DAT[31:0]) to perform CRC operation

In Independent mode, there are mask control, brake control, polarity control and output enable control to control output waveform as shown in Figure 6.17-12.

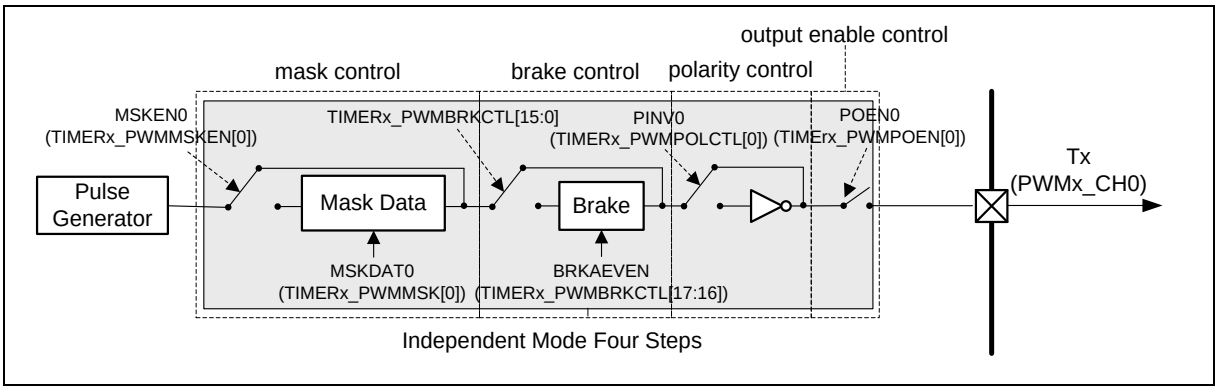


Figure 6.17-12 PWMx_CH0 Output Control in Independent Mode

In complementary mode, there are dead-time insertion control and four control steps the same as independent mode to control PWMx_CH0 and PWMx_CH1 outputs as shown in Figure 6.17-13.

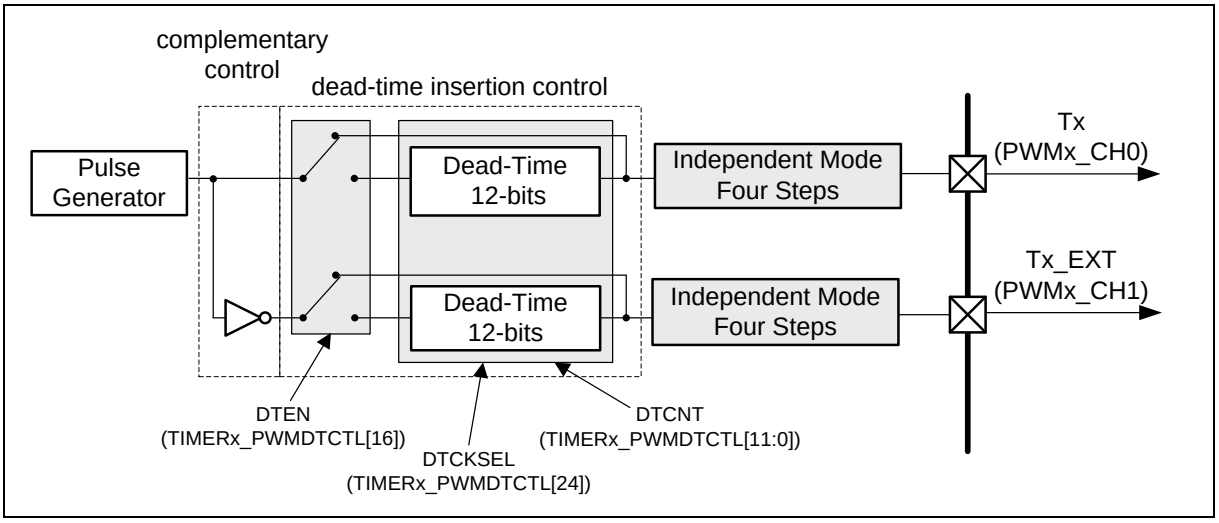


Figure 6.17-13 PWMx_CH0 and PWMx_CH1 Output Control in Complementary Mode

6.17.3.15 Dead-Time Insertion Control

In the complementary application, the complement channels may drive the external devices like power switches. The dead-time generator inserts a low level interval between complementary outputs PWMx_CH0 and PWMx_CH1 as shown in Figure 6.17-14. User sets DTEN (TIMERx_PWMDTCTL[16]) bit to enable dead-time control function, DTCNT (TIMERx_PWMDTCTL[11:0]) and DTCKSEL (TIMERx_PWMDTCTL[24]) to control dead-time interval. The dead-time interval can be calculated from the following formula:

Dead-time interval = (DTCNT + 1) * TMRx_PWMCLK period, if DTCKSEL is 0

Dead-time interval = (DTCNT + 1) * TMRx_PWMCLK * (CLKPSC + 1) period, if DTCKSEL is 1

will occurred when TM_BRAKEx (x=0~3) pin status from high to low.

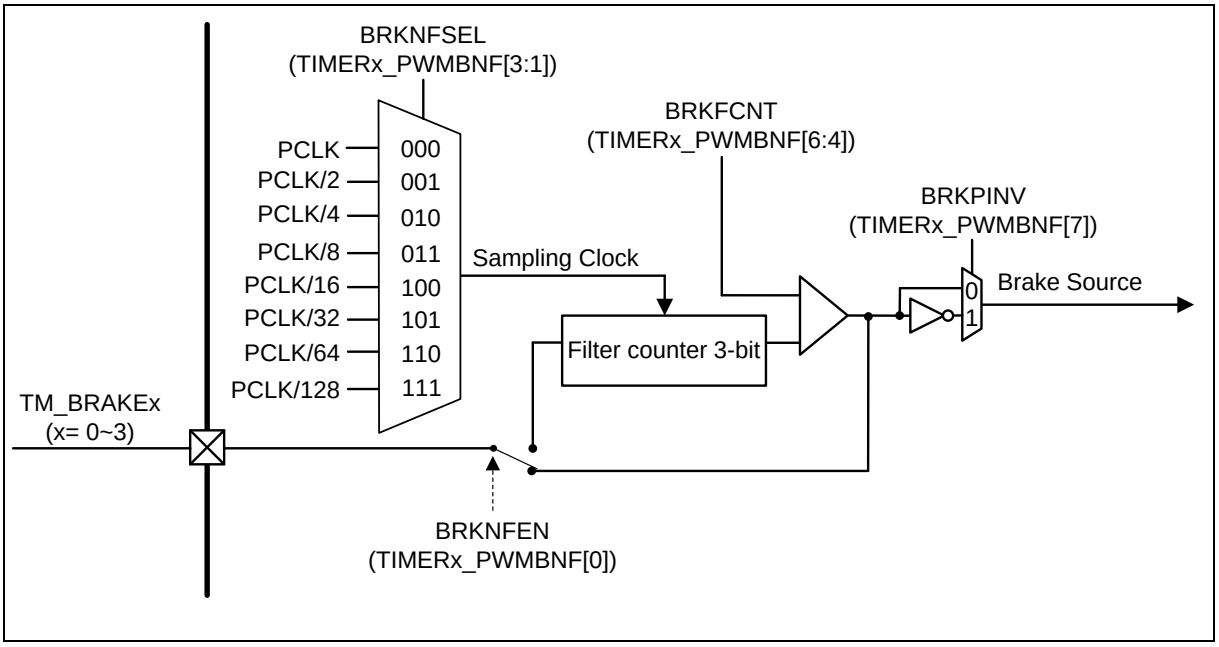


Figure 6.17-16 Brake Pin Noise Filter Block Diagram

User can set BRKAEVEN (TIMERx_PWMBRKCTL[17:16]) for PWMx_CH0 output state and BRKAODD (TIMERx_PWMBRKCTL[19:18]) for PWMx_CH1 output state when PWM brake event happened. There are two brake detector sources, edge detect brake source and level detect brake source when brake event happened. Figure 6.17-17 shows the brake event block diagram for PWMx_CH0 and PWMx_CH1.

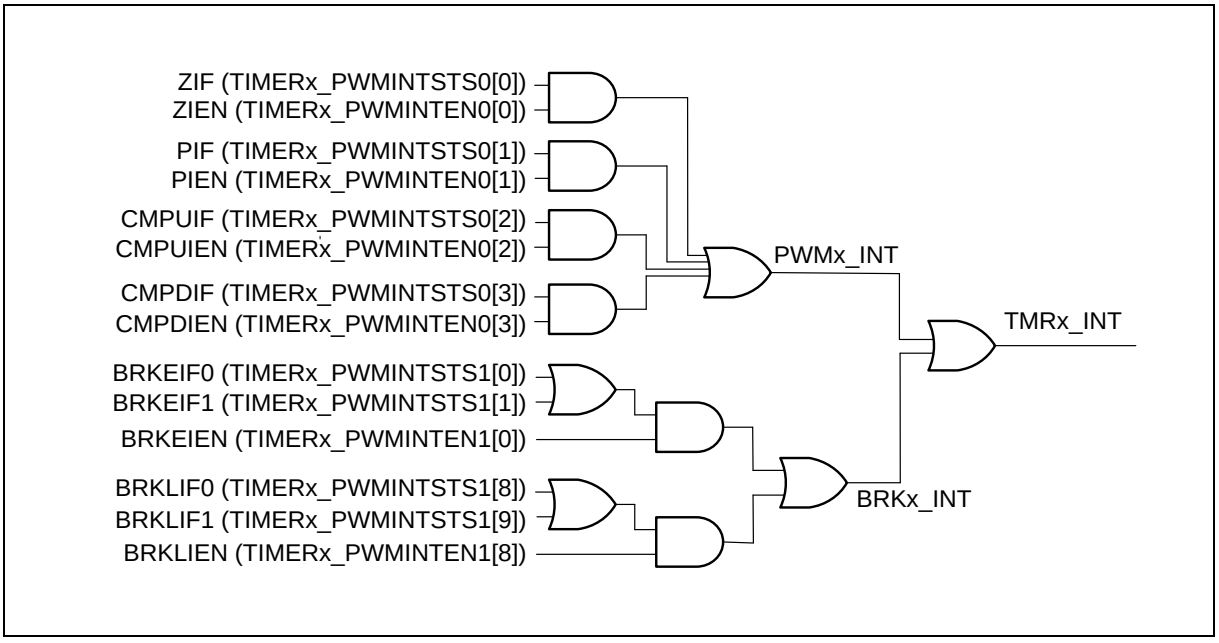


Figure 6.17-23 PWM Interrupt Architecture Diagram

6.17.3.20 PWM Trigger ADC Generator

The PWM counter event can be one of the ADC conversion trigger source. User sets TRGSEL (TIMERx_PWMADCTS[3:0]) to select which PWM counter event can trigger ADC conversion after TRGEN (TIMERx_PWMADCTS [7]) is enabled.

There are five PWM counter events can be selected as the trigger source to start ADC conversion which shown in Figure 6.17-24.

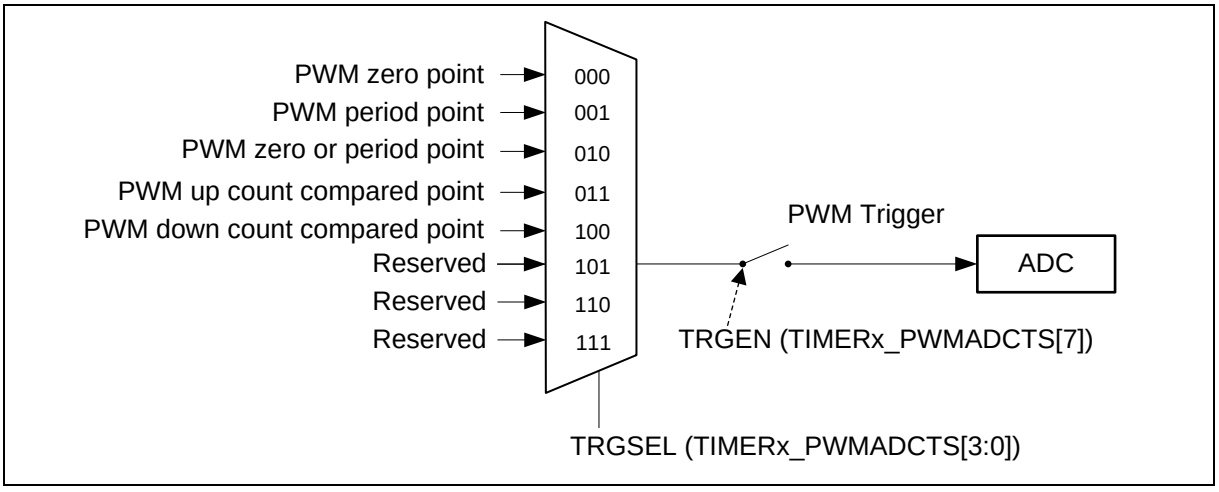


Figure 6.17-24 PWM Trigger ADC Block Diagram

6.24 Window Watchdog Timer (WWDT)

6.24.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset while WWDT counter is not reload within a specified window period when application program run to uncontrollable status by any unpredictable condition.

6.24.2 Features

- Supports 6-bit down counter value CNTDAT (WWDT_CNT[5:0]) and maximum 6-bit compare value CMPDAT (WWDT_CTL[21:16]) to adjust the WWDT compare time-out window period flexible
- Supports PSCSEL (WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode
- WWDT counter only can be reloaded within in valid window period to prevent system reset

6.24.3 Clock Control

The WWDT clock control and block diagram are shown as follows.

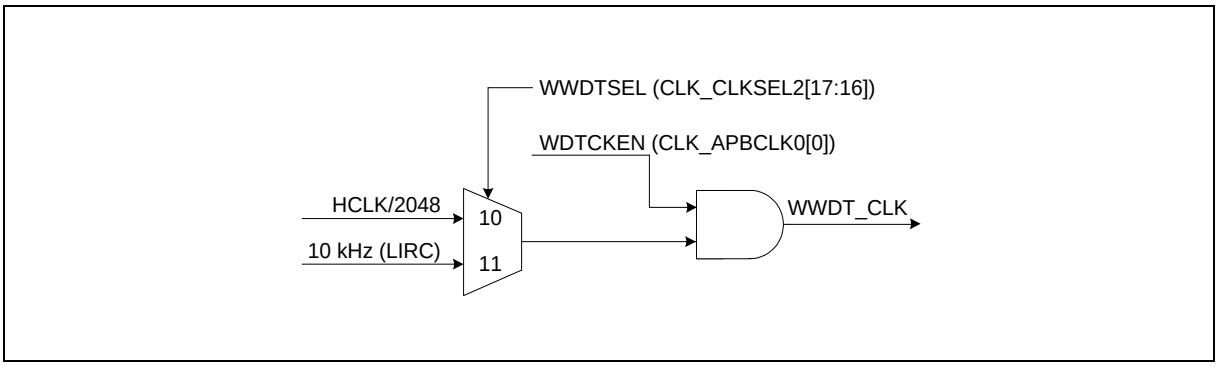


Figure 6.24-1 WWDT Clock Control

8.2 DC Electrical Characteristics

(V_{DD}-V_{SS} = 2.5 ~ 5.5V, TA = 25°C, F_{OSC} = 72 MHz unless otherwise specified.)

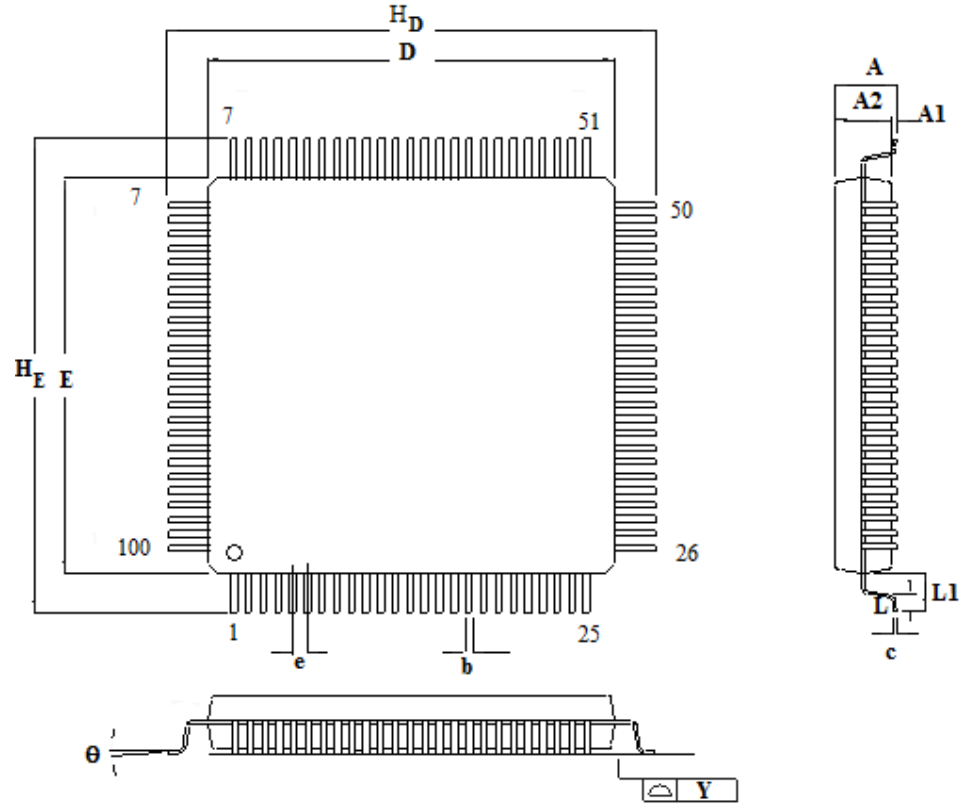
PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS					
		MIN.	TYP.	MAX.	UNIT						
Operation Voltage	V_{DD} - V_{SS}	2.5	-	5.5	V	V_{DD} = 2.5 ~ 5.5V up to 72 MHz					
Power supply for PE.8 ~ PE.13	V_{DDIO} - V_{SS}	1.8	-	5.5	V						
Power supply for PF.0, PF.1 and PF.2	V_{BAT} - V_{SS}	2.5	-	5.5	V						
Power Ground	V_{SS} - AV_{SS}	-0.05	-	+0.05	V						
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	MCU operating in Run, Idle or Power-down mode					
	C_{LDO}	1			uF	Connect to LDO_CAP pin					
Band-gap Voltage	V_{BG}	-	1.21	-	V						
Allowed voltage difference for V_{DD} and AV_{DD}	V_{DD} - AV_{DD}	-0.3	-	+0.3	V						
Operating Current Normal Run Mode HCLK =72 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD1}	-	57	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	12 MHz	X	X	V	V
	I_{DD2}	-	22	-	mA	5.5 V	12 MHz	X	X	V	X
	I_{DD3}	-	57	-	mA	3.3 V	12 MHz	X	X	V	V
	I_{DD4}	-	22	-	mA	3.3 V	12 MHz	X	X	V	X
Operating Current Normal Run Mode HCLK =72 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD5}	-	55	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	X	X	V	V	V
	I_{DD6}	-	21	-	mA	5.5 V	X	X	V	V	X
	I_{DD7}	-	55	-	mA	3.3 V	X	X	V	V	V
	I_{DD8}	-	21	-	mA	3.3 V	X	X	V	V	X
Operating Current Normal Run Mode HCLK =48 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD9}	-	33	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	12 MHz	X	X	V	V
	I_{DD10}	-	14	-	mA	5.5 V	12 MHz	X	X	V	X
	I_{DD11}	-	33	-	mA	3.3 V	12 MHz	X	X	V	V
	I_{DD12}	-	14	-	mA	3.3 V	12 MHz	X	X	V	X

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Sink Current (Quasi-bidirectional, Open-Drain and Push-pull Mode for V_{DDIO} domain)	I_{SK4}	-	-2.2	-	mA	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$ $V_{DDIO} = 1.8V$, $V_S = 1.6V$
Higher GPIO Rising Rate	$HIORR_1$	-	2.46	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, without capacitor
	$HIORR_2$		3.24		ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, with 10pF capacitor
	$HIORR_3$	-	3.12	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.0V$, without capacitor
	$HIORR_4$	-	4.56	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.0V$, with 10pF capacitor
	$HIORR_5$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, without capacitor (for VDDIO domain)
	$HIORR_6$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, with 10pF capacitor (for VDDIO domain)
Basic GPIO Rising Rate	$BIORR_1$	-	3.24	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, without capacitor
	$BIORR_2$	-	4.15	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, with 10pF capacitor
	$BIORR_3$	-	4.75	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.0V$, without capacitor
	$BIORR_4$	-	6.43	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.0V$, with 10pF capacitor
	$BIORR_5$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, without capacitor (for VDDIO domain)
	$BIORR_6$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, with 10pF capacitor (for VDDIO domain)
Higher GPIO Falling Rate	$HIOFR_1$	-	2.10	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, without capacitor

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	$HIOFR_2$	-	2.83	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, with 10pF capacitor
	$HIOFR_3$	-	3.12	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.3V$, without capacitor
	$HIOFR_4$	-	4.19	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.3V$, with 10pF capacitor
	$HIOFR_5$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, without capacitor (for V_{DDIO} domain)
	$HIOFR_6$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, with 10pF capacitor (for V_{DDIO} domain)
Basic GPIO Falling Rate	$BIOFR_1$	-	3.42	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, without capacitor
	$BIOFR_2$	-	4.40	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 5.5V$, with 10pF capacitor
	$BIOFR_3$	-	6.14	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.3V$, without capacitor
	$BIOFR_4$	-	7.87	-	ns	$V_{DD} = V_{BAT} = V_{DDIO} = 3.3V$, with 10pF capacitor
	$BIOFR_5$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, without capacitor (for V_{DDIO} domain)
	$BIOFR_6$	-	TBD	-	ns	$V_{DD} = V_{BAT} = 2.5 \sim 5.5V$, $V_{DDIO} = 1.8V$, with 10pF capacitor (for V_{DDIO} domain)

9 PACKAGE DIMENSIONS

9.1 LQFP 100L (14x14x1.4 mm footprint 2.0 mm)



Controlling Dimension : Millimeters

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	-
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.10	0.15	0.20
D	13.90	14.00	14.10
E	13.90	14.00	14.10
e	-	0.50	-
HD	15.80	16.00	16.20
HE	15.80	16.00	16.20
L	0.45	0.60	0.75
L1	-	1	-
y	-	-	0.10
θ	0°	-	7°