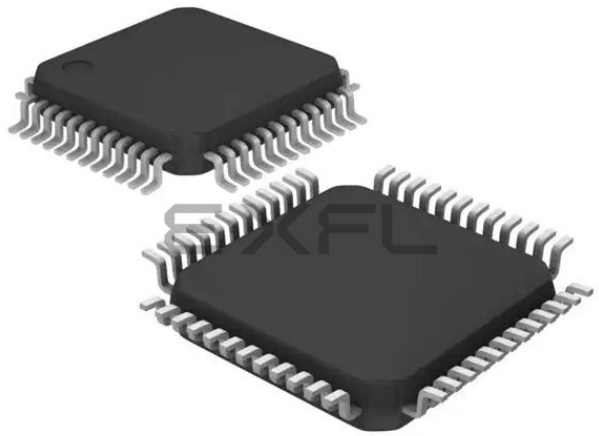

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVR, I²S, PWM
Number of I/O	41
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m0564lg4ae

- Built-in 22.1184 MHz high speed RC oscillator for system operation (Frequency variation < 2% at -40°C ~ +105°C)
- Built-in 48 MHz internal high speed RC oscillator (Frequency variation < 2% at -40°C ~ +105°C)
- Built-in 10 kHz low speed RC oscillator for Watchdog Timer and Wake-up operation
- Built-in 4~24 MHz high speed crystal oscillator for precise timing operation
- Built-in 32.768 kHz low speed crystal oscillator for Real Time Clock
- Supports PLL up to 144 MHz for high resolution PWM operation
- Supports dynamically calibrating the HIRC48 to 48 MHz ±0.25% by external 32.768K crystal oscillator (LXT)
- Supports dynamically calibrating the HIRC to 22.1184Mhz by external 32.768K crystal oscillator (LXT)
- Supports clock on-the-fly switch
- Supports clock failure detection for system clock
- Supports auto clock switch once clock failure detected
- Supports exception (NMI) generated once a clock failure detected
- Supports divided clock output

● GPIO

- Four I/O modes
- TTL/Schmitt trigger input selectable
- I/O pin configured as interrupt source with edge/level trigger setting
- Supports high driver and high sink current I/O (up to 20 mA at 5V)
- Supports software selectable slew rate control
- Supports up to 81/49/35 GPIOs for LQFP100/64/48 respectively

● Timer/PWM

- Supports 4 sets of Timers/PWM

Timer Mode	PWM Mode
TM_CNT_OUT	PWM_CH0
TM_EXT	PWM_CH1 (Complementary)

- Timer Mode
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function to count the event from external pin
  - Supports input capture function to capture or reset counter value
  - Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
  - Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, EADC and PDMA function
  - Supports Inter-Timer trigger mode
- PWM Mode
  - Supports maximum clock frequency up to 50MHz
  - Supports independent mode for 4 sets of independent PWM output channel
  - Supports complementary mode for 4 sets of complementary paired PWM output channel with 12-bit Dead-time generator
  - Supports 12-bit pre-scalar from 1 to 4096

- Supports Auto-Baud Rate measurement and baud rate compensation function
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports LIN function mode
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detection function for receiver
- Supports RS-485 mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function

● Supports PDMA transferSmart Card Host (SC)

- Supports up to two Smart Card Hosts

SC Mode	UART Mode
SC_DATA	Rx
SC_CLK	Tx
SC_CD	-
SC_PWR	-
SC_RST	-

- SC Mode
  - Supports up to two ISO-7816-3 ports
  - Compliant to ISO-7816-3 T=0, T=1
  - Separate receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 266 ETU)
  - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detecting the card is removal
- UART Mode
  - Full duplex, asynchronous communications
  - Supports receiving / transmitting 4-bytes FIFO
  - Supports programmable baud rate generator for each channel
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1 or 2 stop bit generation

● SPI/I^2S

- Supports up to two SPI/I^2S controllers

channel
- Supports digital comparator to monitor conversion result and user can select whether to generate an interrupt when conversion result matches the compare register setting
- An A/D conversion can be triggered by:
  - Software enable
  - External pin (STADC)
  - Timer 0~3 overflow pulse trigger
  - PWM triggers with optional start delay period
- Supports 4 internal channels for
  - Operational amplifier output
  - Band-gap VBG input
  - Temperature sensor input
  - VBAT voltage measure
- Supports internal reference voltage: 2.048V, 2.560V, 3.072V and 4.096V
- Supports PDMA transfer

- Analog Comparator
  - Supports up to 2 rail-to-rail analog comparators
  - Supports 4 multiplexed I/O pins at positive node.
  - Supports I/O pin and internal voltages at negative node
  - Support selectable internal voltage reference from:
    - Band-gap V_{BG}
    - Voltage divider source from AV_{DD} and internal reference voltage.
  - Supports programmable hysteresis
  - Supports programmable speed and power consumption
  - Interrupts generated when compare results change, interrupt event condition is programmable.
  - Supports power-down wake-up
  - Supports triggers for break events and cycle-by-cycle control for PWM
- Cyclic Redundancy Calculation Unit
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - Programmable initial value
  - Supports programmable order reverse setting for input data and CRC checksum
  - Supports programmable 1's complement setting for input data and CRC checksum.
  - Supports 8/16/32-bit of data width
  - Interrupt generated once checksum error occurs
- User Configurable VDD1=1.8~5.5V IO Interface
  - Supports UART0, SPI0 and I2C0
- Supports 96-bit Unique ID (UID)
- Supports 128-bit Unique Customer ID (UCID)
- One built-in temperature sensor with 1℃ resolution
- Brown-out detector
  - With 8 levels: 4.3 V/ 3.7V/ 2.7V/ 2.2V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 2.0 V
- Power consumption
  - Chip power down current < 10 uA with RAM data retention.
  - V_{BAT} power domain operating current <1.5 uA
- Operating Temperature: -40℃~105℃

4.2 Pin Configuration

4.2.1 NuMicro® M0564 Base Series LQFP48 Pin Diagram

Corresponding Part Number: M0564LE4AE, M0564LG4AE

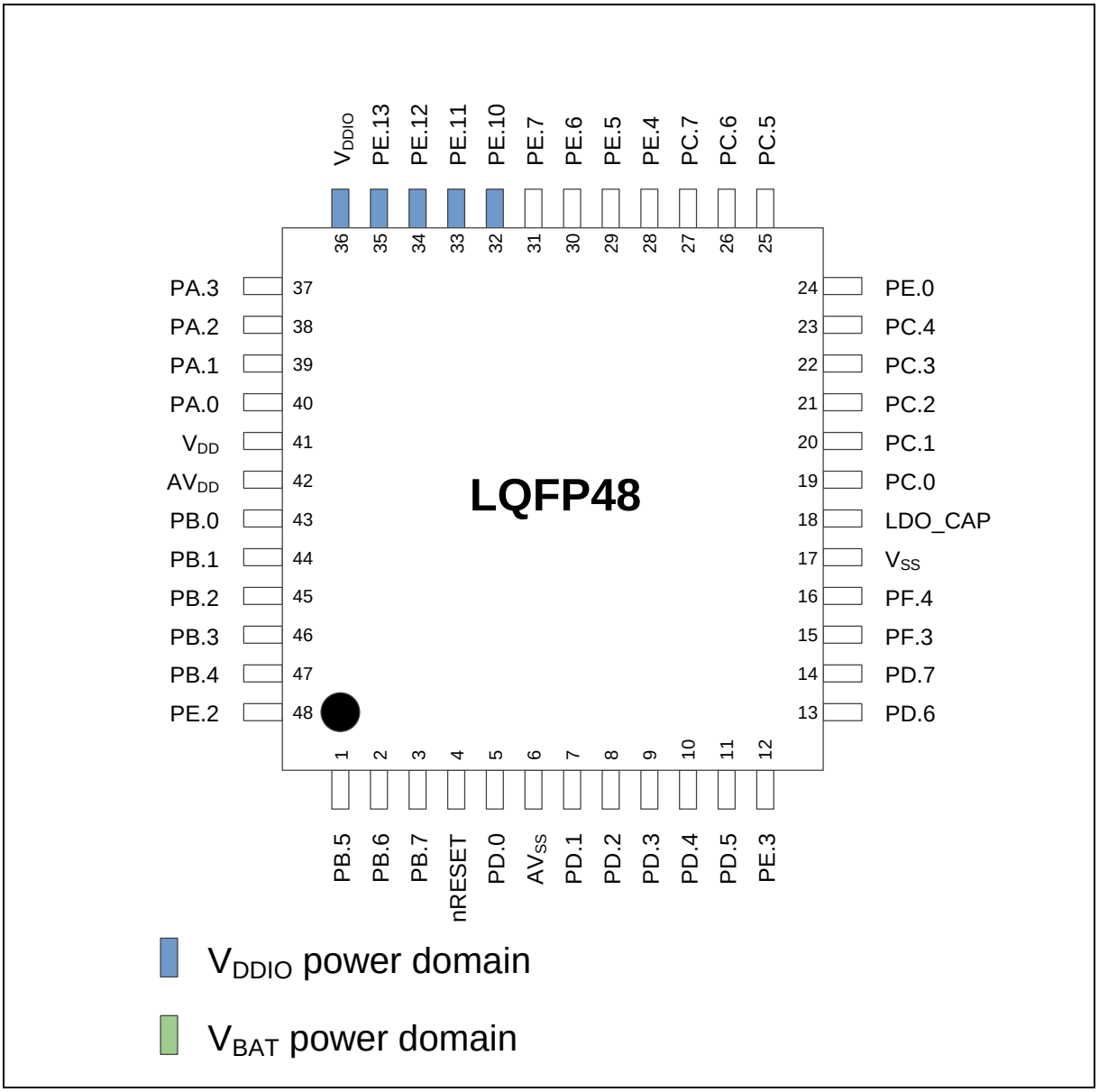

Figure 4.2-1 NuMicro® M0564 Base Series LQFP 48-pin Diagram

4.3 Pin Description

4.3.1 M0564 Base Series Pin Description

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)

PA.0 MFP0 means SYS_GP0_MFPL[3:0]=0x0.

PA.9 MFP5 means SYS_GP0_MFPH[7:4]=0x5.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
		1	PB.13	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH10	A	MFP1	ADC0 channel 10 analog input.
		2	PB.14	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH11	A	MFP1	ADC0 channel 11 analog input.
	1	3	PB.15	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH12	A	MFP1	ADC0 channel 12 analog input.
			ACMP0_P3	A	MFP5	Analog comparator 0 positive input 3 pin.
			EBI_nCS1	O	MFP7	EBI chip select 1 output pin.
1	2	4	PB.5	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH13	A	MFP1	ADC0 channel 13 analog input.
			SPI0_MOSI	I/O	MFP2	SPI0 MOSI (Master Out, Slave In) pin.
			SPI1_MOSI	I/O	MFP3	SPI1 MOSI (Master Out, Slave In) pin.
			ACMP0_P2	A	MFP5	Analog comparator 0 positive input 2 pin.
			SC1_RST	O	MFP6	Smart Card 1 reset pin.
			EBI_AD6	I/O	MFP7	EBI address/data bus bit 6.
2	3	5	PB.6	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH14	A	MFP1	ADC0 channel 14 analog input.
			SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.
			SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin.
			ACMP0_P1	A	MFP5	Analog comparator 0 positive input 1 pin.
			SC1_PWR	O	MFP6	Smart Card 1 power pin.
			EBI_AD5	I/O	MFP7	EBI address/data bus bit 5.
3	4	6	PB.7	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH15	A	MFP1	ADC0 channel 15 analog input.
			SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
			SPI1_CLK	I/O	MFP3	SPI1 serial clock pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			TM3	I/O	MFP6	Timer3 event counter input/toggle output pin.
			EBI_ALE	O	MFP7	EBI address latch enable output pin.
7	10	15	PD.1	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH19	A	MFP1	ADC0 channel 19 analog input.
			PWM0_SYNC_IN	I	MFP2	PWM0 counter synchronous trigger input pin.
			UART0_TXD	O	MFP3	UART0 data transmitter output pin.
			USCI2_CLK	I/O	MFP4	USCI2 clock pin.
			ACMP1_P2	A	MFP5	Analog comparator 1 positive input 2 pin.
			TM0	I/O	MFP6	Timer0 event counter input/toggle output pin.
			EBI_nRD	O	MFP7	EBI read enable output pin.
8	11	16	PD.2	I/O	MFP0	General purpose digital I/O pin.
			ADC0_ST	I	MFP1	ADC0 external trigger input pin.
			TM0_EXT	I/O	MFP3	Timer0 external capture input/toggle output pin.
			USCI2_DAT0	I/O	MFP4	USCI2 data 0 pin.
			ACMP1_P1	A	MFP5	Analog comparator 1 positive input 1 pin.
			PWM0_BRAKE0	I	MFP6	PWM0 Brake 0 input pin.
			EBI_nWR	O	MFP7	EBI write enable output pin.
			INT0	I	MFP8	External interrupt 0 input pin.
9	12	17	PD.3	I/O	MFP0	General purpose digital I/O pin.
			TM2	I/O	MFP1	Timer2 event counter input/toggle output pin.
			SPI0_I2SMCLK	I/O	MFP2	SPI0 I2S master clock output pin
			TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin.
			USCI2_DAT1	I/O	MFP4	USCI2 data 1 pin.
			ACMP1_P0	A	MFP5	Analog comparator 1 positive input 0 pin.
			PWM0_BRAKE1	I	MFP6	PWM0 Brake 1 input pin.
			EBI_MCLK	O	MFP7	EBI external clock output pin.
			INT1	I	MFP8	External interrupt 1 input pin.
10		18	PD.4	I/O	MFP0	General purpose digital I/O pin.
			SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
			I2C0_SDA	I/O	MFP3	I2C0 data input/output pin.
			UART2_nRTS	O	MFP4	UART2 request to Send output pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PE.1	MFP6	I/O	
	PWM0_CH2	PC.2	MFP6	I/O	PWM0 channel 2 output/capture input.
		PB.8	MFP6	I/O	
		PE.2	MFP6	I/O	
	PWM0_CH3	PE.3	MFP6	I/O	PWM0 channel 3 output/capture input.
		PC.3	MFP6	I/O	
	PWM0_CH4	PC.4	MFP6	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH5	PD.6	MFP6	I/O	PWM0 channel 5 output/capture input.
		PD.7	MFP6	I/O	
		PC.5	MFP6	I/O	
	PWM0_SYNC_IN	PD.1	MFP2	I	PWM0 counter synchronous trigger input pin.
		PD.7	MFP3	I	
	PWM0_SYNC_OUT	PB.1	MFP6	O	PWM0 counter synchronous trigger output pin.
PWM1	PWM1_BRAKE0	PF.1	MFP6	I	PWM1 Brake 0 input pin.
		PE.4	MFP6	I	
	PWM1_BRAKE1	PF.2	MFP6	I	PWM1 Brake 1 input pin.
		PE.5	MFP6	I	
	PWM1_CH0	PD.12	MFP6	I/O	PWM1 channel 0 output/capture input.
		PC.9	MFP6	I/O	
		PC.6	MFP6	I/O	
		PC.15	MFP6	I/O	
	PWM1_CH1	PD.13	MFP6	I/O	PWM1 channel 1 output/capture input.
		PC.10	MFP6	I/O	
		PC.7	MFP6	I/O	
		PB.12	MFP6	I/O	
	PWM1_CH2	PD.14	MFP6	I/O	PWM1 channel 2 output/capture input.
		PC.11	MFP6	I/O	
		PA.3	MFP6	I/O	
	PWM1_CH3	PD.15	MFP6	I/O	PWM1 channel 3 output/capture input.
		PC.12	MFP6	I/O	
		PA.2	MFP6	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PE.11	MFP8	I/O	
TM2	TM2	PD.8	MFP6	I/O	Timer2 event counter input/toggle output pin.
		PD.3	MFP1	I/O	
		PD.10	MFP4	I/O	
		PA.14	MFP6	I/O	
		PB.0	MFP4	I/O	
	TM2_EXT	PE.0	MFP4	I/O	Timer2 external capture input/toggle output pin.
		PA.5	MFP3	I/O	
		PE.12	MFP8	I/O	
TM3	TM3	PD.9	MFP6	I/O	Timer3 event counter input/toggle output pin.
		PD.11	MFP4	I/O	
		PA.15	MFP6	I/O	
		PB.1	MFP4	I/O	
	TM3_EXT	PF.5	MFP3	I/O	Timer3 external capture input/toggle output pin.
		PA.4	MFP3	I/O	
		PE.1	MFP3	I/O	
		PE.13	MFP8	I/O	
TM	TM_BRAKE0	PA.8	MFP6	I	Timer Brake 0 input pin.
		PF.5	MFP6	I	
		PB.2	MFP6	I	
	TM_BRAKE1	PA.9	MFP6	I	Timer Brake 1 input pin.
		PA.7	MFP6	I	
		PB.3	MFP6	I	
	TM_BRAKE2	PA.6	MFP6	I	Timer Brake 2 input pin.
		PA.12	MFP6	I	
		PB.8	MFP5	I	
	TM_BRAKE3	PA.5	MFP6	I	Timer Brake 3 input pin.
		PA.13	MFP6	I	
		PE.2	MFP5	I	
UART0	UART0_RXD	PD.0	MFP3	I	UART0 data receiver input pin.
		PD.9	MFP3	I	
		PD.6	MFP3	I	

Group	Pin Name	GPIO	MFP	Type	Description
		PB.8	MFP4	O	
		PE.2	MFP4	O	
UART2	UART2_RXD	PE.3	MFP4	I	UART2 data receiver input pin.
		PC.3	MFP3	I	
		PA.12	MFP3	I	
		PB.0	MFP3	I	
	UART2_TXD	PD.6	MFP4	O	UART2 data transmitter output pin.
		PC.2	MFP3	O	
		PA.13	MFP3	O	
		PB.1	MFP3	O	
	UART2_nCTS	PD.5	MFP4	I	UART2 clear to Send input pin.
		PC.0	MFP3	I	
		PA.14	MFP3	I	
	UART2_nRTS	PD.4	MFP4	O	UART2 request to Send output pin.
		PC.1	MFP3	O	
		PA.15	MFP3	O	
USCI0	USCI0_CLK	PC.4	MFP5	I/O	USCI0 clock pin.
		PE.5	MFP4	I/O	
		PB.9	MFP8	I/O	
	USCI0_CTL0	PC.3	MFP5	I/O	USCI0 control 0 pin.
		PE.4	MFP4	I/O	
		PB.8	MFP8	I/O	
		PE.2	MFP8	I/O	
	USCI0_CTL1	PC.2	MFP4	I/O	USCI0 control 1 pin.
		PC.7	MFP4	I/O	
		PB.4	MFP8	I/O	
	USCI0_DAT0	PC.0	MFP4	I/O	USCI0 data 0 pin.
		PC.5	MFP4	I/O	
		PB.2	MFP8	I/O	
	USCI0_DAT1	PC.1	MFP4	I/O	USCI0 data 1 pin.
		PC.6	MFP4	I/O	
		PB.3	MFP8	I/O	

6.2 System Manager

6.2.1 Overview

The system manager provides the functions of system control, power modes, wake-up sources, reset sources, system memory map, product ID and multi-function pin control. The following sections describe the functions for

- System Reset
- Power Modes and Wake-up Sources
- System Power Distribution
- SRAM Memory organization
- System Control Register for Part Number ID, Chip Reset and Multi-function Pin Control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sourcces are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M0 core Only by writing 1 to CPURST (SYS_IPRST0[1])

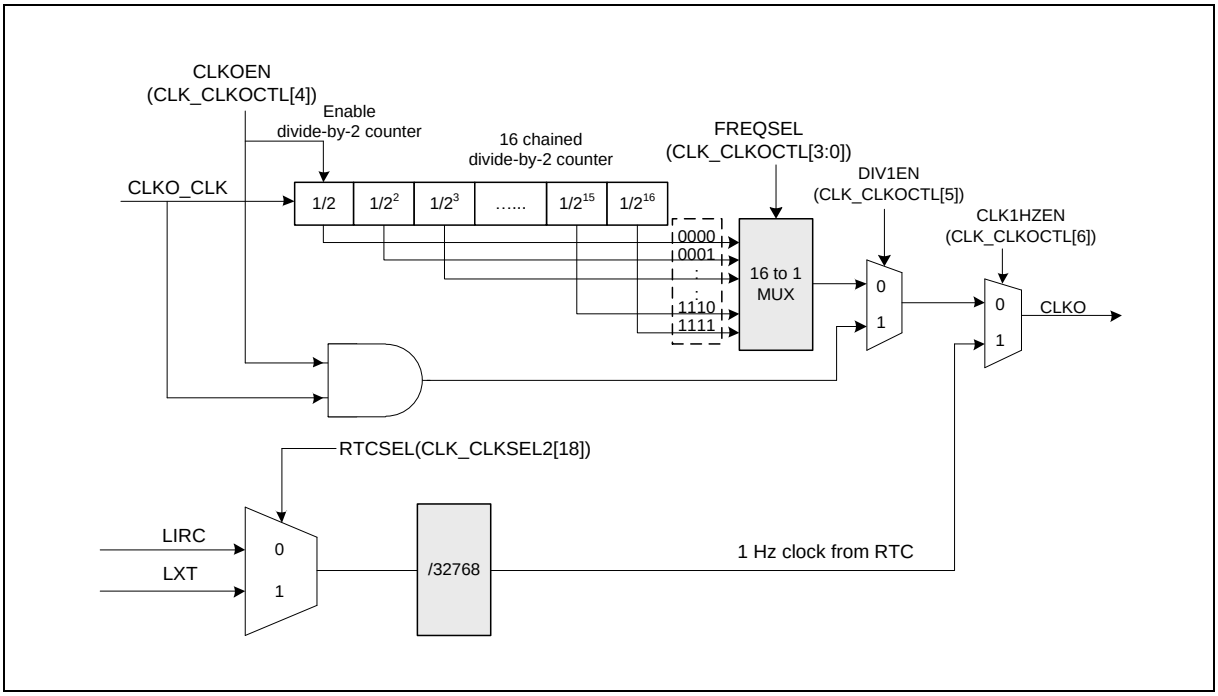

Figure 6.3-7 Clock Output Block Diagram

6.9 General Purpose I/O (GPIO)

6.9.1 Overview

The M0564 series has up to 86 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 86 pins are arranged in 6 ports named as PA, PB, PC, PD, PE and PF. PA, PB, PC, PD has 16 pins on port. PE has 14 pins on port. PF has 8 pins on port. Each of the 86 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOIN (CONFIG0[10]). Each I/O pin has a very weakly individual pull-up resistor which is about 110 kΩ ~ 300 kΩ for V_{DD} is from 5.0 V to 2.5 V.

6.9.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOIN = 0, all GPIO pins in input tri-state mode after chip reset
  - CIOIN = 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the wake-up function

6.10 Hardware Divider (HDIV)

6.10.1 Overview

The hardware divider (HDIV) is useful to the high performance application. The hardware divider is a signed, integer divider with both quotient and remainder outputs.

6.10.2 Features

- Signed (two's complement) integer calculation
- 32-bit dividend with 16-bit divisor calculation capacity
- 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
- Divided by zero warning flag
- 6 HCLK clocks taken for one cycle calculation
- Write divisor to trigger calculation
- Waiting for calculation ready automatically when reading quotient and remainder

6.10.3 Blcok Diagram

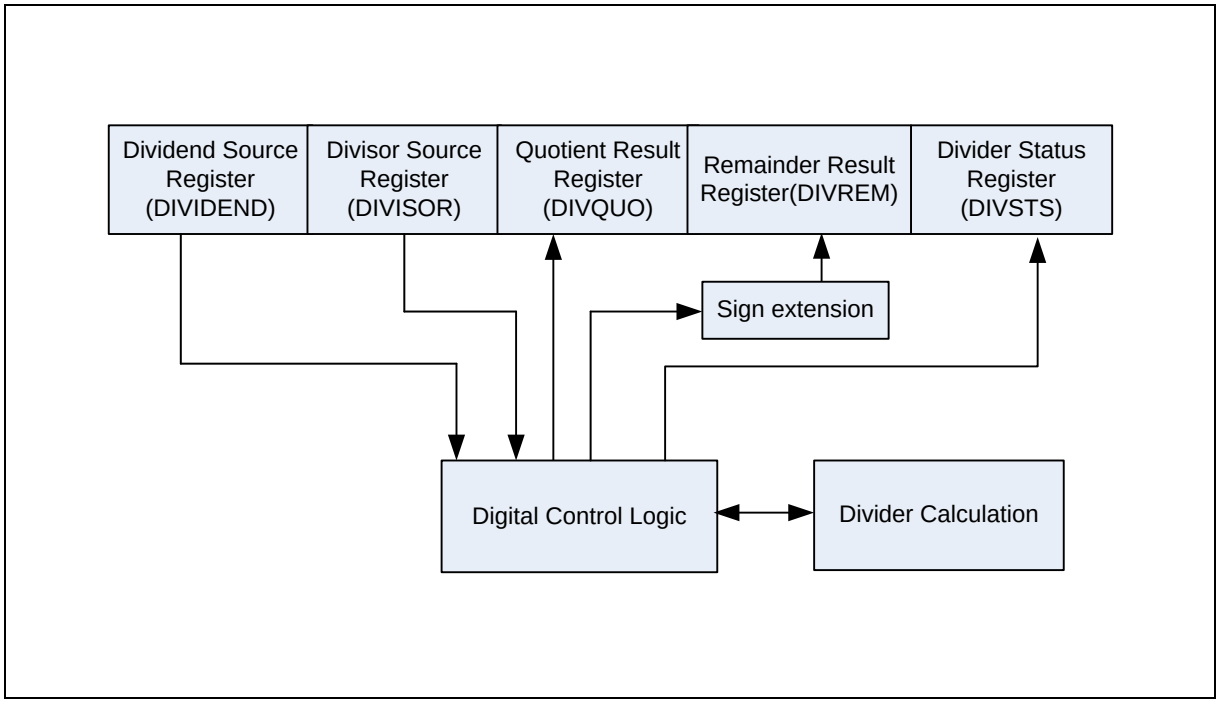

Figure 6.10-1 Hardware Divider Block Diagram

6.13 PWM Generator and Capture Timer (PWM)

6.13.1 Overview

The M0564 provides two PWM generator: PWM0 and PWM1. Each PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses comparator compared with counter to generate events. These events use to generate PWM pulse, interrupt and trigger signal for ADC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various PWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for ADC. For PWM output control unit, it supports polarity output, independent pin mask and brake functions.

The PWM generator also supports input capture function. It supports latch PWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.13.2 Features

6.13.2.1 PWM function features

- Supports maximum clock frequency up to144MHz
- Supports up to two PWM modules, each module provides 6 output channels.
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channels:
  - Dead-time insertion with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution PWM counter
  - Up, down and up-down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each PWM output pin
- Supports brake function
  - Brake source from pin, analog comparator, ADC result monitor and system safety events (clock failed, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared

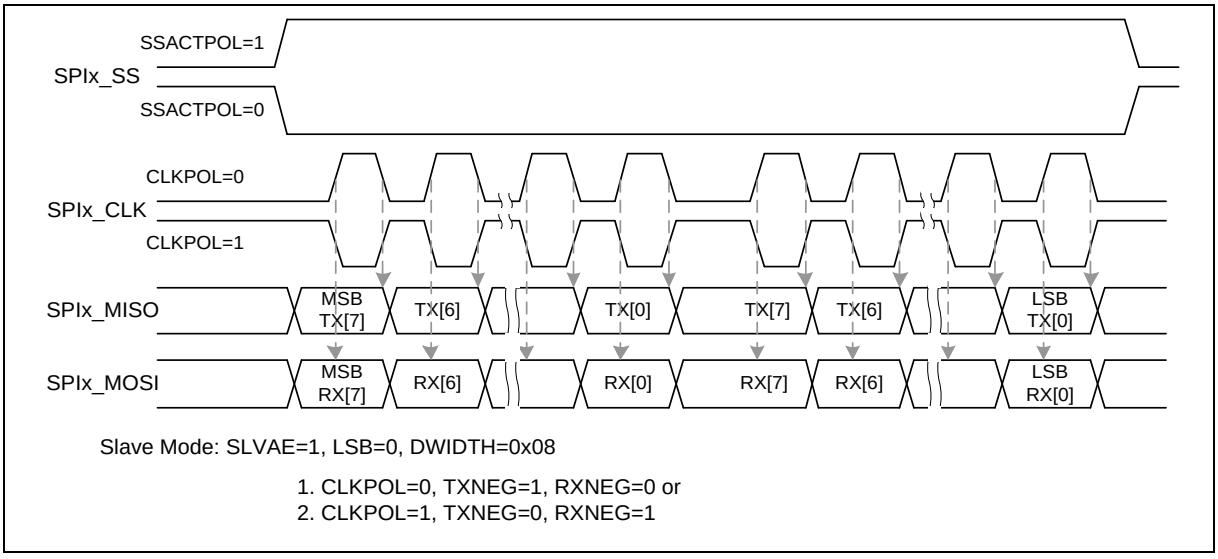

Figure 6.16-3 SPI Timing in Slave Mode

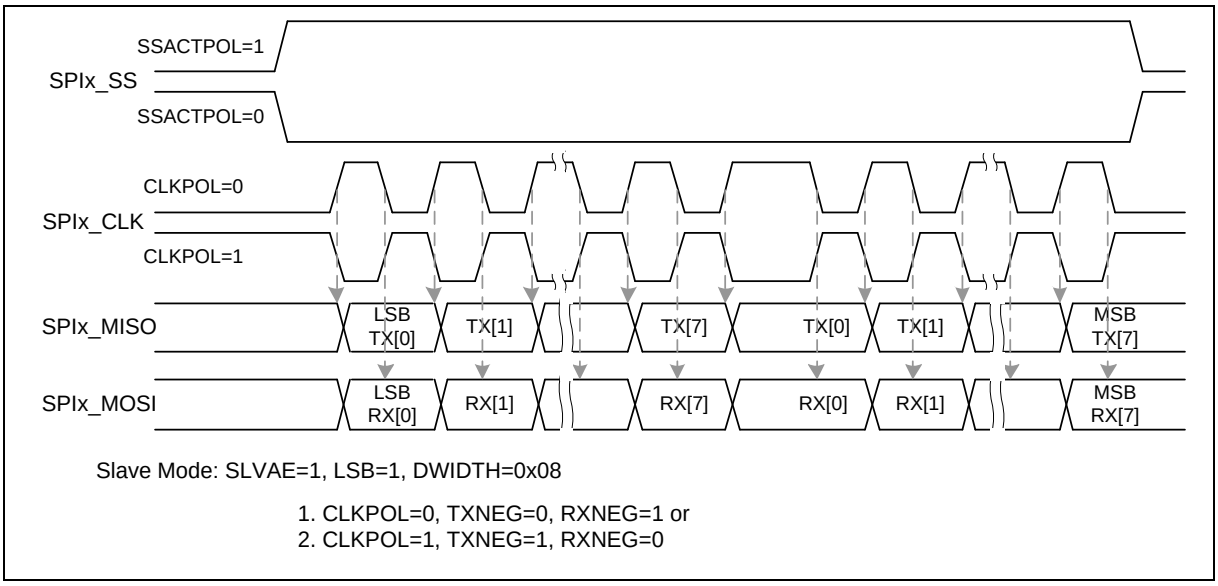

Figure 6.16-4 SPI Timing in Slave Mode (Alternate Phase of SPIx_CLK)

6.17.3 PWM Functional Description

6.17.3.1 PWM Prescale

The PWM prescale is used to divide clock source, and the clock of PWM counter is divided by (CLKPSC+ 1). The prescale is set by CLKPSC (TIMERx_PWMCLKPSC[11:0]). Figure 6.17-1 shows an example of PWM prescale waveform in up count type.

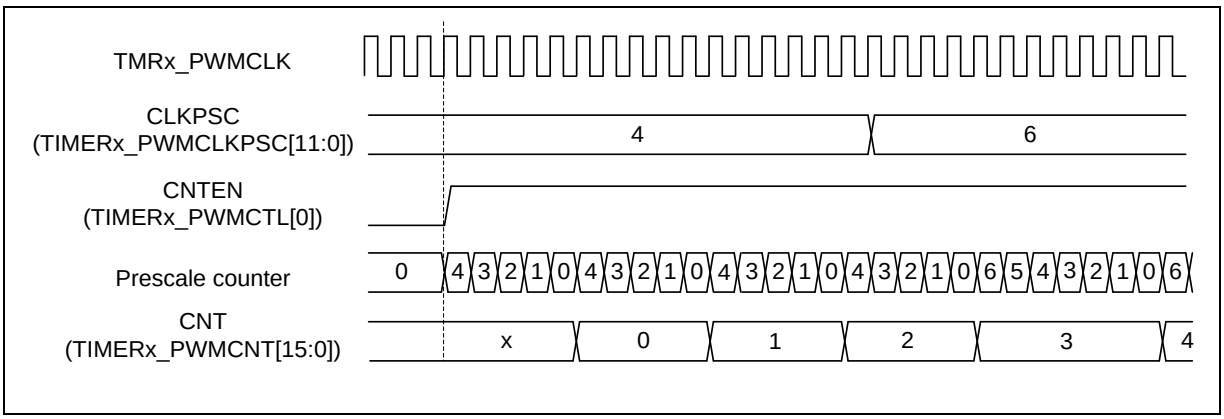

Figure 6.17-1 PWM Prescale Waveform in Up Count Type

6.17.3.2 PWM Counter

PWM supports three counter types operation: up count, down count and up-down count types.

6.17.3.3 Up Count Type

When the PWM counter is set to up count type, CNTTYPE (TIMERx_PWMCTL[2:1]) is 0x0, it starts up-counting from zero to PERIOD (TIMERx_PWMPERIOD[15:0]). The current counter value can be read from the CNT (TIMERx_PWMCNT[15:0]). PWM generates a zero point event when both counter and prescale counts to 0. PWM generates a period point event when the counter counts to PERIOD and prescale counts to 0. Figure 6.17-2 shows an example of PWM up count type, where PWM period time is (PERIOD+1) * (CLKPSC+1) * TMRx_PWMCLK.

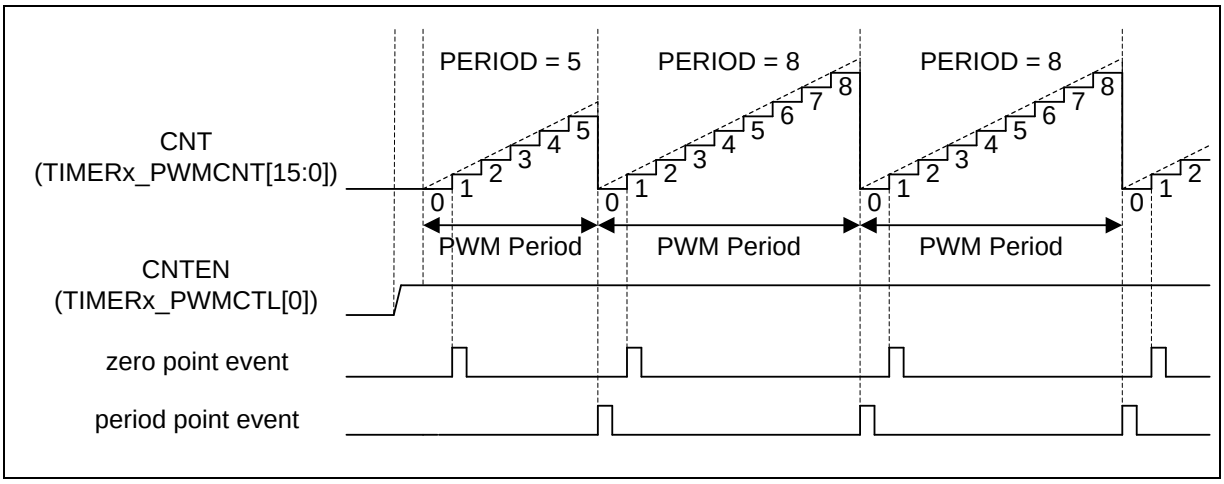

Figure 6.17-2 PWM Up Count Type

6.19 USCI – UART Mode

6.19.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter being independent, frames can start at different points in time for transmission and reception.

The UART controller also provides auto flow control. There are two conditions to wake up the system.

6.19.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-Bit Data Transfer (Support 9-Bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports Wake-up function (Data and nCTS Wakeup Only)

6.20 USCI - SPI Mode

6.20.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1.

This SPI protocol can operate as master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown below.

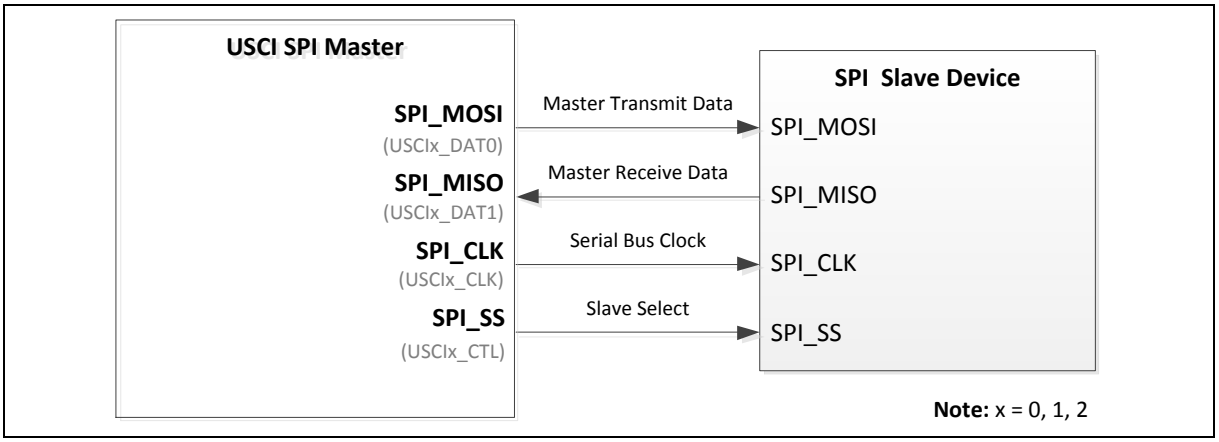

Figure 6.20-1 SPI Master Mode Application Block Diagram

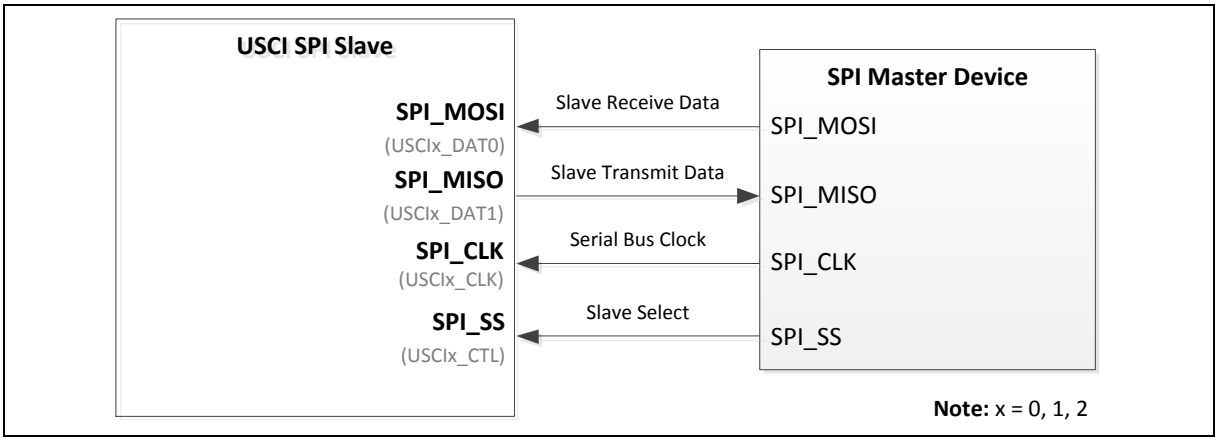

Figure 6.20-2 SPI Slave Mode Application Block Diagram

6.20.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master = f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence

t_{DH}	Data hold time	2*PCLK+6	-	-	ns
t_V	Data output valid time	-	2*PCLK+19	2*PCLK+25	ns

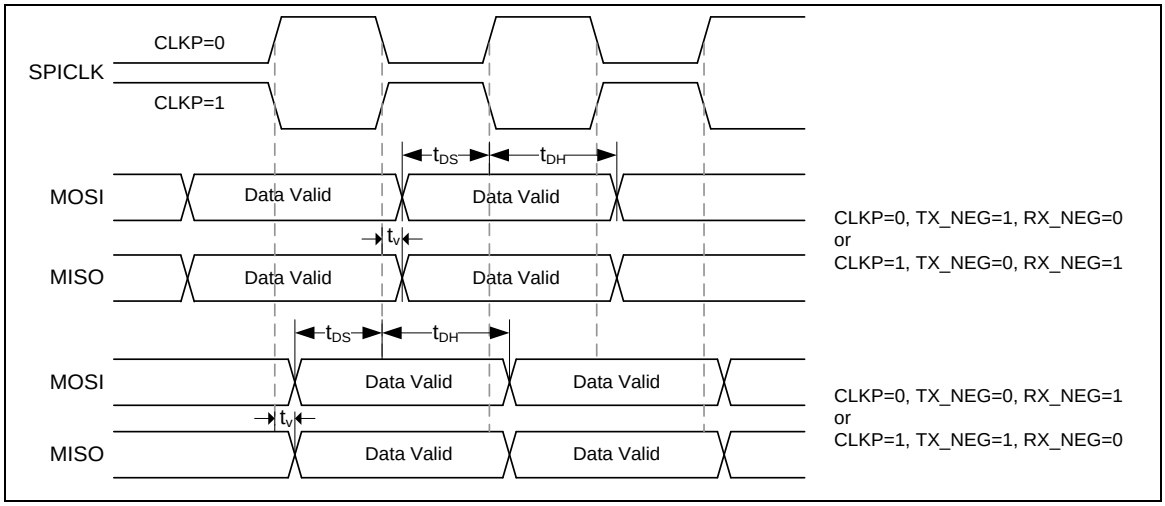

Figure 8.7-2 SPI Slave Mode Timing Diagram