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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVR, I²S, PWM
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 15x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m0564se4ae

2 FEATURES

2.1 NuMicro® M0564 Features

- Core
  - ARM® Cortex®-M0 core running up to 72 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Supports programmable mask-able interrupts
  - Serial Wire Debug supports with 2 watch-points/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5V to 5.5V
- Flash Memory
  - Supports 256/128 KB application ROM (APROM)
  - Supports 4 KB Flash for loader (LDROM)
  - Supports 2 KB Security Protection Rom (SPROM)
  - Supports 12 bytes User Configuration block to control system initiation
  - Supports Data Flash with configurable memory size
  - Supports 2 KB page erase for all embedded flash
  - Supports In-System-Programming (ISP), In-Application-Programming (IAP) update embedded flash memory
  - Supports CRC-32 checksum calculation function
  - Supports flash all one verification function
  - Hardware external read protection of whole flash memory by Security Lock Bit
  - Supports 2-wired ICP update through SWD/ICE interface
- SRAM Memory
  - 20 KB embedded SRAM
  - Supports byte-, half-word- and word-access
  - Supports PDMA mode
- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Write divisor to trigger calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
- PDMA (Peripheral DMA)
  - Supports 5 independent configurable channels for automatic data transfer between memories and peripherals
  - Supports single and burst transfer type
  - Supports Normal and Scatter-Gather Transfer modes
  - Supports two types of priorities modes: Fixed-priority and Round-robin modes
  - Supports byte-, half-word- and word-access
  - Supports incrementing mode for the source and destination address for each channel
  - Supports time-out function for channel 0 and channel 1
  - Supports software and SPI/I2S, UART, USCI, ADC, PWM and TIMER request
- Clock Control

- PWM counter match zero, period value or compared value
- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

- USCI
  - Supports up to 3 sets of USCI

USCI	UART Mode	SPI Mode	I²C Mode
USCI_CLK	-	SPI_CLK	SCL
USCI_CTL0	nCTS	SPI_SS	-
USCI_CTL1	nRTS	-	-
USCI_DAT0	Rx	SPI_MOSI	SDA
USCI_DAT1	Tx	SPI_MISO	-

  - UART Mode
    - Supports one transmit buffer and two receive buffer for data payload
    - Supports hardware auto flow control function
    - Supports programmable baud-rate generator
    - Support 9-Bit Data Transfer (Support 9-Bit RS-485)
    - Baud rate detection possible by built-in capture event of baud rate generator
    - Supports Wake-up function (Data and nCTS Wakeup Only)
  - SPI Mode
    - Supports Master or Slave mode operation (the maximum frequency -- Master = fPCLK / 2, Slave = fPCLK / 5)
    - Supports one transmit buffer and two receive buffers for data payload
    - Configurable bit length of a transfer word from 4 to 16-bit
    - Supports MSB first or LSB first transfer sequence
    - Supports Word Suspend function
    - Supports 3-wire, no slave select signal, bi-direction interface
    - Supports wake-up function by slave select signal in Slave mode
    - Supports one data channel half-duplex transfer
  - I^2C Mode
    - Full master and slave device capability
    - Supports of 7-bit addressing, as well as 10-bit addressing
    - Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
    - Supports multi-master bus
    - Supports one transmit buffer and two receive buffer for data payload
    - Supports 10-bit bus time-out capability
    - Supports bus monitor mode.
    - Supports Power down wake-up by data toggle or address match
    - Supports setup/hold time programmable
    - Supports multiple address recognition (two slave address with mask option)

- UART
  - Supports up to 3 sets of UART
  - Full-duplex asynchronous communications
  - Separates receive and transmit 16/16 bytes entry FIFO for data payloads
  - Supports hardware auto-flow control (RX, TX, CTS and RTS)
  - Programmable receiver buffer trigger level
  - Supports programmable baud rate generator for each channel individually
  - Supports 8-bit receiver buffer time-out detection function
  - Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])

4.1.2 NuMicro® M0564 Base Series (M051 Compatible) Selection Guide

Part Number	Flash (KB)	SRAM (KB)	Data Flash(KB)	SPROM(KB)	ISP ROM (KB)	I/O	Timer/PWM	PWM	Connectivity					ADC(12-Bit)	ACMP	PDMA	VBAT(RTC)	LVIO	EBI	ICP/IAP/ISP	Package
									USCI*	UART	SC/UART	SPI/I^2S	I^2C								
M0564LE4AE	128	20	**Conf***	2	4	41	4	12	3	3	2	2	2	10-ch	2	5	--	√	√	√	LQFP48
M0564LG4AE	256	20	**Conf***	2	4	41	4	12	3	3	2	2	2	10-ch	2	5	--	√	√	√	LQFP48
M0564SE4AE	128	20	**Conf***	2	4	53	4	12	3	3	2	2	2	15-ch	2	5	√	√	√	√	LQFP64*
M0564SG4AE	256	20	**Conf***	2	4	53	4	12	3	3	2	2	2	15-ch	2	5	√	√	√	√	LQFP64*
M0564VG4AE	256	20	**Conf***	2	4	85	4	12	3	3	2	2	2	20-ch	2	5	√	√	√	√	LQFP100

Conf*: Configurable
USCI*: support UART, SPI or I^2C
LQFP64*: 7x7 mm

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			TM3	I/O	MFP6	Timer3 event counter input/toggle output pin.
			EBI_ALE	O	MFP7	EBI address latch enable output pin.
7	10	15	PD.1	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH19	A	MFP1	ADC0 channel 19 analog input.
			PWM0_SYNC_IN	I	MFP2	PWM0 counter synchronous trigger input pin.
			UART0_TXD	O	MFP3	UART0 data transmitter output pin.
			USCI2_CLK	I/O	MFP4	USCI2 clock pin.
			ACMP1_P2	A	MFP5	Analog comparator 1 positive input 2 pin.
			TM0	I/O	MFP6	Timer0 event counter input/toggle output pin.
			EBI_nRD	O	MFP7	EBI read enable output pin.
8	11	16	PD.2	I/O	MFP0	General purpose digital I/O pin.
			ADC0_ST	I	MFP1	ADC0 external trigger input pin.
			TM0_EXT	I/O	MFP3	Timer0 external capture input/toggle output pin.
			USCI2_DAT0	I/O	MFP4	USCI2 data 0 pin.
			ACMP1_P1	A	MFP5	Analog comparator 1 positive input 1 pin.
			PWM0_BRAKE0	I	MFP6	PWM0 Brake 0 input pin.
			EBI_nWR	O	MFP7	EBI write enable output pin.
			INT0	I	MFP8	External interrupt 0 input pin.
9	12	17	PD.3	I/O	MFP0	General purpose digital I/O pin.
			TM2	I/O	MFP1	Timer2 event counter input/toggle output pin.
			SPI0_I2SMCLK	I/O	MFP2	SPI0 I2S master clock output pin
			TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin.
			USCI2_DAT1	I/O	MFP4	USCI2 data 1 pin.
			ACMP1_P0	A	MFP5	Analog comparator 1 positive input 0 pin.
			PWM0_BRAKE1	I	MFP6	PWM0 Brake 1 input pin.
			EBI_MCLK	O	MFP7	EBI external clock output pin.
			INT1	I	MFP8	External interrupt 1 input pin.
10		18	PD.4	I/O	MFP0	General purpose digital I/O pin.
			SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
			I2C0_SDA	I/O	MFP3	I2C0 data input/output pin.
			UART2_nRTS	O	MFP4	UART2 request to Send output pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			EBI_AD6	I/O	MFP7	EBI address/data bus bit 6.
	40	64	PA.5	I/O	MFP0	General purpose digital I/O pin.
			SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
			TM2_EXT	I/O	MFP3	Timer2 external capture input/toggle output pin.
			TM_BRAKE3	I	MFP6	Timer Brake 3 input pin.
			EBI_AD5	I/O	MFP7	EBI address/data bus bit 5.
	41	65	PA.4	I/O	MFP0	General purpose digital I/O pin.
			SPI1_SS	I/O	MFP2	SPI1 slave select pin.
			TM3_EXT	I/O	MFP3	Timer3 external capture input/toggle output pin.
			EBI_AD4	I/O	MFP7	EBI address/data bus bit 4.
		66	V_{SS}	P	MFP0	Ground pin for digital circuit.
		67	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
		68	PE.1	I/O	MFP0	General purpose digital I/O pin.
			TM3_EXT	I/O	MFP3	Timer3 external capture input/toggle output pin.
			SC0_nCD	I	MFP5	Smart Card 0 card detect pin.
			PWM0_CH1	I/O	MFP6	PWM0 channel 1 output/capture input.
	42	69	PE.8	I/O	MFP0	General purpose digital I/O pin.
			UART1_TXD	O	MFP1	UART1 data transmitter output pin.
			TM0	I/O	MFP3	Timer0 event counter input/toggle output pin.
			I2C1_SCL	I/O	MFP4	I2C1 clock pin.
			SC0_PWR	O	MFP5	Smart Card 0 power pin.
	43	70	PE.9	I/O	MFP0	General purpose digital I/O pin.
			UART1_RXD	I	MFP1	UART1 data receiver input pin.
			TM1	I/O	MFP3	Timer1 event counter input/toggle output pin.
			I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
			SC0_RST	O	MFP5	Smart Card 0 reset pin.
32	44	71	PE.10	I/O	MFP0	General purpose digital I/O pin.
			SPI1_MISO	I/O	MFP1	SPI1 MISO (Master In, Slave Out) pin.
			SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.
			UART1_nCTS	I	MFP3	UART1 clear to Send input pin.
			SC0_DAT	I/O	MFP5	Smart Card 0 data pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			EBI_nWRL	O	MFP7	EBI low byte write enable output pin.
			INT1	I	MFP8	External interrupt 1 input pin.
44	58	92	PB.1	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH1	A	MFP1	ADC0 channel 1 analog input.
			VDET_P1	A	MFP2	Voltage detector positive input 1 pin.
			UART2_TXD	O	MFP3	UART2 data transmitter output pin.
			TM3	I/O	MFP4	Timer3 event counter input/toggle output pin.
			SC0_RST	O	MFP5	Smart Card 0 reset pin.
			PWM0_SYNC_OUT	O	MFP6	PWM0 counter synchronous trigger output pin.
			EBI_nWRH	O	MFP7	EBI high byte write enable output pin
			USCI1_DAT1	I/O	MFP8	USCI1 data 1 pin.
45	59	93	PB.2	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH2	A	MFP1	ADC0 channel 2 analog input.
			SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
			SPI1_CLK	I/O	MFP3	SPI1 serial clock pin.
			UART1_RXD	I	MFP4	UART1 data receiver input pin.
			SC0_nCD	I	MFP5	Smart Card 0 card detect pin.
			TM_BRAKE0	I	MFP6	Timer Brake 0 input pin.
			EBI_nCS0	O	MFP7	EBI chip select 0 output pin.
			USCI0_DAT0	I/O	MFP8	USCI0 data 0 pin.
46	60	94	PB.3	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH3	A	MFP1	ADC0 channel 3 analog input.
			SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.
			SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin.
			UART1_TXD	O	MFP4	UART1 data transmitter output pin.
			TM_BRAKE1	I	MFP6	Timer Brake 1 input pin.
			EBI_ALE	O	MFP7	EBI address latch enable output pin.
			USCI0_DAT1	I/O	MFP8	USCI0 data 1 pin.
47	61	95	PB.4	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH4	A	MFP1	ADC0 channel 4 analog input.
			SPI0_SS	I/O	MFP2	SPI0 slave select pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PE.13	MFP4	I/O	
		PA.2	MFP4	I/O	
I2C1	I2C1_SCL	PF.3	MFP3	I/O	I2C1 clock pin.
		PC.9	MFP3	I/O	
		PC.4	MFP3	I/O	
		PE.4	MFP3	I/O	
		PE.8	MFP4	I/O	
	I2C1_SDA	PF.4	MFP3	I/O	I2C1 data input/output pin.
		PC.10	MFP3	I/O	
		PE.0	MFP3	I/O	
		PC.5	MFP3	I/O	
		PE.5	MFP3	I/O	
		PE.9	MFP4	I/O	
ICE	ICE_CLK	PE.6	MFP1	I	Serial wired debugger clock pin.
	ICE_DAT	PE.7	MFP1	O	Serial wired debugger data pin.
INT0	INT0	PD.2	MFP8	I	External interrupt 0 input pin.
		PE.4	MFP8	I	
		PA.0	MFP8	I	
INT1	INT1	PD.3	MFP8	I	External interrupt 1 input pin.
		PE.5	MFP8	I	
		PB.0	MFP8	I	
INT2	INT2	PC.0	MFP8	I	External interrupt 2 input pin.
INT3	INT3	PD.0	MFP8	I	External interrupt 3 input pin.
INT4	INT4	PE.0	MFP8	I	External interrupt 4 input pin.
INT5	INT5	PF.0	MFP8	I	External interrupt 5 input pin.
PWM0	PWM0_BRAKE0	PD.2	MFP6	I	PWM0 Brake 0 input pin.
		PD.4	MFP5	I	
	PWM0_BRAKE1	PD.3	MFP6	I	PWM0 Brake 1 input pin.
		PD.5	MFP5	I	
	PWM0_CH0	PC.0	MFP6	I/O	PWM0 channel 0 output/capture input.
		PE.0	MFP6	I/O	
	PWM0_CH1	PC.1	MFP6	I/O	PWM0 channel 1 output/capture input.

6.2.5 System Memory Map

The M0564 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-5. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The M0564 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128 KB)
0x0000_0000 – 0x0003_FFFF	FLASH_BA	FLASH Memory Space (256 KB)
0x0004_0000 – 0x0005_FFFF	Reserved	Reserved
0x0006_0000 – 0x0007_FFFF	Reserved	Reserved
0x2000_0000 – 0x2000_4FFF	SRAM_BA	SRAM Memory Space (20 KB)
0x2000_4000 – 0x2000_BFFF	Reserved	Reserved
0x2000_C000 – 0x2000_FFFF	Reserved	Reserved
0x6000_0000 – 0x601F_FFFF	EXTMEM_BA	External Memory Space for EBI Interface (2 MB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	SYS_BA	System Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_BA	EBI Control Registers
0x5001_4000 – 0x5001_7FFF	HDIV_BA	Hardware Divider Registers
0x5001_8000 – 0x5001_FFFF	CRC_BA	CRC Generator Registers
Peripheral Controllers Space (0x4000_0000 – 0x401F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWM0_BA	PWM0 Control Registers
0x4004_4000 – 0x4004_7FFF	Reserved	Reserved
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	Reserved	Reserved
0x4007_0000 – 0x4007_3FFF	USCI0_BA	USCI0 Control Registers

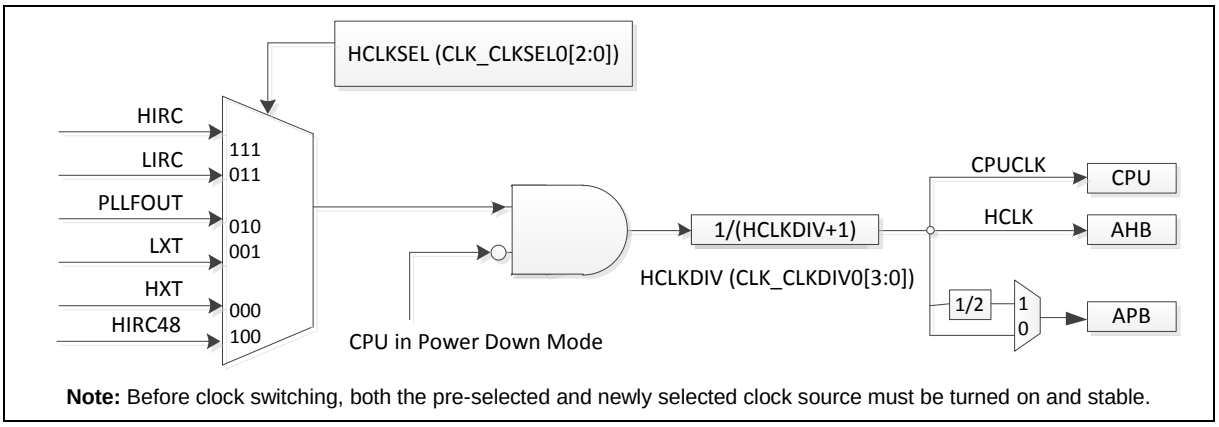
SysTick	15	0x0000003C	Configurable
Interrupt (IRQ0 ~ IRQ)	16 ~ 47	0x00000000 + (Vector Number)*4	Configurable

Table 6.2-6 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BOD_INT	Brown-out low voltage detected interrupt
17	1	WDT_INT	Window Watchdog Timer interrupt
18	2	EINT024	External interrupt from PA.0/PC.0/PD.2/PE.0/PE.4 pin
19	3	EINT135	External interrupt from PB.0/PC.0/ PD.0/PD.3/PE.5/PF.0 pin
20	4	GPAB_INT	External signal interrupt from PA[15:0]/PB[13:0]
21	5	GPCDEF_INT	External interrupt from PC[15:0]/PD[15:0]/PE[13:0]/PF[7:0]
22	6	PWM0_INT	PWM0 interrupt
23	7	PWM1_INT	PWM1 interrupt
24	8	TMR0_INT	Timer 0 interrupt
25	9	TMR1_INT	Timer 1 interrupt
26	10	TMR2_INT	Timer 2 interrupt
27	11	TMR3_INT	Timer 3 interrupt
28	12	UART02_INT	UART0 and UART2 interrupt
29	13	UART1_INT	UART1 interrupt
30	14	SPI0_INT	SPI0 interrupt
31	15	SPI1_INT	SPI1 interrupt
32	16		Reserved
33	17		Reserved
34	18	I2C0_INT	I^2C0 interrupt
35	19	I2C1_INT	I^2C1 interrupt
36	20		Reserved
37	21		Reserved
38	22	USCI_INT	USCI0, USCI1 and USCI2 interrupt
39	23		Reserved
40	24	SC_INT	SC0 and SC1 interrupt
41	25	ACMP01_INT	Analog Comparator interrupt

6.3.2 System Clock and SysTick Clock

The system clock has 6 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0 [2:0]). The block diagram is shown in Figure 6.3-3.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-3 System Clock Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIEN (CLK_CLKDCTL[5]) is set to 1. User can trying to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

The HXT clock stop detect and system clock switch to HIRC procedure is shown in Figure 6.3-4.

6.6 Analog-to-Digital Converter (ADC)

6.6.1 Overview

The M0564 series contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with twenty input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin (STADC/PD.2), timer0~3 overflow pulse trigger and PWM trigger.

6.6.2 Features

- Analog input voltage range: 0 ~ AV_{DD}.
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 20 single-end analog input channels or 10 differential analog input channels
- Maximum ADC peripheral clock frequency is 16 MHz
- Up to 800k SPS sampling rate
- Configurable ADC internal sampling time
- Four operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST bit
  - External pin (STADC)
  - Timer 0~3 overflow pulse trigger
  - PWM trigger with optional start delay period
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- 3 internal channels, they are band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}), and Battery power (V_{BAT})
- Support PDMA transfer mode.

Note1: ADC sampling rate = (ADC peripheral clock frequency) / (total ADC conversion cycle)

Note2: If the internal channel (V_{TEMP}) is selected to convert, the sampling rate needs to be less than 300k SPS for accurate result.

Note3: If the internal channel for band-gap voltage is active, the maximum sampling rate will be 300k SPS.

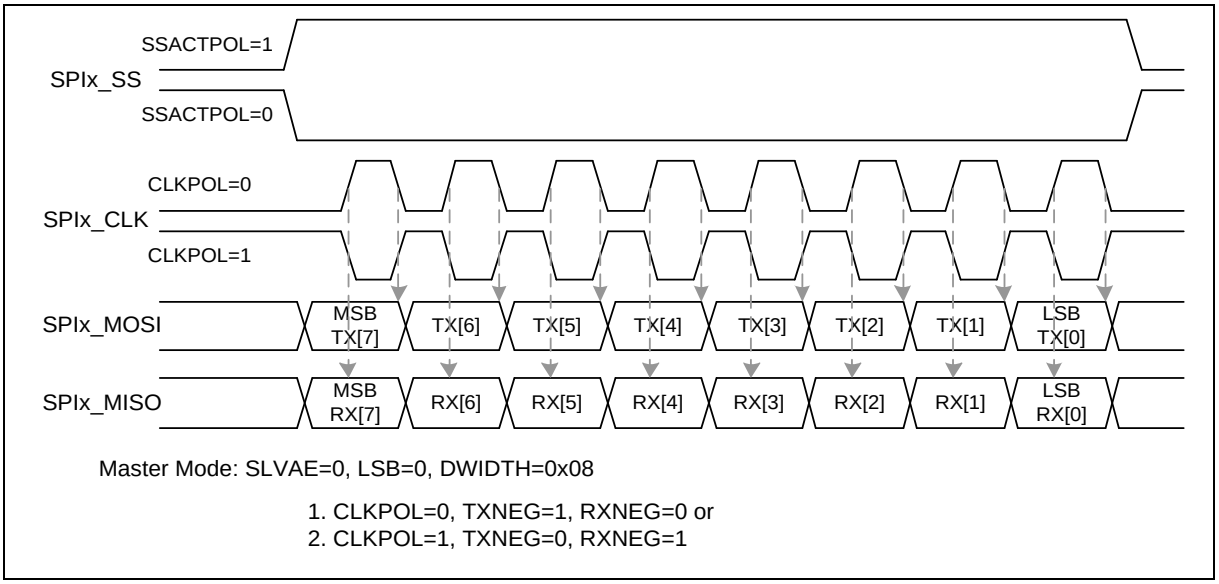


Figure 6.16-1 SPI Timing in Master Mode

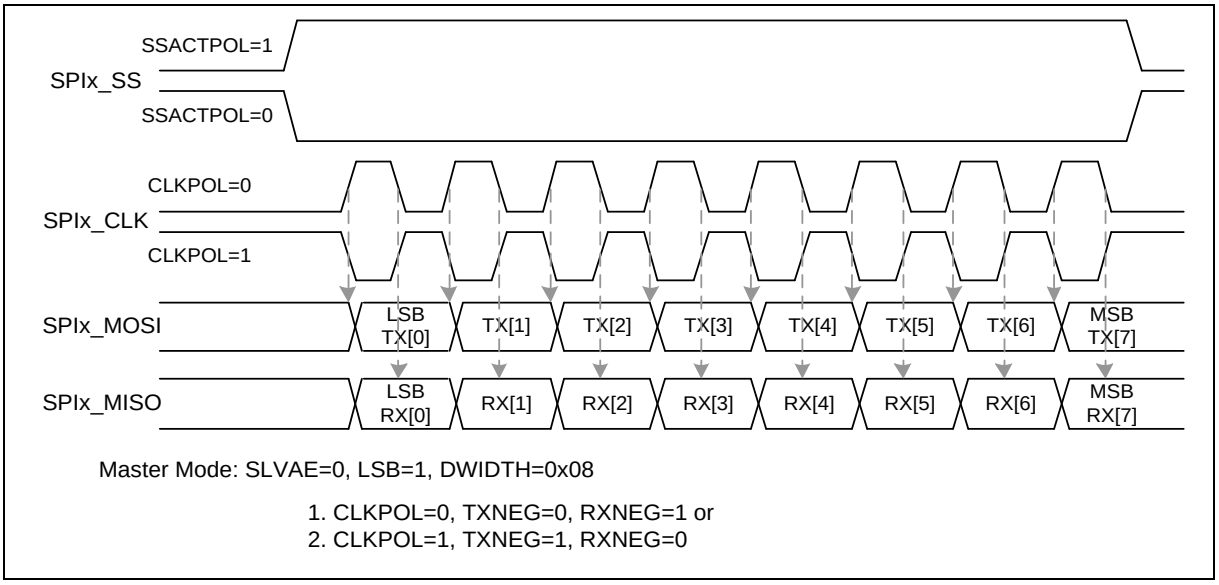


Figure 6.16-2 SPI Timing in Master Mode (Alternate Phase of SPIx_CLK)

6.17 Timer Controller (TMR)

6.17.1 Overview

The Timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The Timer controller also provides four PWM generators. Each PWM generator supports two PWM output channels in independent mode and complementary mode. The output state of PWM output pin can be control by pin mask, polarity and break control, and dead-time generator.

6.17.2 Features

6.17.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer equips one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, ADC and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports Inter-Timer trigger mode

6.17.2.2 PWM Function Features

- Supports maximum clock frequency up to 72MHz
- Supports independent mode for PWM generator with two output channels
- Supports complementary mode for PWM generator with paired PWM output channel
  - 12-bit dead-time insertion with 12-bit prescale
- Supports 12-bit prescale from 1 to 4096
- Supports 16-bit PWM counter
  - Up, down and up-down count operation type
  - One-shot or auto-reload counter operation mode
- Supports mask function and tri-state enable for each PWM output pin
- Supports brake function

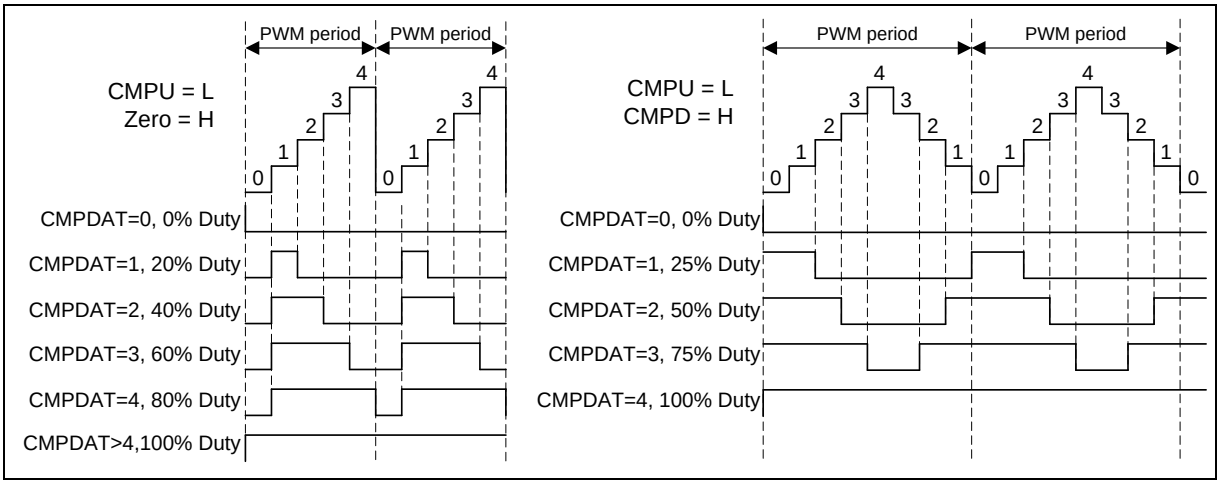


Figure 6.17-9 PWM 0% to 100% Duty Cycle in Up Count Type and Up-Down Count Type

6.17.3.11 PWM Output Mode

The PWM supports two output modes: independent mode which may be applied to DC motor system, complementary mode with dead-time insertion which may be used in the application of AC induction motor and permanent magnet synchronous motor.

6.17.3.12 Independent mode

When OUTMODE (TIMERx_PWMCTL[16]) bit is set to 0, PWM output operates in independent mode. In this mode, both PWMx_CH0 and PWMx_CH1 can output the same waveform as shown in Figure 6.17-10.

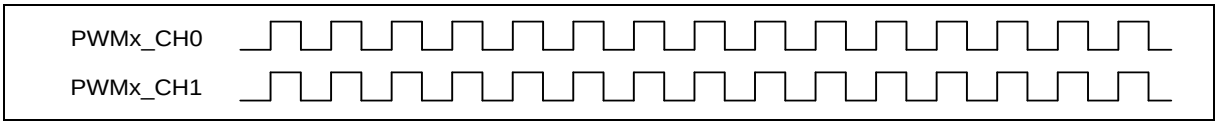


Figure 6.17-10 PWM Independent Mode Output Waveform

6.17.3.13 Complementary mode

When OUTMODE (TIMERx_PWMCTL[16]) bit is set to 1, PWM output operates in complementary mode. In this mode, both PWMx_CH0 and PWMx_CH1 can output waveform and PWMx_CH1 must always be the complement of PWMx_CH0 as shown in Figure 6.17-11.

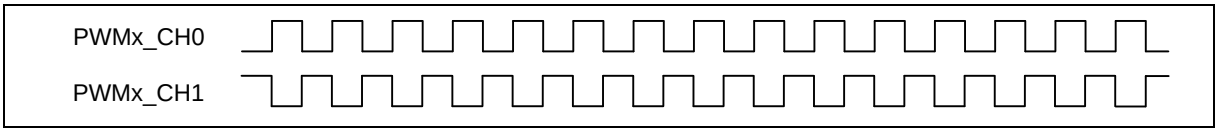


Figure 6.17-11 PWM Complementary Mode Output Waveform

6.17.3.14 PWM Output Control

After PWM pulse generator, there are four steps to control output waveform in independent output mode and five control steps in complementary output mode. User can set POEN0 (TIMERx_PWMPOEN[0]) and POEN1 (TIMERx_PWMPOEN[1]) 1 to enable PWMx_CH0 and PWMx_CH1 output waveform.

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	V_{DD}-V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} – 0.3	V_{DD} + 0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+105	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into V_{DD}	I_{DD}	-	120	mA
Maximum Current out of V_{SS}	I_{SS}	-	120	mA
Maximum Current sunk by a I/O Pin	I_{IO}	-	35	mA
Maximum Current Sourced by a I/O Pin		-	35	mA
Maximum Current Sunk by Total I/O Pins		-	100	mA
Maximum Current Sourced by Total I/O Pins		-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affect the lift and reliability of the device.

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS					
		MIN.	TYP.	MAX.	UNIT						
while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE18}	-	2.2	-	mA	5.5 V	24 MHz	X	X	X	X
	I_{IDLE19}	-	12.5	-	mA	3.3 V	24 MHz	X	X	X	V
	I_{IDLE20}	-	2.2	-	mA	3.3 V	24 MHz	X	X	X	X
Operating Current Idle Mode HCLK =24 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE21}	-	TBD	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	X	X	HIRC48/2	X	V
	I_{IDLE22}	-	TBD	-	mA	5.5 V	X	X	HIRC48/2	X	X
	I_{IDLE23}	-	TBD	-	mA	3.3 V	X	X	HIRC48/2	X	V
	I_{IDLE24}	-	TBD	-	mA	3.3 V	X	X	HIRC48/2	X	X
Operating Current Idle Mode HCLK =22.1184 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE25}	-	12.3	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	X	V	X	X	V
	I_{IDLE26}	-	1.9	-	mA	5.5 V	X	V	X	X	X
	I_{IDLE27}	-	12.3	-	mA	3.3 V	X	V	X	X	V
	I_{IDLE28}	-	1.9	-	mA	3.3 V	X	V	X	X	X
Operating Current Idle Mode HCLK =12 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE29}	-	6.3	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	12 MHz	X	X	X	V
	I_{IDLE30}	-	1.2	-	mA	5.5 V	12 MHz	X	X	X	X
	I_{IDLE31}	-	6.3	-	mA	3.3 V	12 MHz	X	X	X	V
	I_{IDLE32}	-	1.2	-	mA	3.3 V	12 MHz	X	X	X	X
Operating Current Idle Mode HCLK =4 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE33}	-	2.2	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	4 MHz	X	X	X	V
	I_{IDLE34}	-	0.50	-	mA	5.5 V	4 MHz	X	X	X	X
	I_{IDLE35}	-	2.2	-	mA	3.3 V	4 MHz	X	X	X	V
	I_{IDLE36}	-	0.46	-	mA	3.3 V	4 MHz	X	X	X	X
Operating Current Idle Mode HCLK =32.768 kHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE37}	-	129	-	uA	V_{DD}	LXT	LIRC	PLL	All digital module	
						5.5 V	32.768 kHz	X	X	V	
	I_{IDLE38}	-	115	-	uA	5.5 V	32.768 kHz	X	X	X	
	I_{IDLE39}	-	115	-	uA	3.3 V	32.768 kHz	X	X	V	
	I_{IDLE40}	-	101	-	uA	3.3 V	32.768 kHz	X	X	X	
Operating Current Idle Mode HCLK =10 kHz while(1){}executed from flash	I_{IDLE41}	-	119	-	uA	V_{DD}	LXT	LIRC	PLL	All digital module	
						5.5 V	X	10 kHz	X	V	
	I_{IDLE42}	-	114	-	uA	5.5 V	X	10 kHz	X	X	

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input Low Voltage (Schmitt input for V_{DDIO} domain)	V_{IL4}	-0.3	-	$0.3V_{DD}$	V	V_{DDIO} = 1.8 ~ 5.5V
Input High Voltage (Schmitt input)	V_{IH3}	$0.7V_{DD}$	-	V_{DD} + 0.3	V	$V_{DD} = V_{BAT} = V_{DDIO}$ = 2.5 ~ 5.5V
Input High Voltage (Schmitt input for V_{DDIO} domain)	V_{IH4}	$0.7V_{DDIO}$	-	V_{DDIO} + 0.3	V	V_{DDIO} = 1.8 ~ 5.5V
Hysteresis voltage of PA~PF (Schmitt input)	V_{HY}	-	$0.2V_{DD}$	-	V	
Negative going threshold (Schmitt input), nRESET	V_{IL5}	-0.3	-	$0.2V_{DD}$	V	
Positive going threshold (Schmitt Input), nRESET	V_{IH5}	$0.8V_{DD}$	-	V_{DD} + 0.3	V	
Internal nRESET pin pull up resistor	R_{RST}	-	16	-	KΩ	V_{DD} = 5.5V
Source Current (Quasi-bidirectional Mode)	I_{SR1}	-	-400	-	uA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 4.5V, V_S = 2.4V
	I_{SR2}	-	-80	-	uA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 2.7V, V_S = 2.2V
	I_{SR3}	-	-73	-	uA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 2.5V, V_S = 2.0V
Source Current (Quasi-bidirectional Mode for V_{DDIO} domain)	I_{SR4}	-	-19	-	uA	$V_{DD} = V_{BAT}$ = 2.5 ~ 5.5V V_{DDIO} = 1.8V, V_S = 1.6V
Source Current (Push-pull Mode)	I_{SR5}	-	-26		mA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 4.5V, V_S = 2.4V
	I_{SR6}	-	-5.8	-	mA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 2.7V, V_S = 2.2V
	I_{SR7}	-	-5.2	-	mA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 2.5V, V_S = 2.0V
Source Current (Push-pull Mode for V_{DDIO} domain)	I_{SR8}	-	-1.5	-	mA	$V_{DD} = V_{BAT}$ = 2.5 ~ 5.5V V_{DDIO} = 1.8V, V_S = 1.6V
Sink Current (Quasi-bidirectional, Open-Drain and Push-pull Mode)	I_{SK1}	-	15	-	mA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 4.5V, V_S = 0.45V
	I_{SK2}	-	10	-	mA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 2.7V, V_S = 0.45V
	I_{SK3}	-	9	-	mA	$V_{DD} = V_{BAT} = V_{DDIO}$ = 2.5V, V_S = 0.45V

8.3.4 External 32.768 kHz Low Speed Crystal (LXT) Input Clock

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{LXT}	-	32.768	-	kHz	$V_{DD} = V_{BAT}$ = 2.5 ~ 5.5V
Temperature	T_{LXT}	-40	-	+105	°C	
Operating current	I_{LXT}		0.7		μA	$V_{DD} = V_{BAT}$ = 2.5 ~ 5.5V

8.3.4.1 Typical Crystal Application Circuits

CRYSTAL	C3	C4	R2
32.768 kHz	20pF	20pF	without

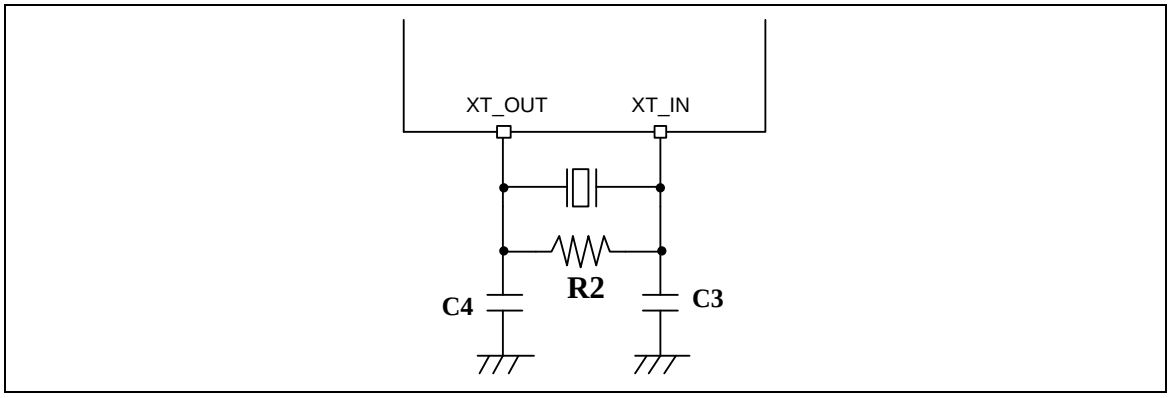


Figure 8.3-2 Typical Crystal Application Circuit

8.6 I2C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	SCL low period	4.7	-	1.2	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	20+0.1Cb	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I^2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I^2C frequency.
3. I^2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

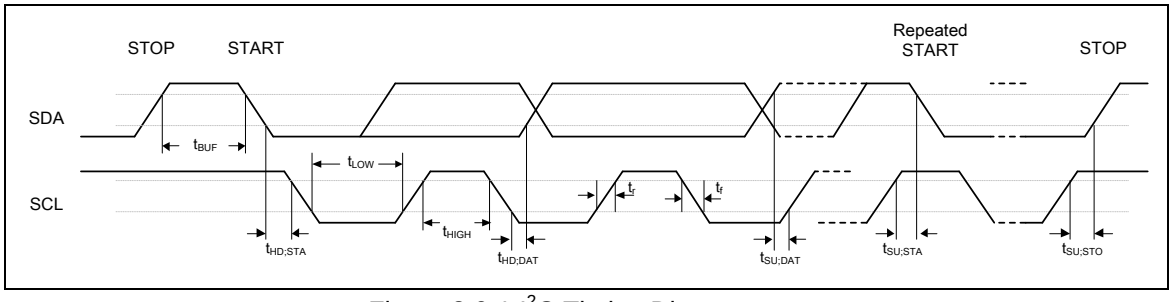
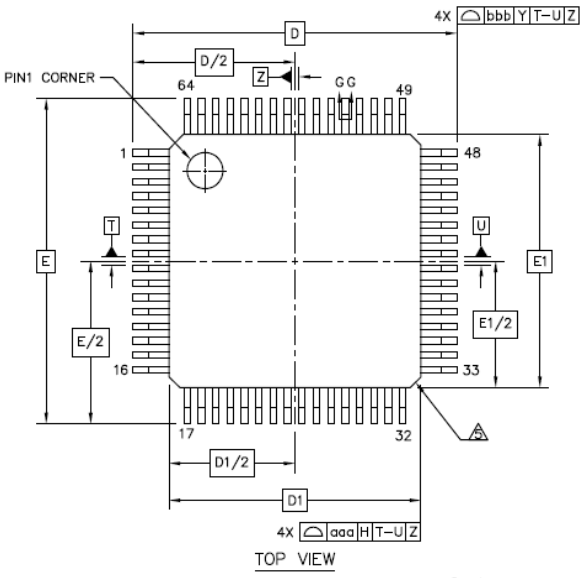


Figure 8.6-1 I^2C Timing Diagram

9.2 LQFP 64L (7x7x1.4 mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05